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Edge-Triggered Pulsed Sequential Elements with SoC Applications

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Abstract **-** The System-On-Chip (SoC) design is integrating hundreds of millions of transistors on one chip, whereas packaging and cooling only have a limited ability to remove the excess heat. In this paper, various design techniques for a low power clocking system are surveyed. Among them is an effective way to reduce capacity of the clock load by minimizing number of clocked transistors. To approach this, we propose a novel clocked pair shared flip-flop which reduces the number of local clocked transistors by approximately 40%. A 24% reduction of clock driving power is achieved. In addition, low swing and double edge clocking, can be easily incorporated into the new flip-flop to build clocking systems.

Keywords: *Flip-flops, latches, clocking, dual edge-triggered, low power, level conversion.*

I. INTRODUCTION

System-on-chip (SoC) design will integrate hundreds of millions of transistors on one chip, whereas packaging and cooling only have a limited ability to remove the excess heat. All of these result in power consumption being one of the main problems in achieving high-performance design. Due to quadratic relations between voltage and power consumption, reducing the supply voltage is very efficient in decreasing power dissipation. A clustered voltage scaling (CVS) scheme has been developed in [1]. In the CVS scheme, by using low supply voltage (VDDL) in noncritical paths, i.e., placing speed insensitive gates with supply voltage VDDL, and using high supply voltage (VDDH) in speed sensitive paths, the whole system power consumption could be reduced without degrading the performance. To implement CVS scheme in a chip, a level converter must be used when a gate, which is supplied by the low supply voltage VDDL, connects to a gate that is supplied by high supply voltage VDDH. The reason is that the data or clock from a low supply voltage block cannot connect to a p-type metal–oxide–semiconductor (PMOS) in a VDDH block directly, since the PMOS cannot be shut off with low supply voltage VDDL. Notice that the dual Vdd system has an overhead, being that it needs an extra power supply line for VDDL causing an area overhead in addition to the level converter's delay and power penalty. One of the main challenges in the CVS system is to design level converters with less power and latency overhead [2] to interface low-voltage blocks with high-voltage blocks.

This paper surveys various level-shifting schemes in LCFFs and classifies them into three types: differential level-shifting scheme style, n-type metal–oxide–semiconductor (NMOS) pass-transistor style, and precharged style. We also propose a novel LCFF design with lower power consumption overhead.

There is a wide selection of flip-flops in the literature [1]–[8]. Many contemporary microprocessors selectively use master-slave and pulsed-triggered flip-flops [2]. Traditional master-slave single-edge flip-flops, for example, transmission gated flip-flop [3], are made up of two stages, one master and one slave. Another edge-triggered flip-flop is the sense amplifier-based flip-flop (SAFF) [4]. All of these hard edged-flip-flops are characterized by a positive setup time, causing large D-to-Q delays. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. 95% of all static timing latching on the Itanium 2 processor use pulsed clocking [5]. Pulse triggered flip-flops could be

classified into two types, implicit-pulsed and explicit-pulsed, for example, the implicit pulse-triggered data-close-to-output flip-flops (ip-DCO) [6] and the explicit pulse-triggered data-close-to-output flip-flops (ep-DCO) [6].

This paper surveys various low power techniques for the clocking system in Section II. After that we elaborate on the reduction of clock capacity to achieve low power in Section III, Section IV presents simulation results. Section V concludes this paper.

II. RELATED WORK

A global optimizer, which uses a robust, steepest-descent algorithm, is used to determine transistor sizes in the various flipflop topologies and minimize total energy per cycle (@ for different target values of data-to-Q *(D-Q)* delay. This process results in a plot of energy versus delay for each flip-flop, which simplifies comparisons between flops. Setup times and clock-to- Q delays for "low" and "high" values of input data are measured by sweeping the arrival time of data with respect to the rising clock edge and determining the point at which the data-to-Q delay is minimized *[5]*. Output storage nodes of all flops are protected from direct noise coupling by a single inverter. Therefore, some flip-flops are inverting while others are non-inverting. A constant output load of 20fF is used for all flops. Limiting the input capacitance value to 5fF sets maximum sizes of the inverters driving the data and clock inputs to the flops.

The typical pulse width is set to 90ps for all pulsed flops so that the worst-case min-delay requirement in the logic cone feeding the flop is less than half the clock period for 3Ghz operation.

Because the hold time of a pulsed flip-flop is roughly equal to the pulse width, this restriction provides a reasonable compromise between the pulsed flop's time-borrowing capability and logic design efforts needed to meet worst-case hold time requirements. In addition, designs which employ an explicit clocking pulse must ensure that the pulse width is large enough that data will correctly be captured across all process, voltage, and temperature comers. Maximum voltage droop criteria at intermediate and output storage nodes are used to size the keeper transistors for adequate robustness, and to determine hold times. Transition activity of input data is assumed to be one-tenth of clock signal activity and all simulations are conducted in a 0.13pm technology using low- Vt transistors at 1.1 1V supply and 110°C.

Designing Issues

Based on the following factors, there are various ways to lower the power consumption shown as follows.

1) ***Double Edge Triggering:*** Using half frequency on the clock distribution network will save approximately half of the power consumption on the clock distribution network. However the flip-flop must be able to be double clock edge triggered. For example, the clock branch shared implicit pulsed flip-flop [7] (CBS-ip DEFF), is a double edge triggered flip-flop. Double clock edge triggering method reduces the power by decreasing frequency in equation.

2) Using a low swing voltage on the clock distribution network can reduce the clocking power consumption since power is a quadratic function of voltage. To use low swing clock distribution, the flip-flop should be a low swing flip- flop. For example, low swing double-edge flip-flop (LSDFF) [8] is a low swing flip-flop. In addition, the level converter flip-flop is a natural candidate tobe used in low swing environment too. For example, CD-LCFF-ip [9], could be used as a low swing flip-flop since incoming signals only drive nMOS transistors. The low swing method reduces the power consumption by decreasing voltage in equation.

3) There are two ways to reduce the switching activity: conditional operation (eliminate redundant data switching: conditional discharge flip-flop (CDFF) [10], conditional capture flip-flop (CCFF) [7]) or clock gating.

a) ***Conditional Operation.***

For dynamic flip-flops, like hybrid latch flip-flop (HLFF) [1], semi dynamic flip-flop (SDFF) [3], there are redundant switching activities in the internal node. When input stays at logic one, the internal node is kept charging and discharging without performing any useful computation. The conditional operation technique is needed to control the redundant switching. For example, in CDFF, a feedback transistor is inserted on the discharging path of 1st stage which will turn off the discharging path when keeps 1. Internal node will not be kept discharging at every clock cycle. In CCFF, it uses a clocked NOR gate to control an nMOS transistor in discharging path when _ keeps 1. The redundant switching activity is removed in both cases. This reduces the power consumption by decreasing data activity in the equation.

b) ***Clock Gating:***

When a certain block is idle, we can disable the clock signal to that block to save power. Gated master slave flip-flop was proposed in [4]. Both conditional operation and clock gating methods reduce power by decreasing switching activity.

4) Using Dual Vt/MTCMOS to reduce the leakage power in standby mode. With shrinking feature size, the leakage current increases rapidly, the MTMOS

technique [5] as well as transistor stacking, dynamic body biasing, and supply voltage ramping could be used to reduce leakage standby power consumption [6]. A data retention flip-flop is proposed in [7].

5) *Reducing Short Current Power:* split path can reduce the short current power, since pMOS and nMOS are driven by separate signals.

6) ***Reducing Capacity of Clock Load:*** 80% of nonclocked nodes have switching activity less than 0.1. This means reducing power of clocked nodes is important since clocked node has 100% activity. One effective way of low power design for clocking system is to reduce clock capacity load by minimizing number of clocked transistor.

Any local clock load reduction will also decrease the global power consumption. This method reduces power by decreasing clock capacity in equation. We will elaborate more in the Next Section.

IV. MIMIMIZING THE CLOCKED TRANSISTORS

A large part of the on-chip power is consumed by the clock drivers [8]. It is desirable to have less clocked load in the system. CDFF and CCFF in Section II both have many clocked transistors. For example, CCFF used 14 clocked transistors, and CDFF used 15 clocked transistors. In contrast, conditional data mapping flip-flop (CDMFF, Fig. 1) [9] used only seven clocked transistors, resulting in about 50% reduction in the number of clocked transistors, hence CDMFF used less power than CCFF and CDFF.

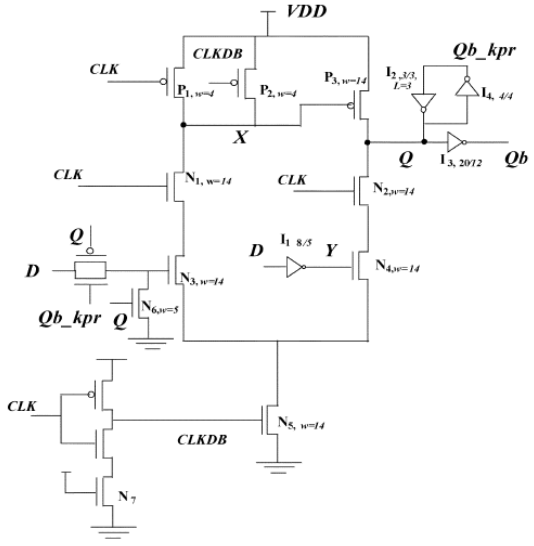

Fig 1.CDMFF.

This shows the effectiveness of reducing clocked transistor numbers to achieve low power. Since CDMFF outperforms CCFF and CDFF in view of power consumption, we do not discuss CCFF or CDFF further in this paper.

However, there is redundant clocking capacitance in CDMFF. When data remains 0 or 1, the precharging transistors, P1 and P2, keep switching without useful computation, resulting in redundant clocking. Clearly, it is necessary to reduce redundant power consumption here. Further, CDMFF has a floating node on critical path because its first stage is dynamic. When clock signal CLK transits from 0 to 1, CLKDB will stay 1 for a short while which produces an implicit pulse window for evaluation.

During that window, both P1, P2 are off. In addition, if D transits from 0 to 1, the pull down network will be disconnected by N3 using data mapping scheme (N6 turns off N3); If D is 0, the pull down network is disconnected from GND too. Hence internal node X is not connected with Vdd or GND during most pulse windows, it is essentially floating periodically.

With feature size shrinking, dynamic node is more prone to noise interruption because of the undriven dynamic node. If a nearby noise discharges the node X, PMOS transistor P3 will be partially on, and a glitch will appear on output node Q. In a nano scale circuit, a glitch not only consumes power but could propagate to the next stage which makes the system more vulnerable to noise. Hence, CDMFF could not be used in noise intensive environment.

V. SIMULATION RESULTS

The simulation results were obtained from HSPICE simulations in 0.18-_m CMOS technology at room temperature. VDD is 1.8 V.

The parasitic capacitances were extracted from the layouts. The setup used in our simulations is shown in Fig. 2. In order to obtain accurate results, we have simulated the circuits in a real environment, where the flip-flop inputs (clock, data) are driven by the input buffers, and the output is required to drive an output load. An inverter is placed after output Q, providing protection from direct noise coupling [6]. The value of the capacitance load at node Qb is 21 fF, which is selected to simulate a fan out of 14 minimum sized inverters (FO14) [2].

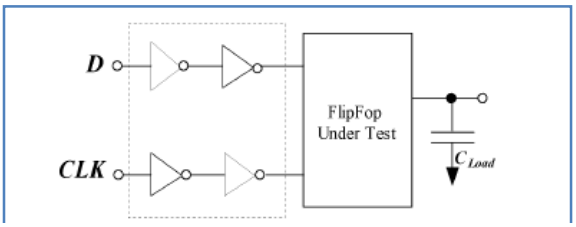

Fig 2.Flip Flop Setup used in Simulation

Assuming uniform data distribution, we have supplied input D with 16-cycle pseudorandom input data with an activity factor of 18.75% to reflect the average power consumption. A clock frequency of 250 MHz is used. Each design is simulated using the circuit at the layout level.

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TABLE I
COMPARING THE FLIP-FLOP IN TERMS OF DELAY, POWER, AND POWER DELAY PRODUCT

Design Name	# of tr	100% switching activity tr	Area λ^2	Total transistor width (um)	Low Swing	Double Edge	DQ (ps)	Clock power	Data driving power	Latching power	Total Power (uw)	PDP (fJ)
CDMFF	22	7	23407	23.2	N	difficult	387	6.25	0.42	5.29	11.98	4.63
CPS FF	19	4	23144	21.1	Y	easy	392	4.74	0.47	5.72	10.9	4.28

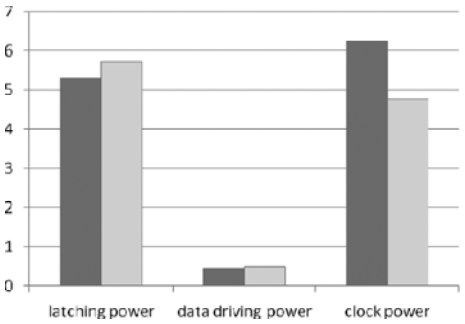

Fig 3. Power break down.

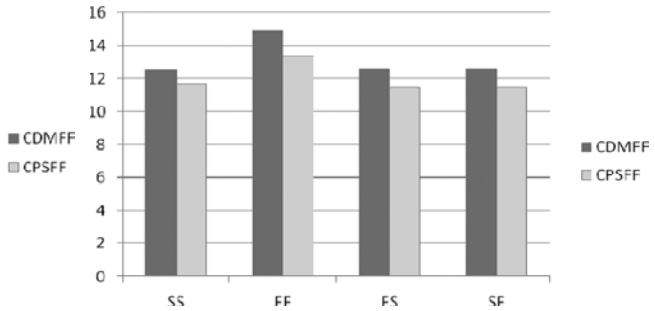

Fig 4. Power consumption at process corners

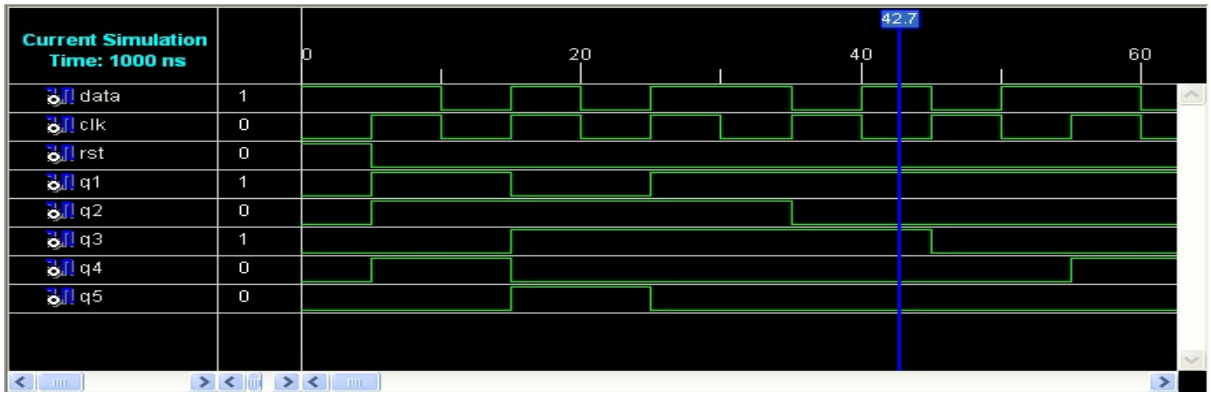

Fig 5. Simulation Results

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All capacitances were extracted from layout such that we can simulate the circuit more accurately.

This is because the internal gate capacitance, parasitic capacitance, and wiring capacitance affect the power consumption heavily in deep sub micrometer technology. Further the delay strongly depends on these capacitors.

The D-to-Q delay is obtained by sweeping the 0 -> 1 and 1->0 data transition times with respect to the clock edge and the minimum data-to-output delay corresponding to optimum set up time is recorded.

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