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FPGA Implementation of Convolutional Encoder And Hard Decision Viterbi Decoder

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Abstract **-** In this paper, we concern with designing and implementing a convolutional encoder and Viterbi decoder which are the essential block in digital communication systems using FPGA technology. Convolutional coding is a coding scheme used in communication systems including deep space communications and wireless communications. It provides an alternative approach to block codes for transmission over a noisy channel. The block codes can be applied only for the block of data. The convolutional coding has an advantage over the block codes in that it can be applied to a continuous data stream as well as to blocks of data.The motivation of this paper is to realize a Viterbi decoder having Constraint length 9 and code rate 1/2 by Xilinx 12.4i tools.

Keywords: *Convolutional encoder, Viterbi decoder, VHDL, Viterbi Algorithm., FPGA*

I. INTRODUCTION

Most digital communication systems nowadays convolutionally encoded the transmitted data to compensate for Additive White Gaussian Noise (AWGN), fading of the channel, quantization distortions and other data degradation effects. For its efficiency the Viterbi algorithm has proven to be a very practical algorithm for forward error correction of convolutionally encoded messages [1]. The requirements for the Viterbi decoder or Viterbi detector depend on the applications used. Most of the researches work to reduce cost, the power consumption, or work with high frequency for using the decoder in the modern applications.

The following discovery code was the cyclic codes. Cyclic codes are also called cyclic redundancy check (CRC) codes primarily used today for the error detection applications rather than for error correction [5]. Bose-Chaudhuri-Hocquenghem (BCH) codes are the important subclass of the cyclic codes which discovered by Hocquenghem in 1959 and by the team of Bose and Ray-Chaudhuri in 1960. Then the BCH codes were extended to the non-binay case (q > 2) by Reed and Solomon in 1960. All communication channels are subject to the additive white gaussian noise (AWGN) around the environment. Forward error correction (FEC) techniques are used in the transmitter to encode the data stream and receiver to detect and correct bits in errors, hence minimize the bit error rate (BER) to improve the performance. RS decoding algorithm complexity is relatively low and can be implemented in hardware at very high data rates. It seems to be an ideal code attributes for any application. However, RS codes perform very poorly in AWGN channel.

Due to weaknesses of using the block codes for error correction in useful channels, another approach of coding called convolutional coding had been introduced in 1955 [7]. Convolutional encoding with Viterbi decoding is a powerful FEC technique that is particularly suited to a channel in which the transmitted signal is corrupted mainly by AWGN. It operates on data stream and has memory that uses previous bits to encode. It is simple and has good performance with low implementation cost. The Viterby algorithm (VA) was proposed in 1967 by Andrew Viterbi [8] and is used for decoding a bitstream that has been encoded using FEC code. The convolutional encoder adds redundancy to a continuous stream of input data by using a linear shift register. The Convolutional Encoder and Viterbi Decoder used in the Digital Communications System is shown in Fig. 1.

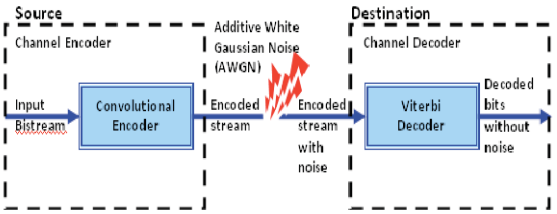

Fig 1. Convolutional encoder and Viterbi decoder.

II. CONVOLUTIONAL ENCODER

A convolutional code is a type of error-correcting code which differs a lot from block codes. First, the former does not have code words made up of distinct data sections and block sections. Instead, redundant bits are distributed throughout the coded data. Second, the encoder of the former contains memory and the *n* encoder outputs at any given time unit depend not only on the *k* inputs at that time unit but also on m previous input blocks. Convolutional codes are sometimes referred as trellis codes. Normally, convolutional encoding is simple, but decoding is much more difficult. Convolutional codes are usually characterized by two parameters and the patterns of *n* modulo-2 adders. The two important parameters are the code rate and constraint length. The code rate (k/n) where the number of output bits must equal or bigger than the input bits (*n_k*), is expressed as a ratio of the number of bits into the Convolutional encoder *k* to the number of channel symbols output by the Convolutional encoder *n* in a given encoder cycle. To convolutionally encode data, start with *m* memory registers, each holding 1 input bit. Unless otherwise specified, all memory registers start with a value of 0.The encoder has *n* modulo-2 adders, and *n* generator polynomials, one for each adder. An input bit *m1* is fed into the leftmost register. Using the generator polynomials and the existing values in the remaining registers, the encoder outputs *n* bits [1]. As shown in Figure 2, where we have a general encoder designed with a code rate (k/n) of 1/2 and an information sequence that is being shifted in to the register *m* of 1 bit at a time. The shift register has a constraint length (K) of 3, equal to the number of stages in the register. The output from the encoder is called code symbols. At initialization all stages in the encoder shall be initially set to zero. The output of the encoder is determined by the generator polynomial equations. Since the complexity of the encoder increases exponentially with the constraint length, none of the encoders uses more than a constraint length of 9, for practical reasons. [9] - [11].

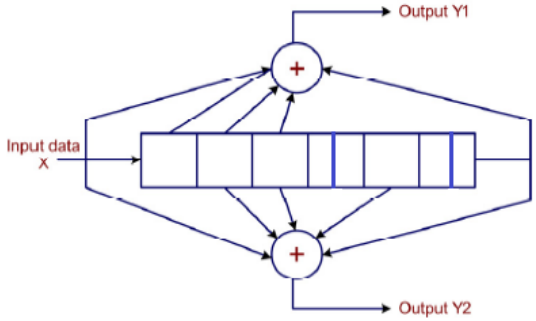

Fig 2. Convolutional encoder with constraint length k=9 and code rate (k/n)=1/2

III. VITERBI DECODER

A Viterbi decoder uses the VA for decoding a bitstream that has been encoded using FEC based on a convolutional code. The Viterbi Decoder is used in many FEC applications and in systems where data are transmitted and subject to errors before reception. The VA is commonly used in a wide range of communications and data storage applications. It is used for decoding convolutional codes, in base band detection for wireless systems, and also for detection of recorded data in magnetic disk drives. The requirements for the Viterbi decoder or Viterbi detector, which is a processor that implements the VA, depend on the applications where they are used. The block diagram of Viterbi decoder is shown in Fig. 3.

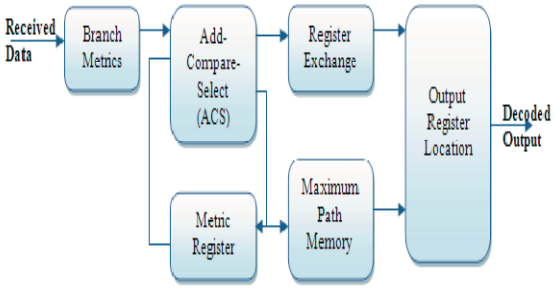

Fig.3 Viterbi decoder block diagram

The block diagram consists of the following modules: Branch Metrics, Add-Compare-Select (ACS), register exchange, maximum path metric selection, and output register selection [9], [11].

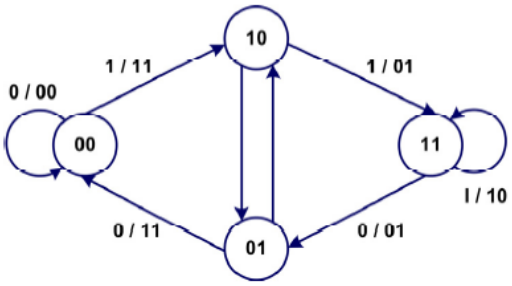

Fig 4. State Diagram

IV. VITERBI ALGORITHM

The Viterbi algorithm has been known as a maximum likelihood decoding algorithm for convolutional codes. Let us consider a simple example for illustrating the principle of Viterbi algorithm. Assume that a car that has 3 states *forward*, *stop* and *reverse* with the condition that a transition from *forward* to *reverse* is not allowed. In other words, it implies that the car first enter the *stop* state and then enter the *reverse* state. Hence, when we receive the information through the processes of *forward*, *reverse* and *stop*, we can safely interpret it as – *forward*, *stop* and *reverse* as this is a "maximum likelihood sequence".

The Viterbi algorithm uses the trellis diagram to compute the path metric value (accumulated distance) from the received sequence to the possible transmitted sequences. The total number of such trellis paths increases exponentially with the number of stages in the trellis. It causes potential complexity and memory problems. The Viterbi decoding algorithm has been classified into hard decision decoding and soft decision decoding.

If the received signal is converted into two levels, either zero or one, it is called hard decision. If the input signal is quantized and processed for more than two levels, it is called soft decision.

The soft decision decoding is expensive and require large amount of memory than hard decision decoding. Hence, this work focuses on the hard decision decoding. Figure 4 shows the trellis diagram for hard decision iterbi decoding.

When a sequence of data is received from the channel, it is desirable to estimate the original sequence that has been sent. The process of identifying such a sequence can be done using a diagram called '*trellis*', which is shown in fig. 4.

The detection of the original stream can be described as finding the most probable path through the trellis. In the trellis diagram each node specifies an individual state at a given time and indicates a possible pattern of recently received data bits. The transition to a new state at the next timing cycle is indicated by each branch.

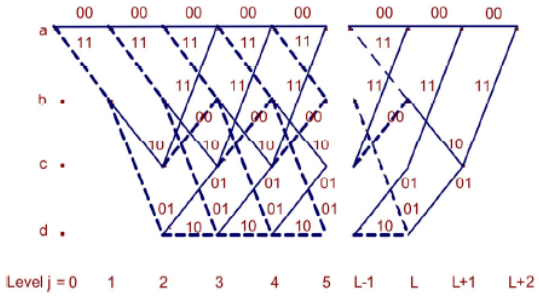

Fig 5. Hard decision Viterbi decoding trellis diagram

V. DECODING ALGORITHMS

VHDL is commonly used as a design-entry language for FPGA and application-specific integrated circuits in electronic design automation of digital circuits. VHDL comes from VHSIC hardware description language, where VHSIC stands for very-high-speed integrated circuit. The process starts with Register Transfer Level (RTL) coding which comprises of Behavioral description and Hardware Description Language (HDL). The convolutional encoder RTL design block diagram is illustrated as Fig. 4. There are three main blocks in the convolutional encoder design. The CONVOLUTIONAL (2, 1, 3) block encodes the IN_BIT (one binary bit) at each clock when the START is HIGH. The outputs of the block are C0 and C1 (both are one binary bit). The 2-BIT MULTIPLEXER block is functioning as a 2-bit parallel-to-serial converter. The encoded codeword is the serial binary data stream and then shows with the LED available on the FPGA board through the DISPLAY_LED block.

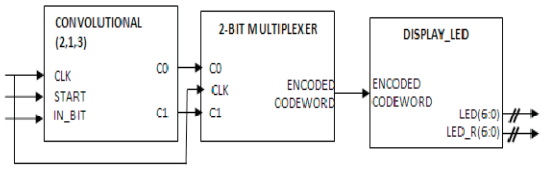

Fig 6.RTL Schematic-Encoder

The process of adaptive Viterbi decoder (AVD) starts with RTL VHDL coding which comprises of Behavioral description and HDL. The CONTROL block which combines all the subcomponents of AVD RTL design block diagram is illustrated as Figure 9. There are five main blocks in the AVD design which are BMU, ACSU, PMU, SPU & TBU, DU and COUNTER. The CONTROL block is having four input ports including the CLK, START, RESET and MODE of 1 bit standard logic(STD_LOGIC).

The CLK is the signal for the synchronization of the circuits. START is a button to enable the decoding process. RESET button reassign all the registers value in the design to initial values.

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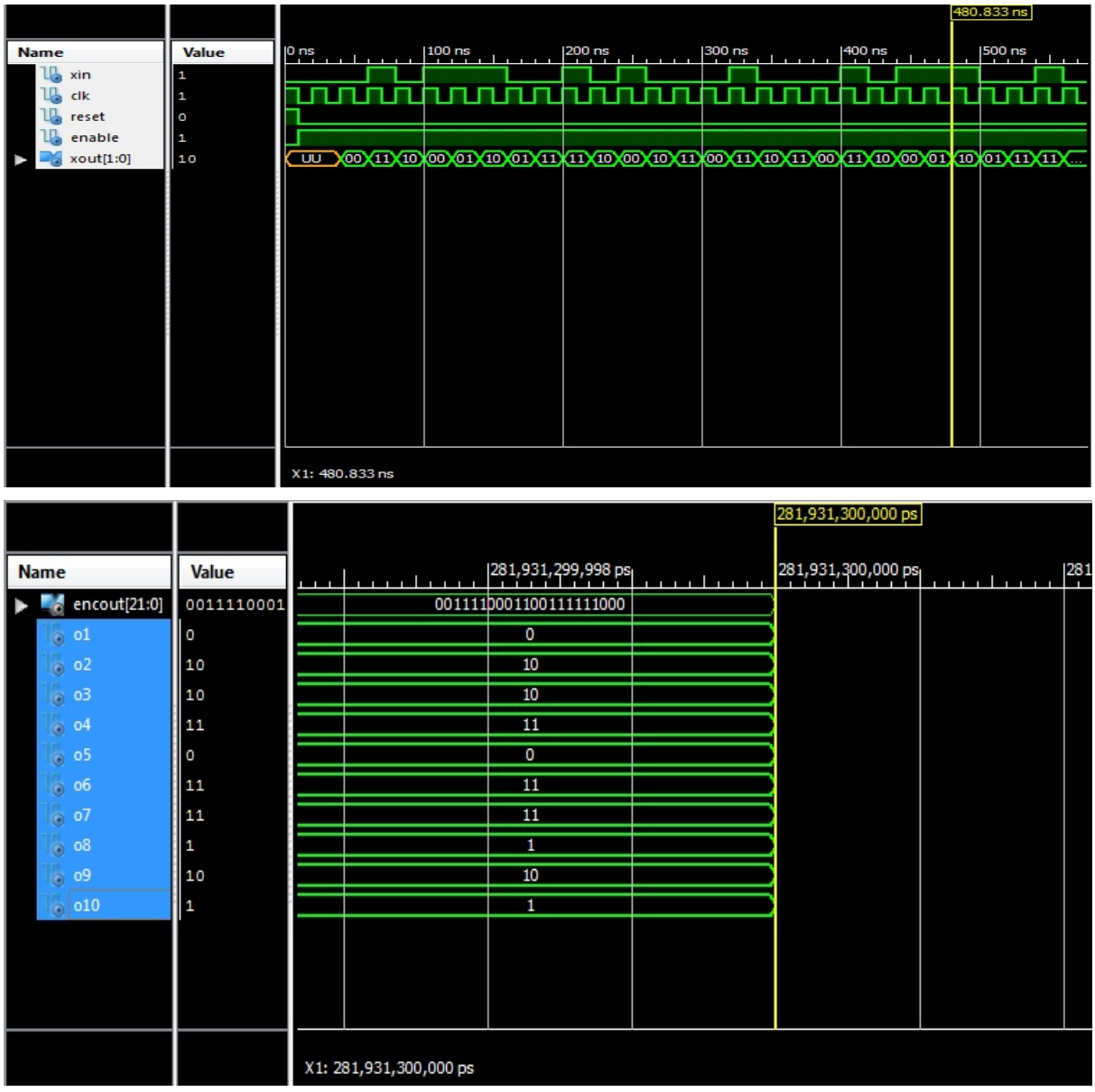

Fig.7 Simulation Results for Encoder and Decoder

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MODE indicates the adaptive trace back length (TL) for decoding process. There is one two bits standard logic vector (STD_LOGIC_VECTOR) input port for the PARALLEL_2BIT_C. It is the parallel 2 bits received codeword from the decoder. There is two 7 bits STD_LOGIC_VECTOR for two 7-segment-LED displays on the FPGA board.

There is also 17 bits

STD_LOGIC_VECTOR which connected to the expansion connector pins for external LED displays. Besides that, four one bit STD_LOGIC output port are included in the CONTROL architecture.

B1 and B0 are the received codeword which has the same value as PARALLEL_2BIT_C. B1 and B0 are connected to the expansion connection pins for external 7-segment LED displays. CLK_OUT and MO are assigned to the Bar graph LED. The logic '0' indicates it is a TL of 4 decoding mode, on the other hand, logic '1' for TL of 15.

VI. RESULTS

The Convolutional encoder for the constraint length of K=9 and code rate of r=1/2 has been developed and the synthesis is carried out. It has been simulated and the simulation result is shown in fig. 7.The Viterbi decoder has been developed using and the synthesis is carried out.

It (decoder) has been simulated and the simulation result is shown in fig. 8.

Typical input and output are as indicated below.

Input bits X=[010111001010001]

Output bits Y=[00 11 10 00 01 10 01 11 11 10 00 10 11 00 11]

Encoded noise =[00 11 11 00 01 10 01 11 11 10 10 10 11 00 11]

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REFERENCES:

[1] C. E. Shannon, "A mathematical theory of communication," Bell Sys. Tech. J., vol. 27, pp. 379–423 and 623–656, 1948.

[2] R. W. Hamming, "Error detecting and correcting codes," Bell Sys. Tech. J., vol. 29, pp. 147–160, 1950.

[3] Irfan Habib, Özgün Paker, Sergei Sawitzki, "Design Space Exploration of Hard-Decision Viterbi Decoding: Algorithm and VLSI Implementation" IEEE Tran. on Very Large Scale Integration (VLSI) Systems, Vol. 18, Pp. 794-807, May 2010.

[4] Hema.S, Suresh Babu.V and Ramesh.P, "FPGA Implementation of Viterbi decoder" proceedings of the 6th WSEAS ICEHWOC, Feb. 2007.

[5] D. E. Muller, "Application of boolean algebra to switching circuit design," IEEE Trans. on Computers, vol. 3, pp. 6–12, Sept. 1954.

[6] J. Wesdock, and C. Patel, "Formulation of modulation recommendations for future nasa space communications," in IEEE Aerospace Conference, Big Sky, Montana, March 2008.

[7] A. J. Viterbi, "Error Bounds for Convolutional Codes and an Asymptotically Optimum Decoding Algorithm," IEEE Trans. on Information Theory, Vol. IT-13, pp. 260-269, April 1967.

[8] M. Kivioja, J. Isoaho and L.Vanska, "Design and implementation of Viterbi decoder with FPGAs," Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology, Kluwer Academic Publishers, vol. 21, no. 1, pp. 5-14, May 1999.

[9] W. Chen, "RTL Implementation of Viterbi Decoder," Linkoping University, Department of Electrical Engineering, June 2006.

[10] E. R. Berlekamp, R. E. Peile, and S. P. Pope, "The application of error control to communications," IEEE Commun. Magazine, vol. 25, pp. 44– 57, Apr. 1987.

[11] M. Kling, "Channel Coding Application for CDMA2000 implemented in a FPGA with a Soft processor Core," Linköping University, Department of Electrical Engineering, 2005.

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