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Asynchronous Model of Flip-Flop's and Latches for Low Power Clocking

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Abstract – There is a wide selection of flip-flops in the literature. Many contemporary microprocessors selectively use master-slave and pulsed-triggered flip-flops. Transmission gated flip-flop, are made up of two stages, one master and one slave. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. The concepts discussed in the related work are related to synchronous design's novel method for low power dissipation asynchronous methods have been improving so as to reduce the power consumption an asynchronous methods for flip-flops are being implemented.

Keywords - Flip-flops, latches, clocking, dual edge-triggered, low power, level conversion.

I. INTRODUCTION

The power distribution of VLSI's differs from product to product. However, it is interesting to note that a clock system and a logic part itself consume almost the same power in various chips, and the clock system consumes 20–45% of the total chip power. In this clock system power, 90% is consumed by the flip-flops themselves and the last branches of the clock distribution network which directly drives the flip-flops [1].

One of the reasons for this large power consumption of the clock system is that the transition probability of the clock is 100% while that of the ordinary logic is about one-third on average. Consequently, in order to achieve low-power designs, it is important to reduce the clock system power. In order to reduce the clock system power, it is effective to reduce a clock voltage swing. This is because the power consumption of the clock system is proportional either to the clock swing or to the square of the clock swing, depending on the circuit configuration, which is described later. One idea to reduce the clock voltage swing was pursued in [2], but it required four clock lines, which will increase clock interconnection capacitance. Moreover, routing four clock lines is disadvantageous in area, and the skew adjustment is difficult.

This paper describes a new small-swing clocking scheme which requires only one reduced swing clock line.

II. RELATED WORK

The hybrid-latch flip-flop (HLFF) and semi-dynamic flip-flop (SDFF) have been known as the fastest flipflops, but they consume large amounts of power due to redundant transitions at internal nodes. To reduce the redundant power consumption in internal nodes of high-performance flip-flops, conditional capture flip-flop (CCFF) has been proposed [4].

Reduced clock-swing flip-flop (RCSFF) is proposed to lower the voltage swing of the clock system. With the conventional flip-flop, the clock swing cannot be reduced because and are required, and overhead becomes imminent if two clock lines and are to be distributed. On the other hand, if only is distributed, most of the clock-related MOSFET's operate at full swing, and only minor power improvement is expected.

The RCSFF is composed of a true single-phase master-latch and a cross-coupled NAND slave-latch. The master-latch is a current-latch-type sense-amplifier. The salient feature of the RCSFF is that it can accept a reduced voltage swing due to the single-phase nature of the flip-flop.

The voltage swing, V_{sw} , can be as low as 1 V. While the MOSFET count of the conventional flip-flop is 24, that of the RCSFF is 20 including an inverter for generating \bar{C} . The number of MOSFET's that are related to a clock is also as small as 3, which should be compared to 12, in the conventional flip-flop. Since only three MOSFET's, M_{N1} , M_{N2} , and M_{N6} , are clocked, the capacitance of a clock network can be reduced with the RCSFF, which in turn decreases the power.

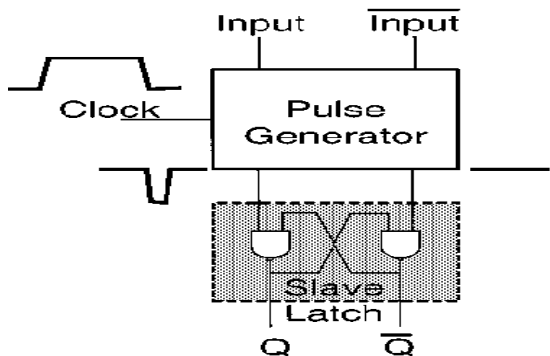


Fig 1. Flip Flop Structure

The conditional capture technique, however, needs many additional transistors for certain flip-flops such as SDFF, which tends to offset the power saving. To overcome the problems of conventional flip-flops, we propose a new low-swing clock double-edge flip-flop. A schematic diagram of our low-swing clock double-edge triggered flip-flop(LSDFF).It is composed of a data sampling front-end ($P1, N1, N3-N6, 11-14$) and a data transferring back-end ($P2, N2, 19, 110$). Internal nodes X and Y are charged and discharged according to the input data, D, not by the clock signal. Therefore, internal nodes of LSDFF switch only when the input changes and inherently do not need a conditional capture mechanism similar to that in pulse-triggered TSPC flipflop (PTTF). In PTTF, either one of data-precharged internal nodes is in floating state, which may cause mal- function of the flip-flop.

Also its internal node does not have a full voltage swing, thus causing performance degradation.

Also, in LSDFF, unlike SDFF, one inverter along with one transistor prevent nodes X, Y from floating without fighting the intended current flow, thus reducing the latency and power consumption. No stacking of transistors at the back-end of SDFF further reduces the latency.

Like HLFF, SDFF, and CCFF, a back-to-back-inverter type driver at the output node is used for robust operation.

Furthermore, HLFF, SDFF, and CCFF use full-swing clock signals, which causes significant power consumption in the clock tree.

III. DESIGNING ISSUES

A mechanism illustrating flip-flop operation is shown in Fig. 1. It is also essential to distinguish it from the master–slave (MS) latch combination consisting of two cascaded latches. MS latch pair can potentially be transparent if sufficient margin between the two clocking phases is not assured. In general, a flip-flop consists of two blocks: a pulse generator (PG) and a slave latch (SL), similar to the MS latch combination consisting of master and slave latches. In the flip-flop structure, the first stage (PG) is a function of the clock and data signals. Therefore, as a result of changes in clock and data values a pulse of a sufficient duration is produced. This pulse in turn sets the slave latch. Depending on a particular realization, the PG stage is sensitive to the transition of the clock (from low-to-high, or high-to-low) and not to its level (as is the case with MS combination). This sensitivity in the implementation of the PG stage may pose a danger under certain conditions in terms of reliability and robustness of operation. Thus, the use of flip-flops has been prohibited in some design methodologies such as IBM's LSSD.

The SAFF consists of the SA in the first stage and the slave set-reset (SR) latch in the second stage as shown in Fig. 2, [7]. Thus SAFF is a flip-flop where the SA stage provides a negative pulse on one of the inputs to the slave latch: or (but not both), depending whether the output is to be set or reset. The pulse-generating stage of this flip-flop is the SA described in [5], [6]. It senses the true and complementary differential inputs.

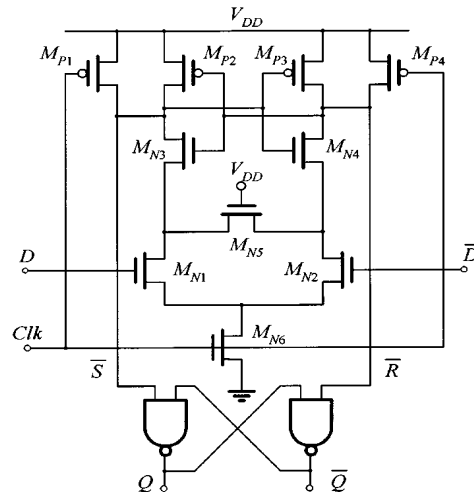


Fig 2. SAFF

The SA stage produces monotonic transitions from one to zero logic level on one of the outputs, following the leading clock edge. Any subsequent change of the data during the active clock interval will not affect the output of the SA. The SR latch captures the transition and holds the state until the next leading edge of the clock arrives. After the clock returns to inactive state, both outputs of the SA stage assume logic one value. Therefore, the whole structure acts as a flip-flop.

IV. PROPOSED CLOCKED-PAIR-SHARED IMPLICIT PULSED FLIP FLOP

CDFE and CCFF use many clocked transistors. CDMFF reduces the number of clocked transistors but it has redundant clocking as well as a floating node. To ensure efficient and robust implementation of low power sequential element, we propose Clocked Pair Shared flip-flop (CPSFF, Fig. 2) to use less clocked transistor than CDMFF and to overcome the floating problem in CDMFF.

In the clocked-pair-shared flip-flop, clocked pair (N3, N4) is shared by first and second stage. An always on pMOS, P1, is used to charge the internal node x rather than using the two clocked precharging transistors (P1, P2) in CDMFF. Comparing with CDMFF, a total of three clocked transistors are reduced, such that the clock load seen by the clock driver is decreased, resulting in an efficient design. Further the transistor N7 in the clocked inverter in CDMFF is removed. CPSFF uses four clocked transistors rather than seven clocked transistors in CDMFF, resulting in approximately 40% reduction in number of clocked transistors.

Furthermore the internal node X is connected to Vdd by an always on P1, so X is not floating, resulting in enhancement of noise robustness of nodeX. This solves the floating point problem in CDMFF. The always ON P1 is a weak pMOS transistor (length $X = \lambda$). This scheme combines pseudo nMOS. When input D stays 1, $Q=1$, N5 is on, N1 will shut off to avoid the redundant switching activity at node X as well as any short circuit current. pMOS P2 should pull Q up when D transits to 1 and so on. Several low power techniques in Section II can be easily incorporated into the new flip-flop. Unlike CDMFF, low swing is possible for CPSFF since incoming low voltage clock does not drive pMOS transistors. Low swing voltage clock signals could be connected to the nMOS transistors N3 and N4, respectively. In addition, it is easy to build double edge triggering flip-flop based on the simple clocking structure in CPSFF. Further CPSFF could be used as a level converter flip-flop automatically, because incoming clock and data signals only drive nMOS transistors.

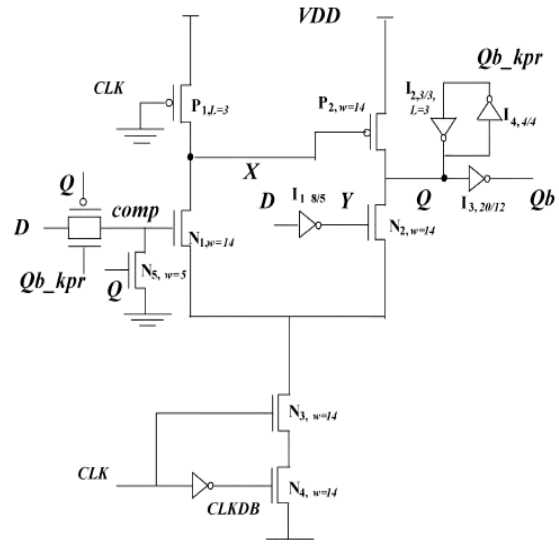


Fig . 2 Clock pair shared FF

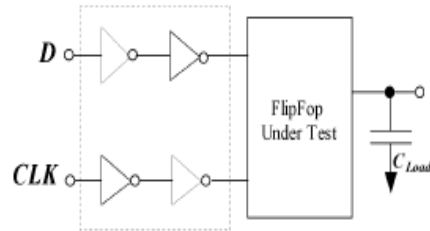


Fig 3. FF simulation Setup

It is desirable to have less clocked load in the system. CDFE and CCFF in Section II both have many clocked transistors.

For example, CCFF used 14 clocked transistors, and CDFE used 15 clocked transistors. In contrast, conditional data mapping flip-flop (CDMFF, Fig. 1) [9] used only seven clocked transistors, resulting in about 50% reduction in the number of clocked transistors, hence CDMFF used less power than CCFF and CDFE. This shows the effectiveness of reducing clocked transistor numbers to achieve low power. Since CDMFF outperforms CCFF and CDFE in view of power consumption, we do not discuss CCFF or CDFE further in this paper.

V. SIMULATION RESULTS

An Asynchronous mode Flip Flop is designed and it has an inverter is placed after output Q, providing protection from direct noise coupling [6]. The value of the capacitance load at node Q_b is 21 fF, which is

selected to simulate a fan out of 14 minimum sized inverters (FO14) [2].

Assuming uniform data distribution, we have supplied input D with 16-cycle pseudorandom input data with an activity factor of 18.75% to reflect the average power consumption.

The parasitic capacitances were extracted from the layouts. The setup used in our simulations is shown in Fig. 2. In order to obtain accurate results, we have simulated the circuits in a real environment, where the flip-flop inputs (clock, data) are driven by the input buffers, and the output is required to drive an output

load. A clock frequency of 250 MHz is used. Each design is simulated using the circuit at the layout level.

All capacitances were extracted from layout such that we can simulate the circuit more accurately. This is because the internal gate capacitance, parasitic capacitance, and wiring capacitance affect the power consumption heavily in deep sub micrometer technology. Further the delay strongly depends on these capacitors. The D-to-Q delay is obtained by sweeping the 0 -> 1 and 1->0 data transition times with respect to the clock edge and the minimum data-to-output delay corresponding to optimum set up time is recorded.

Flip-flop	New SAFF	Sdff	HLFF	TG M-S	C ² MOS	NAND-based SAFF
Total gate width [μm]	64	49	54	52	80	60

Fig 4. Total transistor gate width as a measure of size of compared flip-flops

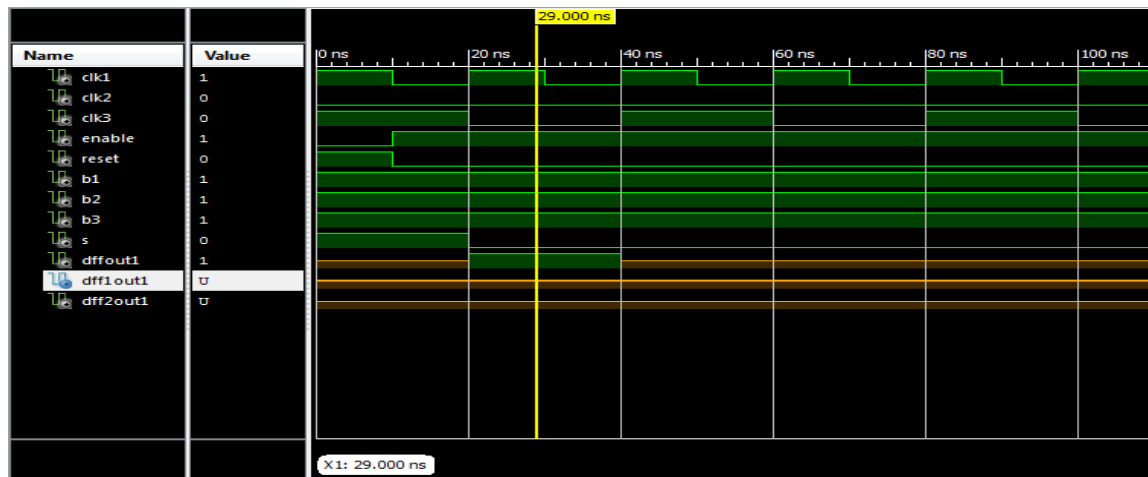


Fig 5. Simulation Results.

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