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AREA REDUCTION TECHNIQUES FOR PARALLEL FIR FILTER WITH SYMMETRIC COEFFICIENTS.

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Abstract-The objective of the paper is to reduce the hardware complexity of higher order FIR filter with symmetric coefficients. The aim is to design efficient Fast Finite-Impulse Response (FIR) Algorithms (FFAs) for parallel FIR filter structure with the constraint that the filter tap must be a multiple of 2. The parallel FIR filter structure based on proposed FFA technique has been implemented based on carry save and ripple carry adder for further optimization. The reduction in silicon area complexity is achieved by eliminating the bulky multiplier with an adder namely ripple carry and carry save adder. For example, for a 6-parallel 1024-tap filter, the proposed structure saves 14 multipliers at the expense of 10 adders, whereas for a six-parallel 512-tap filter, the proposed structure saves 108 multipliers at the expense of 10 adders. Overall, the proposed parallel FIR structures can lead to significant hardware savings for symmetric coefficients from the existing FFA parallel FIR filter, especially when the length of the filter is very large.
General Terms- Ripple Carry Adder (RCA), Carry Save Adder (CAS), Multiple Input Multiple Output (MIMO).

Keywords-*Digital Signal Processing (DSP), Fast Finite Impulse Response (FIR) Algorithms (FFA), Parallel FIR, Very Large Scale Integration (VLSI).*

1. INTRODUCTION

Finite Impulse Response (FIR) filter is one of the fundamental processing elements in many digital signal processing (DSP) system. Ranging from wireless communication to video and Image Processing. FIR filter must be operate at high frequency. In MIMO (Multiple Input Multiple Output) systems request high throughput FIR filter. Parallel processing is a well known technique for finite impulse response (FIR) digital filters, which increases the throughput, and decreases the power consumption by lowering the supply voltage .However due to its linear increase in the hardware implementation cost brought by the increase of block size "L". The Parallel Processing technique lost its advantage to be employed in practice therefore it has become a research topic to reduce the complexity of parallel FIR filter in last decades .In many design situation, hardware overhead that is incurred by parallel processing cannot be tolerated due to limitation in design area therefore it is advantageous to realize parallel FIR filtering structure that consume less area than traditional parallel FIR filtering structure.

The Proposed FFA structure successfully overcomes the constraint that the hardware implementation cost of a parallel FIR filter has a linear increase with block size L. Fast FIR algorithms (FFAs) introduced use approximately (2L-1) sub-filter blocks to implement a L-parallel filter, each sub-filter has length N/L. Area complexity is optimized by reducing bulky multipliers from (2N - N/L) to L x N using the FFA technique.

The Iterated Short Convolution (ISC) based linear convolution structure is transposed to obtain a new hardware efficient FFA filter structure which saves a large amount of hardware cost, especially when the length of the FIR filter is large .Small-sized filtering structures are constructed based on fast linear convolution, and then long convolution is decomposed into several short convolutions, i.e., larger block-sized filtering structures can be constructed through iterations of the small-sized filtering structures.

However, in both categories, symmetry of coefficients in the filter design has not been taken into consideration for the design of structures yet. This can lead to significant savings in hardware complexity and cost. In this paper, we provide a new parallel FIR filter structure based on FFA consisting of advantageous polyphase decompositions, which can reduce amounts of bulky multiplications in the sub-filter section by exploiting the inherent nature of the symmetric coefficients compared to the existing FFA fast parallel FIR filter structure.

2. FAST FIR ALGORITHM (FFA)

In general the output of an n-tap FIR filter which can be expressed as in (1)

(1)

where the input {x(n)} is an infinite-length input sequence of the length N FIR filter coefficients. Then, the traditional L- parallel FIR filter can be derived using polyphase decomposition as

$$Y(z) = X(z)H(z), \text{ i.e.,}$$

$$\sum_{p=0}^{L-1} Y_p(z^L) z^{-p} = \left(\sum_{q=0}^{L-1} x_Q(z^L) z^{-q} \right) \times \left(\sum_{r=0}^{L-1} H_r(z^L) z^{-r} \right), \quad (2)$$

where

$$x_q = \sum_{k=0}^{\infty} z^{-k} x(Lk+q),$$

$$H_r = \sum_{k=0}^{\left(\frac{N}{L}\right)-1} z^{-k} x(Lk+r),$$

$$Y_p = \sum_{k=0}^{\infty} z^{-k} x(Lk+p),$$

2.1 Traditional Parallel FIR Filter Structure

The Figure 1, shows the traditional parallel FIR filter structure

$$Y0=H0X0+Z^{-2}H1X1$$
$$Y1=H0X1+H1X0 \quad (3)$$

This equation gives the output of 2*2 traditional parallel FIR filter structure .This traditional filter requires four sub filter blocks of length N/2, 4 multiplier and 2 adders.

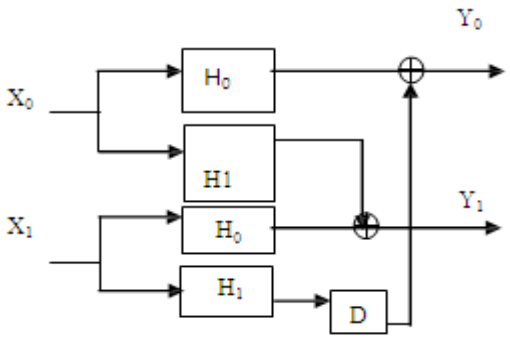


Figure 1:Traditional parallel FIR filter for L=2

2.2 FFA based FIR filter structure

2.2.1. Existing 2 x 2 FFA Technique (L = 2 parallel)

This Figure 2, shows the FFA based FIR filter structure

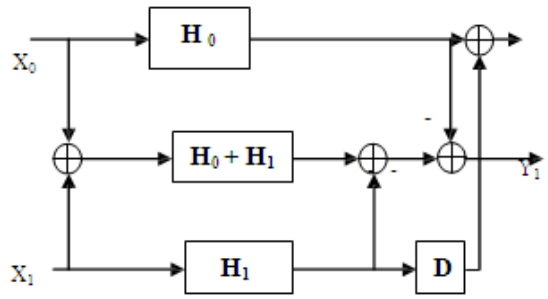


Figure 2:FFA Based FIR Filter for L=2

The output equation for this filter structure is

$$Y0=H0X0+Z^{-2}H1X1$$
$$Y1=(H0+H1)(X0+X1)- H0X0-H1X1 \quad (4)$$

The implementation of (4) will require three FIR sub-filter blocks of length N/2, one preprocessing and three post processing adders, and 3N/2 multipliers and + 4 adders, which reduces approximately one fourth over the traditional two-parallel filter hardware cost from (3). A two-parallel (L = 2) FIR filter implementation using FFA obtained from (4) is shown in Fig. 2. The 2-parallel filter can also be written in matrix form as

(5)

2.2.2. Existing 3 x 3 Fast FIR Algorithm (L = 3 parallel)

With reference to the three-parallel FIR filter using FFA can be expressed as [2]

$$Y_0 = H_0X_0 - z^{-3}H_2X_2 + z^{-3}[(H_1+H_2)(X_1+X_2) - H_1X_1],$$
$$Y_1 = [(H_0+H_1)(X_0+X_1) - H_1X_1 - H_0X_0 - z^{-3}H_2X_2],$$

(6)

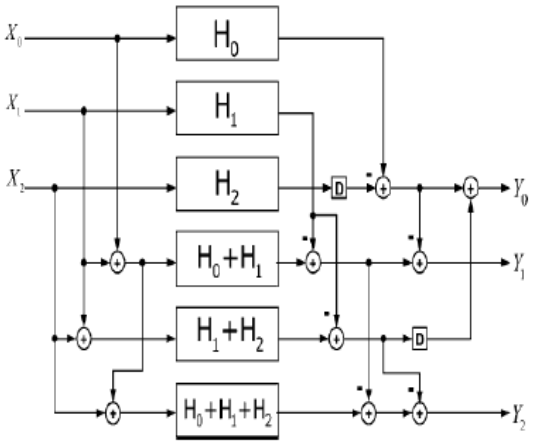


Figure 3: FFA Based FIR Filter for L=3

To utilize the symmetry of coefficients, the hardware implementation of (7) requires six length-N/3 FIR sub-filter blocks, three preprocessing and seven post processing adders, and three N multipliers and adders, which has reduced approximately one third over the traditional three-parallel filter hardware cost. The implementation obtained from (6) is shown in Fig. 3.The 3-parallel filter can be expressed in matrix form as

(7)

3. PROPOSED FFA STRUCTURES FOR SYMMETRIC CONVOLUTIONS

The main objective of the proposed structures is to earn as many sub-filter blocks as possible which contain symmetric coefficients so that half the number of multiplications in the single sub-filter block can be reused for the multiplications of whole taps, which is similar to the fact that a set of both odd and even symmetric coefficients would only require half the filter length of multiplications in a single FIR filter. Therefore, for an N-tap L-parallel FIR filter the total amount of saved multipliers would be the number of sub-filter blocks that contain symmetric coefficients times half the number of multiplications in a single sub-filter block (N/2L).

3.1 Proposed FFA for L=2 parallel FIR

From (3), a two-parallel FIR filter can also be written as

$$Y_0 = \left[\begin{array}{l}\left\{\frac{1}{2}\left[(H_0+H_1)(X_0+X_1)+(H_0-H_1)(X_0-X_1)\right]-H_1X_1\right\} \\ +z^{-2}H_1X_1\end{array}\right]$$

$$Y_1 = \frac{1}{2}\left[(H_0+H_1)(X_0+X_1)-(H_0-H_1)(X_0-X_1)\right]$$

(8)

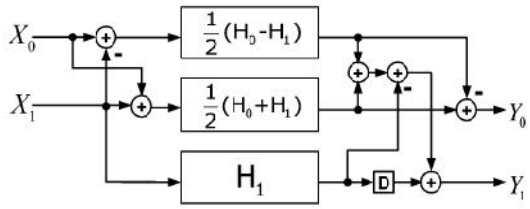


Figure 4: Proposed FIR filter for two-parallel implementation

When it comes to a set of even symmetric coefficients, (8) can earn one more sub-filter block containing symmetric coefficients than (6), the existing FFA parallel FIR filter. Fig. 4 shows the implementation of the proposed two-parallel FIR filter based on (8). An example is demonstrated here for a clearer perspective.

Example: Consider a 24-tap FIR filter with a set of symmetric coefficients applying to the proposed two-parallel FIR filter

{h(0), h(1), h(2),h(3), h(4), h(5)….
h(6), h(7), h(8), h(9), …, h(23)}

where h (23) = h(0), h(22) = h(1), h(21) = h(2), h(3) = h(20), h(4) = h(19), h(5) = h(18),….h(11) = h(12), applying to the proposed two-parallel FIR filter structure, and the top two sub-filter blocks will be given as

$$H_0 \pm H_1 = \{h(0)\pm h(1), h(2)\pm h(3),$$
$$h(4)\pm h(5), h(6)\pm h(7), \ldots, h(18)\pm h(19),$$
$$h(20)\pm h(21), h(22)\pm h(23)\}$$

where

$$h(0)\pm h(1) = \pm(h(38)\pm h(39))$$
$$h(2)\pm h(3) = \pm(h(36)\pm h(37))$$
$$h(4)\pm h(5) = \pm(h(34)\pm h(35))$$
$$h(6)\pm h(7) = \pm(h(16)\pm h(17))\ldots..$$

(9)

As observed from the above example, two of three sub-filter blocks from the proposed two-parallel FIR filter structures, H0-H1 and H0 + H1, are with symmetric coefficients, now, as (8), which means the sub-filter block can be realized by Fig. 4, with only half the amount of multipliers required. Each output of multipliers responds to two taps. Note that the transposed direct-form FIR filter is employed. Compared to the existing FFA two-parallel FIR filter structure, the proposed FFA structure leads to one more sub-filter block which contains symmetric coefficients. However, it comes with the price of the increase of amount of adders in preprocessing and post processing blocks. In this case, two additional adders are required for L = 2.

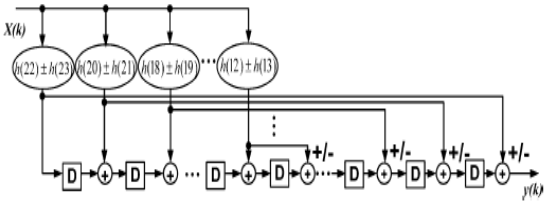


Figure 5:Subfilter block implementation with stmmetric coefficients

3.2. 3 x 3 Proposed FIR structure using FFA (L=3)

With the similar approach, from (8), a three-parallel FIR filter can also be written as (10). Fig. 6 shows implementation of the proposed three-parallel FIR filter. When the number of symmetric coefficients N is the multiple of 3, the proposed three-parallel FIR filter structure enables four sub-filter blocks with symmetric coefficients in total, whereas the existing FFA parallel FIR filter structure has only two ones out of six sub-filter blocks. Therefore, for an N-tap three-parallel FIR filter, the proposed structure can save N/3 multipliers from the existing FFA structure. However, again, the proposed three-parallel FIR structures also bring an overhead of seven additional adders in preprocessing and post processing blocks.

$$Y_0 = \left[\begin{array}{l}\left\{\frac{1}{2}\left[(H_0+H_1)(X_0+X_1)\right]+(H_0-H_1)(X_0-X_1)-H_1X_1\right\} \\ +z^{-3}\left\{\begin{array}{l}(H_0+H_1+H_2)(X_0+X_1+X_2)-(H_0+H_2)(X_0+X_2) \\ -\frac{1}{2}\left[(H_0+H_1)(X_0+X_1)-(H_0-H_1)(X_0-X_1)\right]-H_1X_1\end{array}\right\}\end{array}\right]$$

$$Y_1 = \left[\begin{array}{l}\left\{\frac{1}{2}\left[(H_0+H_1)(X_0+X_1)\right]+(H_0-H_1)(X_0-X_1)\right\} \\ +z^{-3}\left\{\begin{array}{l}\frac{1}{2}(H_0+H_2)(X_0+X_2)+(H_0-H_2)(X_0-X_2) \\ -\frac{1}{2}\left[(H_0+H_1)(X_0+X_1)+(H_0-H_1)(X_0-X_1)\right]+H_1X_1\end{array}\right\}\end{array}\right]$$

$$Y_2 = \frac{1}{2}\left[(H_0+H_2)(X_0+X_2)-(H_0-H_2)(X_0-X_2)+H_1X_1\right]$$

(10)

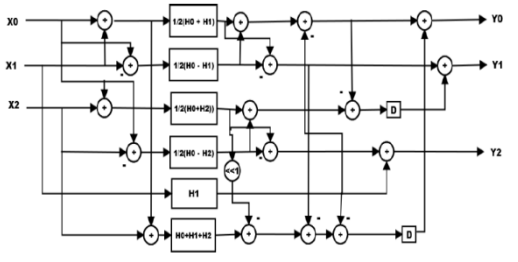
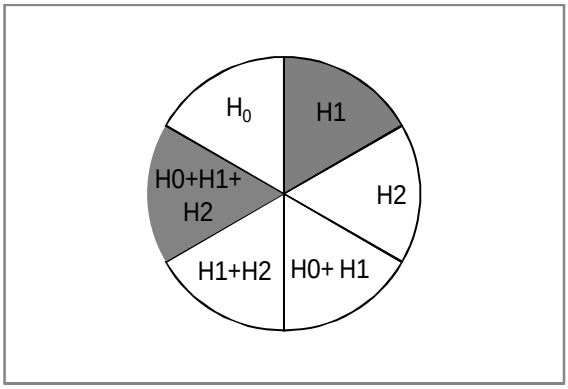
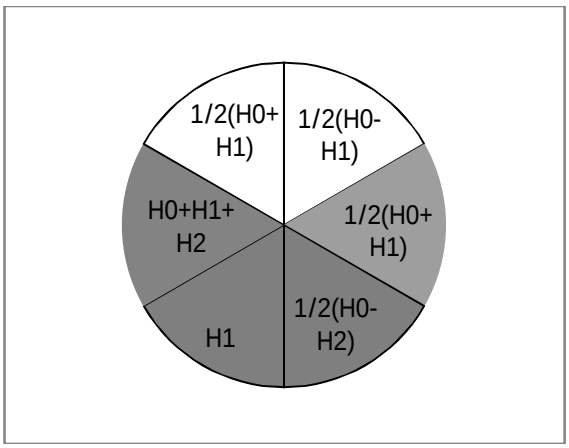


Figure 6:Proposed three –parallel FIR filter implementation



Existing FFA



Proposed FFA

Figure. 7: Comparison of sub-filter blocks between existing FFA and the proposed FFAthree-parallel FIR structures

4. COMPARISON

TABLE 1:Comparison of proposed and existing FFA structures with number of required multipliers, reduced multiplier, number of required adders in sub-filter section, number of required adders in pre-processing and post-processing blocks

i)For L = 2 Parallel FIR Filter:

Length		24-tap	36-tap	81-tap	512-tap	1024-tap
Multipliers	Existing FFA	36	54	122	768	1536
	Proposed FFA	30	45	102	640	1305
	Reduced	6	9	20	128	231
Adders (Pre/Post)	Existing FFA	4	4	4	4	4
	Proposed FFA	6	6	6	6	6
	Increased	2	2	2	2	2
Sub-Filters Block Adders		33	51	118	765	1533

ii)For L = 3 Parallel Filter:

Length		24-tap	36-tap	81-tap	512-tap	1024-tap
Multipliers	Existing FFA	48	72	162	1024	2048
	Proposed FFA	40	60	135	854	1707
	Reduced	8	12	27	170	341
Adders (Pre/Post)	Existing FFA	10	10	10	10	10
	Proposed FFA	17	17	17	17	17
	Increased	7	7	7	7	7
Sub-Filters Block Adders		42	66	156	507	2042

5. FPGA IMPLEMENTATION ANALYSIS

The existing and proposed FFA structures are implemented in Verilog HDL targeted on Xilinx VirtexE FPGA device of filter length of 12 and 27, word length of 8-bit. The comparison results are tabulated as

TABLE 2: Comparison of Area

Length	Structure	Area (Ripple Carry Adder Based)		Area (Carry Save Adder Based)	
		L=2	L=3	L=2	L=3
12-tap	Proposed FFA*	1080	1195	850	990
	Existing FFA	1290	1860	1150	1560
27-tap	Proposed FFA	920	1010	780	890
	Existing FFA	1090	1980	975	1690

* in terms of slices/LUT`s

TABLE III: Comparison of Delay

Length	Structure	Delay (ns) [Ripple Carry Adder)		Delay(ns) [Carry Save Adder]	
		L=2	L=3	L=2	L=3
12-tap	Proposed FFA	9.95	10.56	8.5	9.85
	Existing FFA	7.8	8.12	6.35	7.35
27-tap	Proposed FFA	10.65	11.45	9.45	10.65
	Existing FFA	8.4	9.4	6.4	8.5

6. CONCLUSIONS

The proposed efficient parallel FIR filter structures in this paper are advantages for symmetric convolutions or filter with symmetric coefficients. The Proposed parallel FFA technique is suitable for both even and odd number of tap which is a multiple of 2 or 3. Multiplier consumes the major area in the hardware for the parallel FIR implementation. The proposed structure extracts the nature of even symmetric coefficients and save a significant multiplier area at the expense of additional adder in pre-processing and post processing adder block in FIR filter. The Proposed structures is implemented using ripple carry and carry save adder, where the carry save based FFA technique reduces the hardware complexity by approximately by 10%. Since an adder occupies less area when compared to multipliers, it is advantageous to exchange multipliers with adders in terms of hardware cost. Moreover the number of increased adders stays still the same when the length of FIR filter becomes large, whereas the number of reduced multipliers increases along with the length of the filter. The larger the length of FIR filters is, the more the proposed structure and save form the existing FFA structure.

In this paper, we have proposed new parallel FIR structures for polyphase decompositions dealing with symmetric convolutions comparatively better than the existing FFA structure in terms of hardware consumption

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