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IMPLEMENTATION OF MULTITRACK SIMULATOR IN FPGA FOR ESM SYSTEM

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Abstract- This project PDW Simulator aims at developing a simulator which can be used to test the processor in the absence of Receiver hardware. This simulates the 128 bit PDW along with the required control signals which will be generated by the receiver card ESM Processor. The 128 bit PD Word is organized as four 32 bit words. Two address bits are used to indicate the word address. A strobe is to be provided to indicate the presence of each word. The simulator is being planned to be developed using Xilinx ISE 10.1 and the simulated results are to be demonstrated on Modelsim simulator or on Xilinx simulator itself.

Keywords- *ESM: Electronic System Measure, PDW: Pulse Description Word*

I. INTRODUCTION

ESM (Electronics Support Measure) systems intercept radar emissions which are within the operating frequency range of the system. ESM System consists of Antennas, Front End Receiver, Receiver subsystem, Processor subsystem and Display subsystem. Antennas intercepts the RF signals which are given to Front end receiver. The Front End Receiver gives amplified RF and detected video outputs. Amplified RF output is given to DIFM unit which measures the frequency. Video output of Front End Receiver is connected to the receiver subsystem.

The receiver sub systems measures the parameters such as Pulse width, Pulse repetition frequency and amplitude of the on pulse by pulse basis. It also time stamps the received signal by generating the Time Of Arrival (TOA) parameter. The measured frequency from DIFM Receiver is also routed to receiver subsystem. The above mentioned measured parameters are interleaved into 128 bit word called Pulse Descriptor Word (PDW).

II. BLOCK DIAGRAM

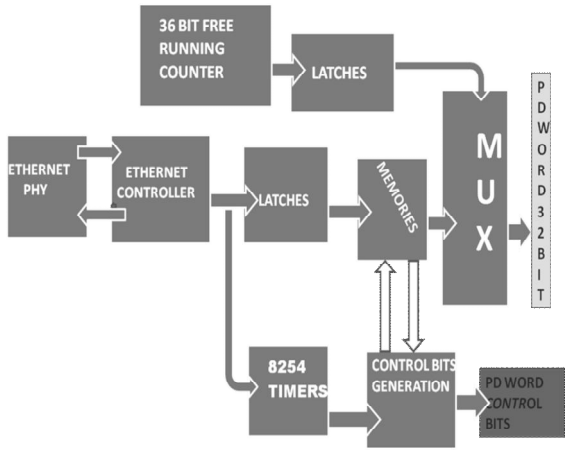

Figure.1 Block Diagram

A. INTRODUCTION TO ESM SYSTEMS

In military telecommunications, the terms Electronic Support (ES) or Electronic Support Measures (ESM) describe the division of electronic warfare involving actions taken under direct control of an operational commander to detect, intercept, identify, locate, record, and/or analyze sources of radiated electromagnetic energy for the purposes of immediate threat recognition (such as warning that fire control RADAR has locked on a combat vehicle, ship, or aircraft) or longer-term operational planning. Thus, Electronic Support provides a source of information required for decisions involving Electronic Protection (EP), Electronic Attack (EA), avoidance, targeting, and other tactical employment of forces. Electronic Support data can be used to produce Signals Intelligence (SIGINT), Communications Intelligence (COMINT) and Electronics Intelligence (ELINT).

Electronic support measures gather intelligence through passive "listening" to electromagnetic radiations of military interest. Electronic Support Measures can provide initial detection or knowledge of foreign systems, a library of technical and operational data on foreign systems, and tactical combat information utilizing that library. ESM collection platforms can remain electronically silent and detect and analyze RADAR transmissions beyond the RADAR detection range because of the greater power of the transmitted electromagnetic pulse with respect to a reflected echo of that pulse. United States airborne ESM receivers are designated in the AN/ALR series.

Desirable characteristics for electromagnetic surveillance and collection equipment include wide-spectrum or bandwidth capability because foreign frequencies are initially unknown, wide dynamic range because signal strength is initially unknown, narrow band pass to discriminate the signal of interest from other electromagnetic radiation on nearby

frequencies, and good angle-of arrival measurement for bearings to locate the transmitter. The frequency spectrum of interest ranges from 30 MHz to 50 GHz. Multiple receivers are typically required for surveillance of the entire spectrum, but tactical receivers may be functional within a specific signal strength threshold of a smaller frequency range.

B.8254 PROGRAMMABLE INTERVAL TIMER

- Compatible with All Intel and Most Other Microprocessors
- Handles Inputs from DC to 10 MHz
  - 8 MHz 8254
  - 10 MHz 8254-2
- Status Read-Back Command
- Six Programmable Counter Modes
- Three Independent 16-Bit Counters
- Binary or BCD Counter

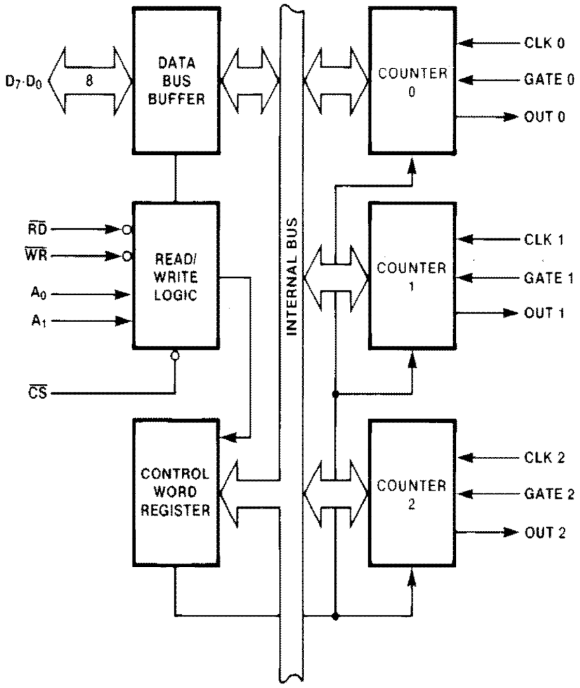

Figure2 8254 Block Diagram

The 8254 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software. The 8254 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 8254 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 8254 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

C.PROGRAMMING THE 8254 TIMER

Counters are programmed by writing a Control Word and then an initial count. The Control Words are written into the Control Word Register, which is selected when A_1, A_0 =11. The Control Word itself specifies which Counter is being programmed.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Figure3 Control Word Format

MODES OF 8254
MODE 0- Interrupt On Terminal Count
MODE 1- Programmable One Shot
MODE 2 -Rate Generator
MODE 3 -Square Wave Rate Generator
MODE 4 -Software Triggered Strobe
MODE 5- Hardware Triggered Strobe

Table 1. Modes Of 8254

COUNTER 0 CONTROL WORD								
0	0	1	1	0	1	1	0	=36H
COUNTER 1 CONTROL WORD								
0	1	0	1	0	1	0	0	=54H
COUNTER 2 COUNTER WORD								
1	0	1	1	0	1	1	0	=B6H

Table 2. Control Words Of Counters

D. PD CONTROL WORDS

In the real world scenario ESM system intercepts the RADAR signals that are emitted in its range and process its outputs for future purpose. But in the absence of the receiver's hardware to test the processor functioning we generate PD control bits and generate PD Words that gives information about Time Of Arriva(TOA), Direction Of Arrival(DOA),Pulse Width, Pulse Repetition Frequency, and Amplitude of the received signal.

For the system generated frequency between 1-2 GHz we use freq1 <= freq+5000-1951.

For the system generated frequency between 2-18 GHz we use freq1 <= (freq-1953).

DOA and Pulse Width are also calculated according to the received frequency.

III. IMPLEMENTATION

There is an increasing utilization of passive sensors in military target tracking. This paper describes a method of integrating Electronics Support Measure (ESM) and multitrack simulation trackers. The method can be generalized to address different types of ESM measurements data. In target environment where the availability of radar range measurement is severely reduced due to several possible factors including Electronics Support Measure (ESM) terrain screening, and the presence of low radars cross section targets, augmenting the radar tracking system with an ESM tracker provides an inexpensive but effective approach to improving track maintenance.
An ESM sensor is a passive sensor used to detect emission from platforms containing signals emitters such as ESM devices and acquisition radar. When ESM device is activated, the range measurement may become too degraded to achieve reason ally good tracking performance with a radar alone, as depicted by the diverging radar tracks. During this period , the ESM trackers can take over the task of updating tracks and provide containing in multitrack maintenance.

For the multitracker integration, we use the centralized approach to fusion where all the sensor measurements are sent to a central processing site to create maintain multitasks. One of the problems with this method is that low quality measurements from one sensor requirements by analyzing target ranging techniques. After that, we will briefly review the result used for ESM trackers and describe a tracker integration method. Computer simulation results will be described. To simplify the task, we do not consider how track ESM data association is performed the algorithms to detect ESM activation/deactivation emission mode changes and false alarms.

Let us review various multitrack simulation techniques. The most obvious one is multitrack simulation using radar measurements in which both range and frequency information are contained in a single report. If Angle Of Arrival(AOA) measurement are available from two or more spatially separated angle sensors, target location can be determined from the intersection of strobes. If ESM sensors are capable of measuring signal arrival times, then using the time difference of arrival (TDOA), target location can be determined. If a system consists of mixed sensors, i.e., AOA and TDOA , the location is determined by intersection of it.One of the problems in the passive ranging technique is asynchronous is measurement acquisition that spatially sensors may not be able to detect the same signal at the same time, and the time asynchrony will result in location estimate errors.

IV. SIMULATION RESULTS

The simulation software is Xilinx 12.1. And the selected device is Vertex 5 FPGA: XC5VLX330. The Simulation result in a Digital Clock Manager as shown in Figure 4.All global clock buffers can drive all clock regions in Virtex-5 devices by DCM. During simulation, the system clock frequency is set to 2-18 GHz and the clock period is set to 2micro -20milli seconds.

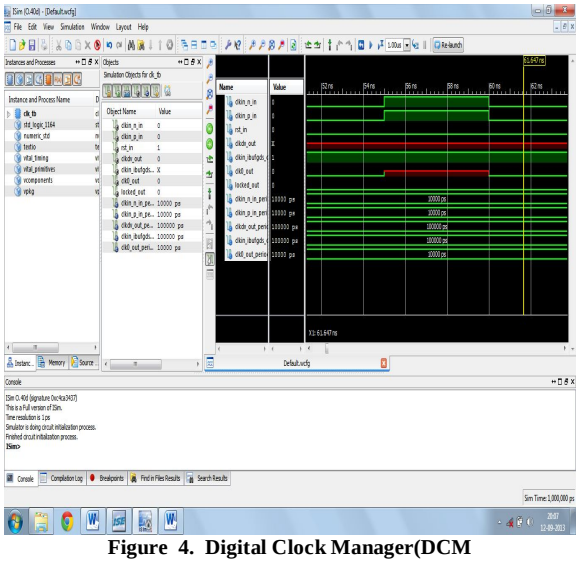

Figure 4. Digital Clock Manager(DCM

This counter is used to store the generated PD Words and the PD control bits Which is of 28 bits as shown in figure 5

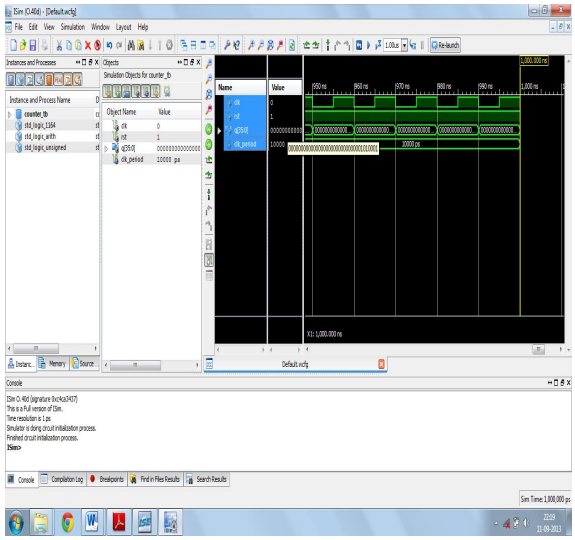

Figure 5 .36 Bit Free Running Counter

The Top module of Simulation result as shown in Figure 6.

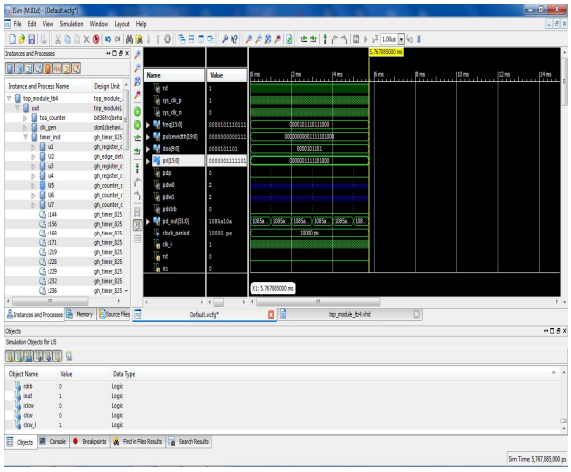

Figure 6.C.Top Module

V. CONCLUSION

This design uses VHDL as design language to achieve the modules of MULTITRACK SIMULATOR. Using Xilinx Software 12.1, Vertex 5 series FPGA chip XC5VLX330 to complete simulation and test. The results are stable and reliable. The design has great flexibility, high integration, with some reference value. Especially in the field of electronic design, where SOC technology has recently become increasingly nature, this design shows great significance.

VI. FUTURE WORK

The natural extension to this research is the best-track solution. We believe that by selecting the best solution among the outputs of different tracks of the received multitracks might improve the quality of result. But this also means there will be a huge synchronization effort which will decrease the speed up of the parallel implementation of the multi tracks. We plan to continue the simulation study by examining TDOA tracker integration and analysis , as well as examining performance with a one-site AOA ESM strobes and radar tracks are being developed.

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