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DECOUPLING LOGIC BASED SRAM DESIGN FOR POWER REDUCTION IN FUTURE MEMORIES

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DECOUPLING LOGIC BASED SRAM DESIGN FOR POWER REDUCTION IN FUTURE MEMORIES

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Abstract- In this paper we are going to modify the column decoupled SRAM for the purpose of more reduced leakages than the existing type of designs as well as the new design which is combined of virtual grounding with column decoupling logic is compared with the existing technologies & the nanometer technology is also improved for the purpose of much improved reduction of area & power factors the simulations were done using microwind & DSCH results

INTRODUCTION:

The main objective of this thesis is to provide new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, this work focuses on the reduction of the power dissipation, which is showing an ever-increasing growth with the scaling down of the technologies. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level.

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. Two components determine the power consumption in a CMOS circuit.

DEVICE miniaturization and the rapidly growing demand for mobile or power-aware systems have resulted in an urgent need to reduce power supply voltage (Vdd). However, voltage reduction along with device scaling is associated with decreasing signal charge. Furthermore, increasing intra-die process parameter variations, particularly random dopant threshold voltage variations can lead to large number of fails in extremely small channel area memory designs. Due to their small size and large numbers on chip, SRAM cells are adversely affected. This trend is expected to grow significantly as designs are scaled further with each technology generation [1].

Particularly, it conflicts with the need to maintain a high signal to noise ratio, or high noise margins, in SRAMs and is one of the major impediments to producing a stable cell at low voltage. When combined with other effects such as narrow width effects, soft error rate (SER), temperature, and process variations and parasitic transistor resistance, the scaling of SRAMs becomes increasingly difficult due to reduced margins [2]. Fig. 1 illustrates the saturation in the scaling trend (dashed line) of SRAM cells across technology generations. The plot indicates that the SRAM area scaling drops below 50% for 32-nm technology and beyond. Furthermore, voltage scaling is virtually nullified. Higher fail probabilities occur due to voltage scaling, and low voltage operation is becoming problematic as higher supply voltages are required to conquer these process variations.

To overcome these challenges, recent industry trends have leaned towards exploring larger cells and more exotic SRAM circuit styles in scaled technologies. Examples are the use of write-assist design [3], read-modify-write [4], read-assist designs [5], and the 8T register file cell. Conventional 6T used in conjunction with these techniques does not lead to power saving due to exposure to half select condition Column select/half-select is very commonly used in SRAMs to provide SER protection and to enable area efficient utilizationand wiring of the macro. Nevertheless, the use of column select introduces a read disturb condition for the unselected cells along a row (half-selected cells), potentially destabilizing them.
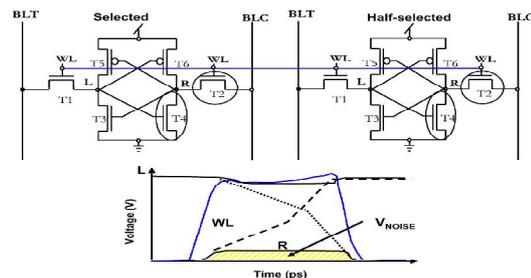

Fig1: Problem during operation in the SRAM's

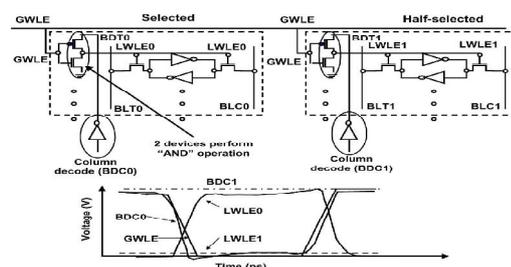Using 8T column decoupling logic design for this problem

Fig2: SRAM with column Decoupling Logic

Fig.2 illustrates a new 8T-CDC SRAM cell (inside dashed rectangle) with a gated wordline which enables the decoupling of the column/half-select condition [5] hence eliminating halfselect stability fails. A localized gated inverter consisting of two additional transistors, T1 and T2, effectively perform a logical "AND" operation between the column select signal (BDT0) and the decoded row, or global wordline, GWLE. The output of the inverter is the local wordline signal (LWLE0). The local wordline is ON only when both the column and row are selected (i.e., for fully selected cells only); hence, as illustrated in the waveforms of Fig. 3, LWLE0 of the selected columned turns ON while LWLE1 of the half-selected column remains low. This ensures that the local wordline for only the selected cells is activated, thereby effectively protecting the half-selected SRAM cells from the read disturb scenario that exists in 6T cell due to wordline sharing. Alternatively, it is possible to swap the input and supply pairs of the gated inverter; however this comes at the cost of extra delay stage and power. The advantages of the 8T-CDC cell are as follows: 1) conforming with traditional 6T requirements in terms of (a) allowing the designer to integrate it in a column select fashion and (b) offering/maintaining SER protection while 2) maximizing array efficiency, 3) eliminating the read disturb to the unselected cells, and 4) reducing power with simplification in peripheral logic.

The two extra devices are integrated on top of an existing 6T cell to allow for easy cell mirroring and integration into an array topology. The addition of the two new transistors results in a cell area increase of 40% (all in -direction). Through the use of higher level metallurgy to wire in the column decode (BDC) signal, the growth to the direction of cell was not impacted. The increase to the –dimension of the cell causes a proportionate increase to the BL metal capacitance while maintaining the original diffusion capacitance contributed by the 6T cell. Column decode signal integrated with higher level metal. Area penalty can be further reduced to 30% via use of 6T thin cell integration. Further reduction can be achieved by use of non-DRC clean devices. The area can be reduced further to 30% by utilizing thin cells as presented in this paper without degrading the bitline capacitance.

Concept of using Virtual Grounding
SRAM is an important part of modern microprocessor design, taking a large portion of the total chip area and power. Increasing the density of SRAM caches provides an effective method to enhance system performance. That has resulted in over 70% of the chip area being occupied by SRAM [1]. Scaling device size doubled the transistor count every two years according to Moore's law, and hence the density of SRAM caches kept mounting every

next generation. However device dimensions become too small in nano-scale technologies and are more prone to variations due to manufacturing process. These variations can disturb the read/write stability of a SRAM design causing reliability problems. A conventional 6T-SRAM has a poor read stability due to constraint design requirements, and can suffer functional failures due to high threshold voltage variations.

Statistical variability arising from the discreteness of charge and matter is a major source of threshold variation that degrades the reliability of conventional SRAM design [2].

Conventionally device sizing is used to enhance the read stability of SRAM cell design. However conventional sizing can be ineffective in nano-scaled technologies due to large threshold variations [3, 4]. Different SRAM designs have previously been presented that use from 6 to 10 transistors to provide reliable and/or low power operation. Sub-threshold (below 200 mV) [3] and low power [5] 6T-SRAM designs have been proposed, however the write speed for both is degraded due to single-sided read/write. A low power 6TSRAM design was presented in [6] that provided an improvement by 1/2 in access delay and reduced the write power by 1/10. However it did not improve noise margin and required a negative voltage during a read operation that degrades device reliability.

A 7T-SRAM design was presented for low voltage SNM free operation, but it suffered from dynamic retention [7]. Also the write margin decreased at lower voltage, and read operation could destroy cell data. Other designs used 8 or 10 transistors to increase robustness [8, 9]. However, they had a very high area overhead. For example, the 8T design incurred an area overhead of 30 %.

Design of 7T-SRAM for enhanced read stability
A conventional 6TSRAM cell design consists of a cross-coupled inverter pair (M3-M6) that does data storage and two access transistors (M1-M2) to load/retrieve data on bit lines, BL and BLB. During a write operation, the data is loaded on the bit lines and the word select signal WS is turned high. A successful write operation occurs if the data is correctly latched in the cell.

The bit lines are pre-charged to the supply voltage and the word select line is turned high to retrieve data during a read operation. The bit line (BL) connected to the storage node (V1) storing a '0' gets discharged. The storage node (V1) rises above '0' during a read operation due to voltage division between the access transistor (M1) and the driver transistor (M6). A read failure can occur if the voltage drop rises higher than the threshold voltage of the inverter (M3, M5).
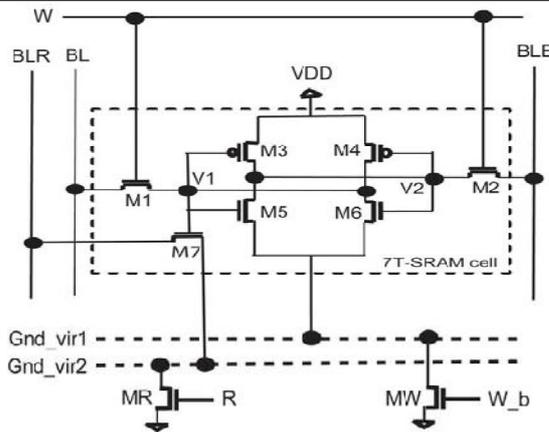
Fig 3: Virtual Grounding Based Read Error Reduced SRAM Cell

A conventional 6T-SRAM cell provides poor read stability since the access transistors provide direct access to the cell storage during a read operation. The proposed design (see Fig. 3) removes the access hazard during a read operation and therefore eliminates the chances of cell content being inadvertently flipped. It consists of a cross-coupled pair (M3-M6) for data storage as in case of a conventional 6T-SRAM cell. However the ground terminal of the inverter pair is connected to a virtual ground (Gnd_vir1) in the proposed design to provide high speed low-power write operation. The word select line 'WS' is held high only during a write operation to load new data in the cell by turning on the write access transistors (M1-M2). A read access transistor (M7) connected to a virtual ground (Gnd_vir2) is used to retrieve data on read bit line (BLR) during a read operation. Our design decouples read/write operation using separate read/write access transistors. Therefore it doesn't suffer from constrained read/write requirements as in 6T-SRAM design.

Proposed Design & results using Microwind & DSCH
Our idea is to combine these 8T SRAM that is shown in Fig:5 with virtual grounding concept shown in fig:6 to different technologies & to design a new circuit that is shown in fig:7 with much efficiency than the existing two designs. Thus we are designing a new circuit & showing the simulation results of the different technologies as shown below.

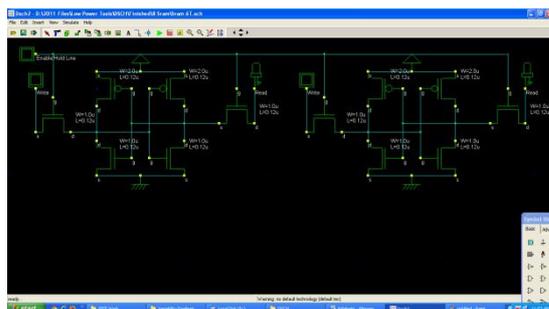**Fig: 4.1 Layout for Conventional 6T SRAM**
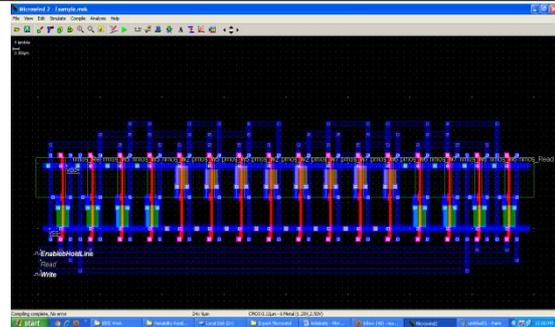

Fig: 4.2 Characteristic waveform for Conventional 6T SRAM

Fig: 5 8T SRAM Design
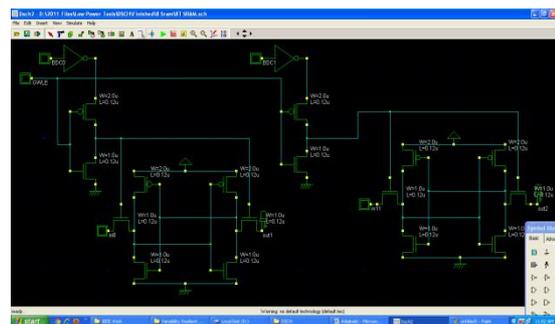

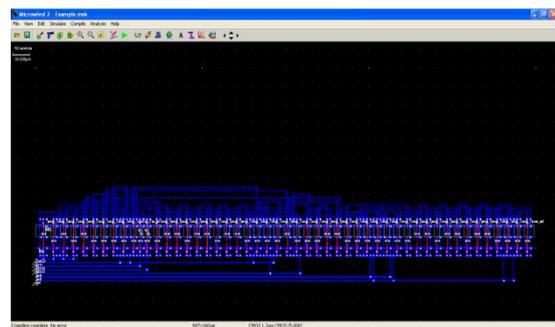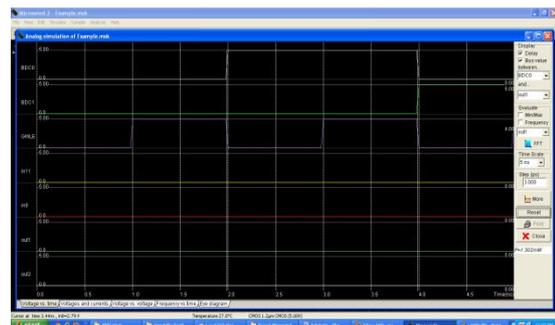**Fig : 5.1 8T SRAM layout**

Fig: 4 Conventional 6T SRAM

Fig: 5.2 Characteristic waveform for 8T SRAM

Fig: 6 Virtual Grounding Embedded SRAM

Fig: 7.1 Our Proposed layout combined with 8T & Virtual grounding concept

Fig: 6.1 Virtual Grounding Embedded SRAM layout

Fig: 7.2 Characteristic waveform for our proposed layout combined with 8T & Virtual grounding concept.

Fig: 6.2 Characteristic waveform for Virtual Grounding Embedded SRAM

Fig: 7 Our Proposed design combined with 8T & Virtual grounding concept

CONCLUSION

Our proposed design shows that much less power than the existing ones. 1.76uw at the standard Our Proposed layout combined with 8T & Virtual grounding concept 50nm technology. And it is having much reduced area than the conventional SRAM designs. Thus this design can be used for future SRAM core memories.

REFERENCE

[1] Kevin, Z., Embedded Memories for Nano-Scale VLSIs. 2009: Springer Publishing Company, Incorporated. 400.

[2] Brown, A.R., Roy, G., and Asenov, A., Poly-Si-Gate-Related Variability in Decananometer MOSFETs With Conventional Architecture. Electron Devices, IEEE Transactions on, 2007. 54(11): p. 3056-3063.

[3] Bo, Z., et al. A Sub-200mV 6T SRAM in 0.13um CMOS. in Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International. 2007.

[4] Cheng, B., Roy, S., Roy, G., Brown, A., and Asenov, A. Impact of Random Dopant Fluctuation on Bulk CMOS 6-T SRAM Scaling. in Solid-State Device Research Conference, 2006. ESSDERC 2006. Proceeding of the 36th European. 2006.

[5] Jawar Singh, D.K.P., Simon Hollis, and Saraju P. Mohanty, A single ended 6T SRAM cell design for ultra-low-voltage applications. IEICE Electronics Express, 2008. 5(18): p. 750-755.

[6] Mizuno, H. and T. Nagano, Driving source-line cell architecture for sub-1-V high-speed low-power applications. Solid-State Circuits, IEEE Journal of, 1996. 31(4): p. 552-557.

[7] Takeda, K., et al., A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications. Solid-State Circuits, IEEE Journal of, 2006. 41(1): p. 113-121.

[8] Chang, L., et al., An 8T-SRAM for Variability Tolerance and Low-Voltage Operation in High-Performance Caches. Solid-State Circuits, IEEE Journal of, 2008. 43(4): p. 956-963.

[9] Tae-Hyoung, K., et al. A High-Density Subthreshold SRAM with Data-Independent Bitline Leakage and Virtual Ground Replica Scheme. in Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International. 2007.

[10] Wang, X., Roy, S., and Asenov, A., Impact of Strain on the Performance of high-k/metal replacement gate MOSFETs, in Proc. 10th Ultimate Integration on Silicon (ULIS 2009). 2009.

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