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DESIGN OF A 500MHZ, 4-BIT LOW POWER ADC FOR UWB APPLICATION

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Abstract-This paper presents a new topology of an Analog-to-Digital Converter (ADC), named as Switched Reference ADC (SR-ADC) where the reference voltages are applied through switches. The switched reference voltage concept works with few mutually exclusive switches which are appropriately selecting the reference voltages for comparison with the input signal. This SR-ADC has been implemented using 0.18µm single poly and six metal CMOS technology. The spectra simulation result of this SR-ADC shows an ENOB of ≈3.53 for a 1V peak-to-peak input signal having a frequency of 100MHz while operating at a sampling frequency of 500MHz. The total power consumption is 21.39mW for a single power supply of 1.8V having a core area of ≈253µm*221µm.

Keywords-*UWB, SR-ADC, RFID, SAR ADC, DMN*

I. INTRODUCTION

Because of its ability to transmit information through short base-band pulses without employing a carrier, Ultra Wide Band (UWB) system becomes an useful option for low-power, low-cost radio. The Federal Communications Commission (FCC) has defined UWB in three bands: 0~960MHz, 3.1~10.6GHz and 24~29GHz [1]. The lower frequency band has got lot of preference because of longer transmit distance, lower power consumption and lower complexity of implementation, suitable for low data rate applications such as wireless sensor networks, RFID, etc. For an ADC to be used in low frequency band of UWB system, 4-bit resolution is sufficient [2]. The biggest challenge for the design of the ADC to be used in UWB system is to have a sampling speed ≥500MHz with low power dissipation.

The conventional ADCs designed using operational amplifiers consume more power [3]. Therefore, for low power ADC design, several techniques have been reported in the literature such as flash, pipelined, time interleaved Successive Approximation (SAR) etc. A low power, 4-bit and 400MHz Flash ADC reported in [4] uses common mode jump circuit to handle large input signals ($2V_{pp}$). However, the static and dynamic performances of this ADC are low due to the use of active load pre-amplifiers in comparators. SAR ADC consumes low power but operates at low speed. Higher speeds can be achieved using time interleaving. A dual scalable 5-bit time interleaved SAR ADC reported in [5] has a speed of 500MSPS and uses self timed logic to improve the latency of individual SAR ADC. However, the Effective Number Of Bits (ENOB) of this ADC is only 3. The 32mW, 1.25GS/s 6-bit and 2-bit/step SAR ADC proposed in [6] uses three Digital-to-Analog Converters (DAC) to detect 2-bits per clock cycle. But it occupies large capacitor area (52% of total core area) on chip.

In this paper, a completely new ADC architecture has been proposed. In this ADC, the reference voltages are applied discretely for comparison with the input signal through a number of mutually exclusive switches (only one switch will be in ON state at any time instant). The ON and OFF operations of these switches are controlled by a Decision Making Network (DMN) designed using digital logic circuits. This technique of using reference voltages helps in keeping the number of analog blocks fixed even if the resolution is increased. Only the switch count along with the reference voltages and the circuitry in the DMN to control the operation of the switches will increase with the resolution. As the DMN is implemented using digital logic circuits, the circuit complexity of the SR-ADC remains low in comparison to other architectures mentioned in [4], [5] and [6].

The subsequent sections of this paper have been arranged in the following manner. Section II describes the 4-bit SR-ADC architecture. Operation and circuit implementation are discussed in Section III. Results and discussion are given in Section IV. Finally, Section V concludes the paper.

II. ARCHITECTURE OF 4-BIT SR-ADC

The architecture of the 4-bit SR-ADC is shown in Fig. 1. In this ADC, feedback concept is used for processing the input signal to produce the binary output. As shown in Fig. 1, the reference voltages are applied through a number of switches. The operations of these switches are controlled by the feedback signal generated by the DMN. To increase the resolution of this SR-ADC there will be an increase in the ladder network for generating the reference voltages maintaining the number of other analog blocks fixed. As a result the power dissipation and the circuit complexity will still remain low. The front end of this SR-ADC consists of a differential amplifier.

One of the inputs (V_{in+}) to this differential amplifier is the analog input signal. The other input (V_{in-}) is connected to 16 reference voltages ($1V_r$ -$16V_r$) through mutually exclusive switches (S_1-S_{16}). All these switches are implemented using pass-transistors and controlled by the decision signals (V_{S1}-V_{S16}) generated by the DMN. The front end of the DMN consists of two latched comparators (MP_1 and MP_2). The output nodes X and Y of the differential amplifier are fed to the input port (V_{in}) of comparators MP_1 and MP_2 respectively. The second input (V_{ref}) of MP_1 is connected to a DC voltage (V_{R1}) which is equal to the output common mode voltage of the differential amplifier and the second input (V_{ref}) of MP_2 is connected to a DC voltage (V_{R2}) which is equal to the maximum voltage obtained at the output node (X) of the differential amplifier. The outputs of these two comparators are connected to a digital network which generates the decision signals to control the switches (S_1-S_{16}). The digital network is designed using AND/OR logic gates and D-FFs. Besides controlling the operation of switches (S_1-S_{16}), the outputs of the DMN (V_{S1}-V_{S16}) are also fed to an encoder which generates the SR-ADC outputs (B_0-B_3) in binary form corresponding to the input analog signal.

III. OPERATION AND CIRCUIT IMPLEMENTATION OF THE SR-ADC

With a view to explain the operation and circuit implementation lucidly, initially we have considered a 2-bit SR-ADC architecture, later the steps to be followed for 4-bit SR-ADC are explained.

The input analog signal to the 2-bit SR-ADC is a slow varying triangular waveform as shown in Fig. 2. The reason behind selecting this sort of signal is to have distinguishable transition points over the reference voltages ($1V_r$-$4V_r$) marked by time tokens (t_n). Fig. 3 demonstrates the front end differential amplifier of this 2-bit SR-ADC along with the switches (S_1-S_4) and reference voltages ($1V_r$-$4V_r$). The triangular input signal and the reference voltages ($1V_r$-$4V_r$) are applied at the input ports V_{in+} and V_{in-} of the differential amplifier respectively. The switches are implemented using pass transistors and controlled by the DMN. The common mode voltage at both the input ports V_{in+} and V_{in-} is set to $V_{in,cm}$. With only this common mode voltage at both the input ports, the output common mode voltage becomes $V_{o,cm}$.

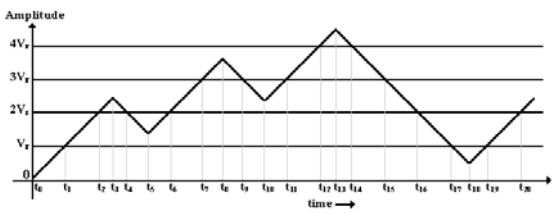

Figure 2. Input triangular waveform

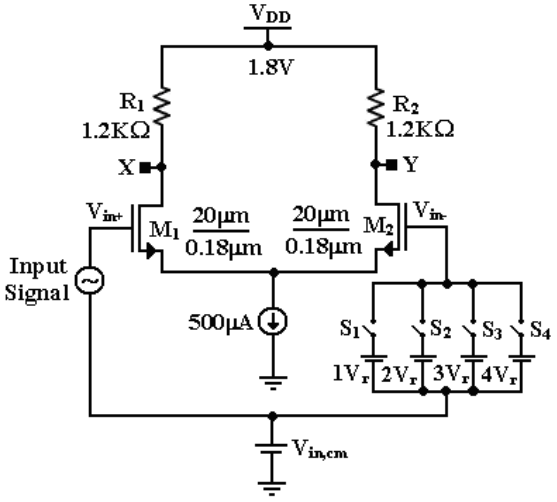

Figure 3. Front end differential amplifier of the 2-bit SR-ADC

At time t_0, the input signal is at zero, as shown in Fig. 2. With this value of the input signal, the voltage difference between the two input ports (V_{in-} and V_{in+}) is $1V_r$ [= ($V_{in,cm}$+$1V_r$)-$V_{in,cm}$]. This voltage difference at the two input ports sets differential output voltages of V_x and V_y ($V_x > V_y$) at ports X and Y respectively. The output characteristic of the differential amplifier at time t_0 is shown in Fig. 4.

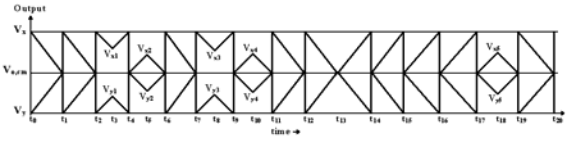

Figure 4. Output characteristic of the front end differential amplifier

As the input signal gradually rises at port V_{in+}, the output voltage (V_x) starts decreasing and the voltage (V_y) starts increasing. At time t_1, the input signal gets equal to the reference voltage $1V_r$. This brings both the output voltages (V_x and V_y) at ports X and Y to output common mode voltage $V_{o,cm}$. With a nominal increase in the input signal beyond reference voltage $1V_r$, the DMN brings the second switch (S_2) in the switching network to ON state. This changes the voltage at port V_{in-} from ($V_{in,cm}$+$1V_r$) to ($V_{in,cm}$+$2V_r$). This change in the reference voltage allows the output voltages at ports X and Y to transit from $V_{o,cm}$ to V_x and V_y instantaneously. With further increase in the input signal, the output voltage at port X gradually falls and the voltage at port Y raises slowly. At time t_2, the input signal gets equal to the reference voltage $2V_r$ making the voltage at port V_{in+} to ($V_{in,cm}$+$2V_r$). This once again brings the output voltages at ports X and Y to $V_{o,cm}$. When the input signal marginally exceeds the reference voltage of $2V_r$, the DMN brings the third switch (S_3) to ON state. This changes the reference voltage from ($V_{in,cm}$+$2V_r$) to ($V_{in,cm}$+$3V_r$) at the input port (V_{in-}) of the differential amplifier. This change in the reference voltage allows the output voltages at ports X and Y to transit from $V_{o,cm}$ to V_x and V_y respectively. As the input analog signal

increases beyond ($V_{in,cm}+2V_r$), the output voltage at port X starts falling and the voltage at port Y starts increasing. At time t_3, the input signal changes its direction and starts falling. This change in the input analog signal allows the output voltage at port X to increase and the output voltage at port Y to decrease. At time t_4, when the input signal moves just below $2V_r$, the DMN switches OFF S_3 and switches ON S_2 in the switching network. This changes the reference voltage from ($V_{incm}+3V_r$) to ($V_{in,cm}+2V_r$) at the input port V_{in-} of the differential amplifier. This change in the reference voltage allows the output voltages at ports X and Y to transit from V_x and V_y to $V_{o,cm}$. With further decrease in the input signal, the output voltage at X increases and at Y decreases. At time t_5, the input signal once again changes its direction and starts increasing. With this change in the input signal, the output voltage at X starts falling and at Y starts increasing. At time t_6, the input signal becomes equal to $2V_r$ bringing both the output voltages at X and Y to $V_{o,cm}$. As the input signal slightly exceeds the reference voltage $2V_r$, the DMN brings the switch S_3 to ON state. This changes the reference voltage from ($V_{in,cm}+2V_r$) to ($V_{in,cm}+3V_r$). This change in the reference voltage instantaneously allows the output voltages at ports X and Y to transit from $V_{o,cm}$ to V_x and V_y respectively. This process of voltage transitions at ports X and Y with respect to the input analog signal continues for rest of the time slots.

A. Implementation of the decision making network

At the beginning of the operation, assuming input analog voltage is less than $1V_r$, switch S_1 remains in ON state and the other switches (S_2, S_3 and S_4) present in the switching network are in OFF state. This means, the control signal V_{S1} is at logic '1' state while V_{S2}, V_{S3} and V_{S4} are at logic '0' state. With the transition of the voltage levels at the outputs of MP_1 and MP_2, the states of the control signals (V_{S1}-V_{S4}) change. All the possible state transitions of the control signals with the change in the logic levels at the outputs of MP_1 and MP_2 are given below;

a. V_{S1} = '1', $V_{S2} = V_{S3} = V_{S4}$ = '0'
Output of MP_1 = '0' → '1', Output of MP_2 = '0'
('0' → '1': transition of logic '0' to logic '1')
V_{S2} = '1', $V_{S1} = V_{S3} = V_{S4}$ = '0'

b. V_{S2} = '1', $V_{S1} = V_{S3} = V_{S4}$ = '0'
Output of MP_1 = '0', Output of MP_2 = '0' → '1'
V_{S1} = '1', $V_{S2} = V_{S3} = V_{S4}$ = '0'

c. V_{S2} = '1', $V_{S1} = V_{S3} = V_{S4}$ = '0'
Output of MP_1 = '0' → '1', Output of MP_2 = '0'
V_{S3}= '1', $V_{S1} = V_{S2} = V_{S4}$ = '0'

d. V_{S3} = '1', $V_{S1} = V_{S2} = V_{S4}$ = '0'
Output of MP_1 = '0', Output of MP_2 = '0' → '1'
V_{S2}= '1', $V_{S1} = V_{S3} = V_{S4}$ = '0'

e. V_{S3} = '1', $V_{S1} = V_{S2} = V_{S4}$ = '0'
Output of MP_1 = '0' → '1', Output of MP_2 = '0'
V_{S4}= '1', $V_{S1} = V_{S2} = V_{S3}$ = '0'

f. V_{S4} = '1', $V_{S1} = V_{S2} = V_{S3}$ = '0'
Output of MP_1 = '0', Output of MP_2 = '0' → '1'
V_{S3}= '1', $V_{S1} = V_{S2} = V_{S4}$ = '0'

Fig. 5 shows the variation of the control voltages V_{S1}, V_{S2}, V_{S3} and V_{S4} with respect to the comparator output voltages corresponding to the input signal shown in Fig. 2.

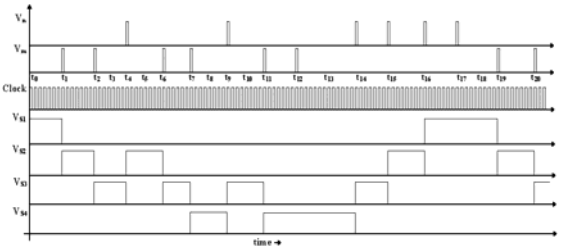

Figure. 5. Variation of the control voltages (V_{S1}-V_{S4})

The transitions of the control signals (V_{S2}-V_{S4}) shown in Fig. 5 are given in Table I which is a state assignment table. In this table, the present state and the next state of V_{S2}, V_{S3} and V_{S4} are represented by "a", "b" and "c" and "A", "B" and "C" respectively. The outputs of the latched comparators MP_1 and MP_2 are represented as V_m and V_n respectively. This table is used to design the digital network.

TABLE I
State assignment table for control voltages

Present State			Next State								
			Vm = 0 Vn = 0			Vm = 1 Vn = 0			Vm = 0 Vn = 1		
a	b	c	A	B	C	A	B	C	A	B	C
0	0	0	0	0	0	1	0	0	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
0	1	0	0	1	0	0	0	1	1	0	0
0	0	1	0	0	1	0	0	1	0	1	0

Quine-Mccluskey method has been used to get the logic expressions for the control signals (V_{S2}, V_{S3} and V_{S4}) which are given below;

$$V_{S1} = V_{S2} + V_{S3} + V_{S4} \quad (1)$$
$$V_{S2} = A = abcV_mV_n + abcV_mV_n + abcV_mV_n \quad (2)$$
$$V_{S3} = B = abcV_mV_n + abcV_mV_n + abcV_mV_n \quad (3)$$
$$V_{S4} = C = abcV_mV_n + abcV_mV_n + abcV_mV_n \quad (4)$$

Signal V_{S1} used to control the operation of switch S_1 is generated from the control signals (V_{S2}-V_{S4}). Fig. 6 demonstrates the digital network.

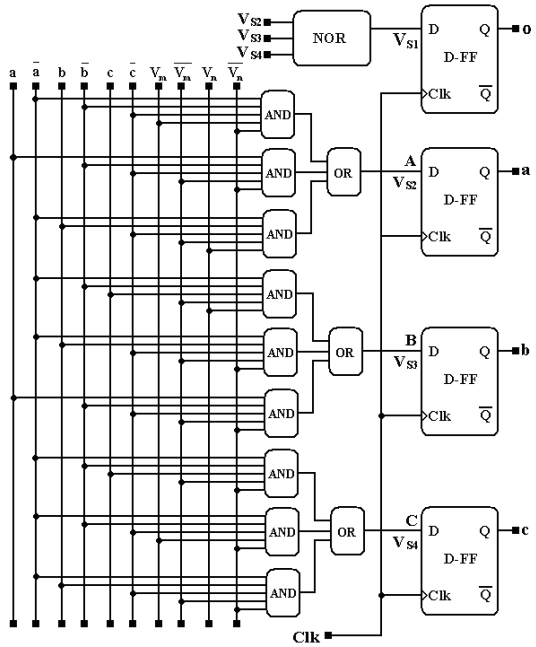

Figure 6. Implementation of the digital network

B. Encoder implementation

To explain the design principle of the encoder for the 2-bit SR-ADC, a triangular input signal shown in Fig. 7(a) has been considered. For this input signal, the control signals (V_{S1}, V_{S2}, V_{S3} and V_{S4}) generated in the DMN are shown in Fig. 7(b).

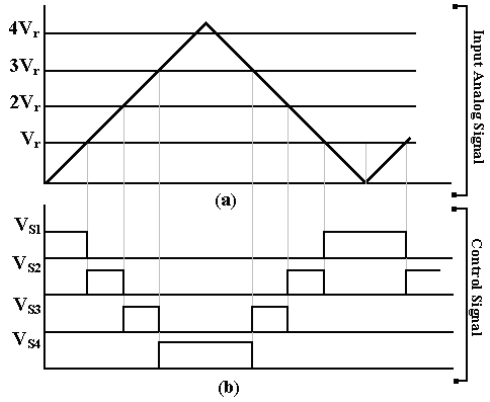

Figure 7. Triangular input waveform

Besides controlling the switches (S_1, S_2, S_3 and S_4), these control signals are also used as the input to the encoder for obtaining the 2-bit SR-ADC output (B_0 and B_1). The transition of the control signals and the SR-ADC output in the binary form are given in Table II.

TABLE II
2-bit SR-ADC output

V_{S4}	V_{S3}	V_{S2}	V_{S1}	B_1	B_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

It is evident from Table II that bits B_1 and B_0 are equal to (V_{S4} OR V_{S3}) and (V_{S4} OR V_{S2}) respectively. This completes the depiction of the operation and design principle of the 2-bit SR-ADC.

C. Design principle of 4-bit SR-ADC

The circuit operation and the design principle of the 4-bit SR-ADC follow the same steps described for the 2-bit SR-ADC. The differences between the 2-bit and 4-bit SR-ADC are given below.

a. Sixteen switches (S_1-S_{16}) instead of four switches (S_1-S_4) are used for connecting sixteen reference voltages ($1V_r$-$16V_r$) to the V_{in-} port for comparison with the input analog signal.
b. The number of control signals has been increased from four (V_{S1}-V_{S4}) to sixteen (V_{S1}-V_{S16}). This increase in the number of control signals increases the number of logic gates and D-FFs in the digital network.

Because of the increased control signals (from 4 to 16) at the input of the encoder and increased output bits (from 2 to 4), the number of logic gates in the encoder has been increased to the order of $\approx 2^8$. The designed 4-bit SR-ADC has been implemented using a 0.18µm, single poly and six metal CMOS process. Common centroid layout technique has been adapted at intra and interblock levels for obtaining a better matching between the devices. In the design of the pre-amplifier of the latched comparator and front end differential amplifier, dummy devices have been used to reduce the random offsets coming from mismatch. The active area of this 4-bit SR-ADC is ≈253.7µm*221.88µm.

IV. RESULTS AND DISCUSSION

The post layout simulation of this SR-ADC shows that the values of the Differential Non-Linearity (DNL) and the Integral Non-Linearity (INL) are < ±0.35LSB and < ±0.45LSB respectively. The SNDR of the SR-ADC becomes ≈23.01dB for an input signal frequency of 100MHz and sampling frequency of 500MHz. This value of the SNDR corresponds to an ENOB of ≈3.53. Fig. 8 shows the DNL/INL plot of the SR-ADC and Fig. 9 shows the FFT plot.

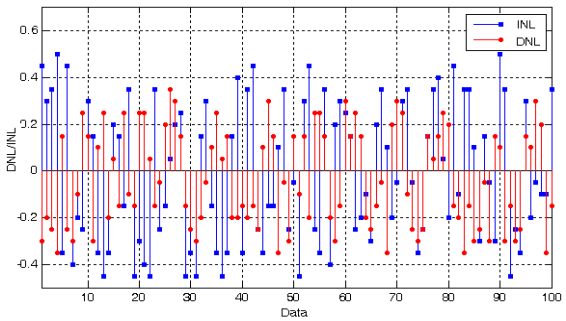

Figure 8. DNL/INL Plot

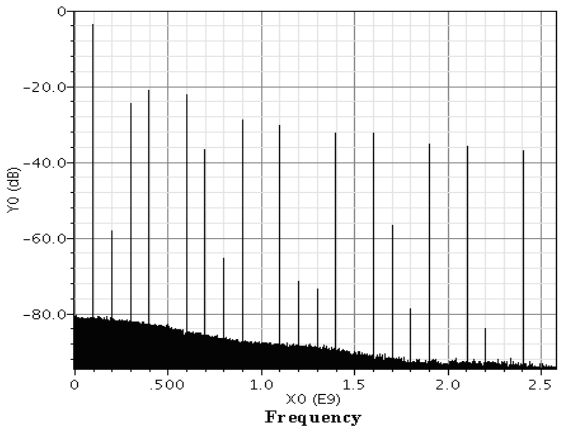

Figure 9. FFT Plot (f_{in} = 100MHz and f_S = 500MHz) (Noise Floor ≈81dB)

The comparison of the performance parameters of the designed SR-ADC with some previously published low power ADCs is given in Table III. From Table III it is evident that the speed of operation of the proposed 4-bit SR-ADC is 200MHz less than that of the 4-bit ADC reported in [2]. The lower sampling speed of the SR-ADC comes at the cost of reduced power dissipation. In comparison to the ADC given in [4], SR-ADC shows better sampling speed as well as improved resolution with lower power dissipation. The power dissipation of the ADCs published in [7] and [8] are very low in comparison to the proposed SR-ADC. But the sampling speeds of these ADCs are far less than that of the SR-ADC. Also, the area of the ADC [8] is larger than that of the SR-ADC. Considering all the above comparisons (only simulation results), it can be viewed that the overall performance parameters of the proposed SR-ADC are better than the ADCs reported in [2], [4], [7] and [8].

V. CONCLUSIONS

In this paper the working principle and the design methodology of a 4-bit SR-ADC have been presented. In this ADC the reference voltages are applied discretely for comparison with the input signal through a number of mutually exclusive switches. The ON and OFF states of the switches are controlled by a digital network designed with logic gates and flip-flops. To increase the resolution of this SR-ADC there will be an increase in the ladder network for generating the reference voltages maintaining the number of other analog blocks fixed. As a result the power dissipation and the circuit complexity will still remain low. While implementing the SR-ADC, steps have been taken in design and layout to improve the accuracy/linearity of this ADC. The designed 4-bit SR-ADC shows an SNDR of ≈23.01dB (ENOB ≈3.53) for a sampling frequency of 500MHz and input signal frequency of 100MHz. The total power consumption is ≈21.39mW for a power supply of 1.8V. The total core area of this ADC is ≈253μm*221μm. All these features of this SR-ADC make it suitable for the UWB application in the lower frequency band.

REFERENCES

[1] J. Reed,, "Introduction to Ultra Wideband Communication Systems", Prentice Hall, Apr. 2005.
[2] S. G. Talekar, S. Ramasamy, G. Lakshminarayanan and Venkataramani, "A Low Power 700MSPS 4bit Time Interleaved SAR ADC in 0.18um CMOS", TENCON 2009.
[3] J-F. Lin, S-J. Chang, C-C. Liu, and C-H. Huang, "A 10-bit 60-MS/s Low-Power Pipelined ADC With Split-Capacitor CDS Technique", IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 57, No. 3, March 2010.
[4] S. Banik, D. Gangopadhyay, and T. K. Bhattacharyya, "A low power 1.8V 4-bit 400-MHz flash ADC in 0.18_m Digital CMOS", Proc. of IEEE VLSID, 2006.
[5] B.P. Ginsburg, and A.P. Chandrakasan, "Dual Scalable 500MS/s, 5b Time-Interleaved SAR ADCs for UWB applications", Proc. of IEEE CICC,2005.
[6] Z. Caol, S. Yan, and Y. Li, "A 32mW 1.25GS/s 6b 2b/step SAR ADC in 0.13_m CMOS", Proc. of IEEE ISSCC, 2008.
[7] J. R. Fernandes, and M. M. Silva, "A Very Low-Power CMOS Parallel A/D Converter for Embedded Applications", ISCAS 2004.
[8] S-C. Hsia and W-C. Lee, "A very low-power flash A/D converter based on CMOS inverter circuit", IWSOC 2005.
[9] M. Dahoumane, D. Dzahini, J. Bouvier, E. Lagorio, J.Y. Hostachy, O. Rossetto, H. Ghazlane, and D. Dallet, "A low power and low signal 4 bit 50MS/s double sampling pipelined ADC for Monolithic Active Pixel Sensors", Journal of Instrumentation, Vol. 3, March 2008.

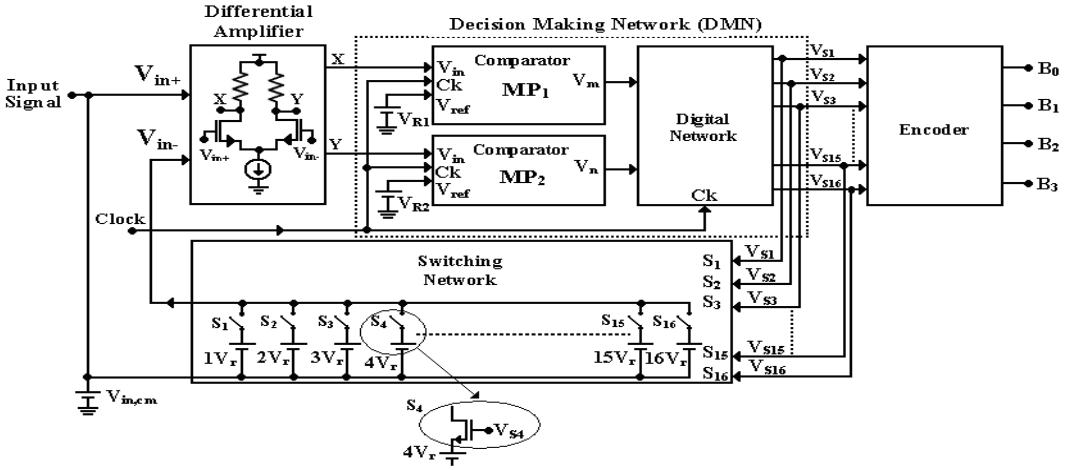

Figure 1. Architecture of the 4-bit SR-ADC

TABLE III
Comparison of the performance parameters of the low power ADC's with the designed SR-ADC (* → Simulated Results, # → Test results)

Ref.	[2]*	[4]*	[5]#	[7]*	[8]*	[9]#	Proposed Design*
Tech. (μm)	0.18	0.18	0.18	0.35	0.35	0.35	0.18
Supply (V)	1.8	1.8	1.2/ 1.8	1.5	3.3	5	1.8
Speed (MHz)	700	400	500	135	100	50	500
Input Swing (V)	1	2	-	1	2	-	1
ENOB/Res. (bits)	~3.68	~3.23	~3.06	4	8	4	~3.53
Power (mW)	23.3	30	7.8	0.21	0.895	2.6	21.39
Core area (μm^2)	-	-	1000*500	150*220	386*497	80*900	253*221

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