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A NEW LOW POWER TECHNOLOGY FOR POWER REDUCTION IN SRAM'S USING READ STABILITY WITH REDUCED TRANSISTOR COUNT FOR FUTURE CACHES

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A NEW LOW POWER TECHNOLOGY FOR POWER REDUCTION IN SRAM'S USING READ STABILITY WITH REDUCED TRANSISTOR COUNT FOR FUTURE CACHES

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Abstract- In this paper we are going to modify the Schmitt Trigger based SRAM for the purpose of more reduced power & area than the existing type of designs as well as the new design which is combined of virtual grounding with read Error Reduction Logic is compared with the existing technologies & the nanometer technology is also improved for the purpose of much improved reduction of area & power factors than the Schmitt Trigger based SRAM Designs the simulations were done using microwind & DSCH results.

I. INTRODUCTION:

As microprocessors and other electronics applications get faster and faster, the need for large quantities of data at very high speeds increases, while providing the data at such high speeds gets more difficult to accomplish. As microprocessor speeds increase from 25 MHz to 100 MHz, to 250 MHz and beyond, systems designers have become more creative in their use of cache memory, inter leaving, burst mode and other high-speed methods for accessing memory. The old systems sporting just an on-chip instruction cache, a moderate amount of DRAM and a hard drive have given way to sophisticated designs using multilevel memory architectures. One of the primary building blocks of the multi-level memory architecture is the data cache.

There are many reasons to use an SRAM or a DRAM in a system design. Design tradeoffs include density, speed, volatility, cost, and features. All of these factors should be considered before you select a RAM for your system design.

Speed: The primary advantage of an SRAM over a DRAM is its speed. The fastest DRAMs on the market still require five to ten processor clock cycles to access the first bit of data. Although features such as EDO and Fast Page Mode have improved the speed with which subsequent bits of data can be accessed, bus performance and other limitations mean the processor must wait for data coming from DRAM. Fast, synchronous SRAMs can operate at processor speeds of 250 MHz and beyond, with access and cycle times equal to the clock cycle used by the microprocessor. With a well-designed cache using ultra-fast SRAMs, conditions in which the processor has to wait for a DRAM access become rare.

• Density. Because of the way DRAM and SRAM memory cells are designed, readily available DRAMs have significantly higher densities than the largest SRAMs. Thus, when 64 Mb DRAMs are rolling off the production lines, the largest SRAMs are expected to be only 16 Mb.

• Volatility. While SRAM memory cells require more space on the silicon chip, they have other advantages that translate directly into improved performance. Unlike DRAMs, SRAM cells do not need to be refreshed. This means they are available for reading and writing data 100% of the time.

• Cost. If cost is the primary factor in a memory design, then DRAMs win hands down. If, on the other hand, performance is a critical factor, then a well-designed SRAM is an effective cost performance solution.

• Custom features. Most DRAMs come in only one or two flavors. This keeps the cost down, but doesn't help when you need a particular kind of addressing sequence, or some other custom feature. IBM's SRAMs are tailored, via metal and substrate, for the processor or application that will be using them.

Features are connected or disconnected according to the requirements of the user. Likewise, interface levels are selected to match the processor levels. IBM provides processor specific solutions by producing a chip with a standard core design, plus metal mask options to define feature sets.

Even though the SRAM is high Power Consuming Element to remove this unwanted power consumption a new Schmitt trigger based SRAM memory is proposed in our reference Paper. The proposed design is built after analyzing the different types of SRAM using low power design techniques the simulations were done under DSCH & Microwind Software.

The Problem Found in the existing SRAM Designs are listed below:

- SRAMs are consuming most of the power of the core Processor Element.
- The leakage in the SRAM circuit is high when compared to the all other processor components.

- As its consuming much power heat dissipation also occurs
- So less efficient than all other elements.

Need of Schmitt Trigger Based SRAM Designs

In order to resolve the conflicting read versus write design requirements in the conventional 6T bitcell, we apply the Schmitt Trigger (ST) principle for the cross-coupled inverter pair. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition. In the proposed ST SRAM bitcells, the feedback mechanism is used only in the pull-down path, as shown in figure. During input transition, the feedback transistor (NF) tries to preserve the logic "1" at output ( ) node by raising the source voltage of pull-down nMOS (N1). This results in higher switching threshold of the inverter with very sharp transfer characteristics. Since a read-failure is initiated by a input transition for the inverter storing logic "1," higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation.

For the input transition, the feedback mechanism is not present. This results in smooth transfer characteristics that are essential for easy write operation. Thus, input-dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-ability of the SRAM bitcell. Two novel bitcell designs are proposed. The first ST-based SRAM bitcell has been presented in our earlier work. Another ST-based SRAM bitcell which further improves the bitcell stability has been reported in existing works. To maintain the clarity of the discussion, the ST bitcell in [30] is termed the "ST-1" bitcell while the other ST bitcell is termed the "ST-2" bitcell shown in the Figure below.

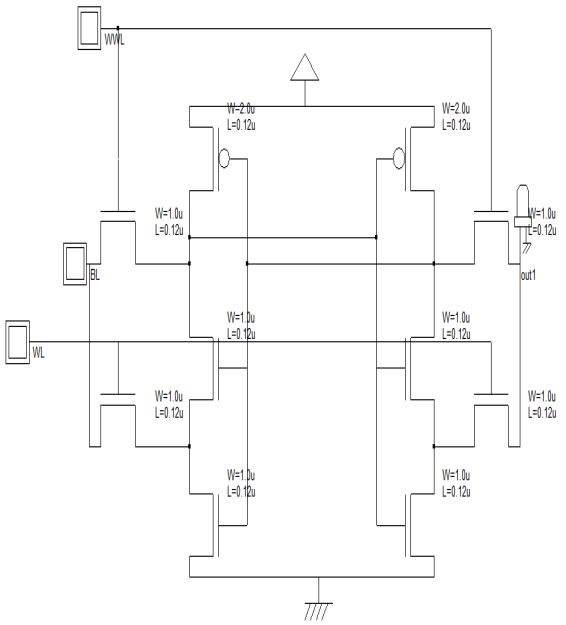

Figure 1: ST2 Bit Cell

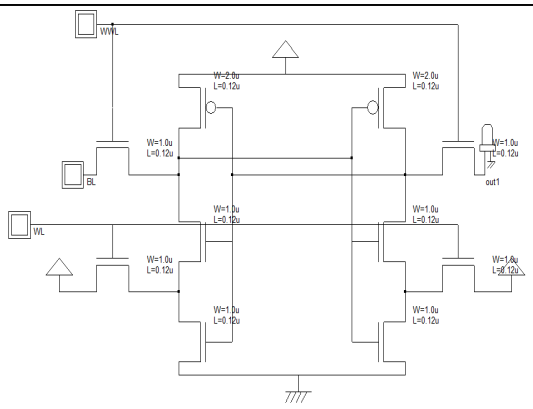

Figure 2: ST1 Bit Cell

Need of 7T-SRAM for enhanced read stability

A conventional 6TSRAM cell design consists of a cross-coupled inverter pair (M3-M6) that does data storage and two access transistors (M1-M2) to load/retrieve data on bit lines, BL and BLB. During a write operation, the data is loaded on the bit lines and the word select signal WS is turned high. A successful write operation occurs if the data is correctly latched in the cell. The bit lines are pre-charged to the supply voltage and the word select line is turned high to retrieve data during a read operation. The bit line (BL) connected to the storage node (V1) storing a '0' gets discharged. The storage node (V1) rises above '0' during a read operation due to voltage division between the access transistor (M1) and the driver transistor (M6). A read failure can occur if the voltage drop rises higher than the threshold voltage of the inverter (M3,M5).

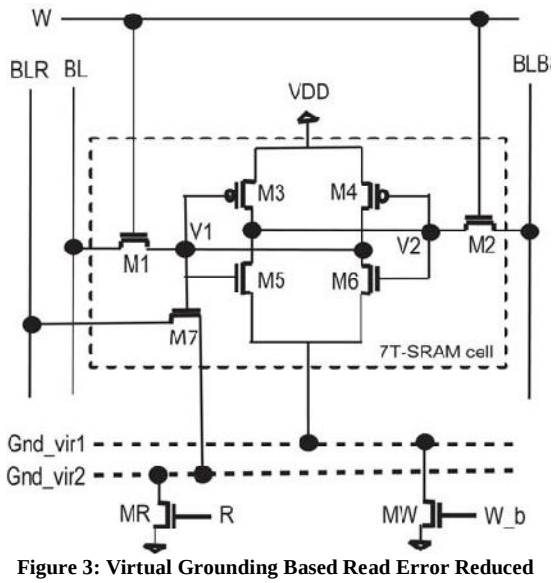

Figure 3: Virtual Grounding Based Read Error Reduced SRAM Cell

A conventional 6T-SRAM cell provides poor read stability since the access transistors provide direct access to the cell storage during a read operation. The proposed design (see Fig. 3) removes the access hazard during a read operation and therefore

eliminates the chances of cell content being inadvertently flipped. It consists of a cross-coupled pair (M3-M6) for data storage as in case of a conventional 6T-SRAM cell. However the ground terminal of the inverter pair is connected to a virtual ground (Gnd_vir1) in the proposed design to provide high speed low-power write operation. The word select line 'WS' is held high only during a write operation to load new data in the cell by turning on the write access transistors (M1-M2). A read access transistor (M7) connected to a virtual ground (Gnd_vir2) is used to retrieve data on read bit line (BLR) during a read operation. Our design decouples read/write operation using separate read/write access transistors. Therefore it doesn't suffer from constrained read/write requirements as in 6T-SRAM design.

Proposed Low Power SRAM

As the Schmitt trigger based designs are having high number of transistor to make the read stability that is 10 Transistor which very high when compared to the existing 6T SRAM Design we are going to combine the mentioned read stability at the above part to our proposed work to reduce the count than the Schmitt trigger based designs at the same time we are going to achieve reduced power consumption with reduced transistor count without affecting the read stability. At the same time the proposed design supports separate read and write operations as in the Schmitt Trigger based designs. Our idea is to combine these to different technologies & to design a new circuit with much efficiency than the existing two designs.

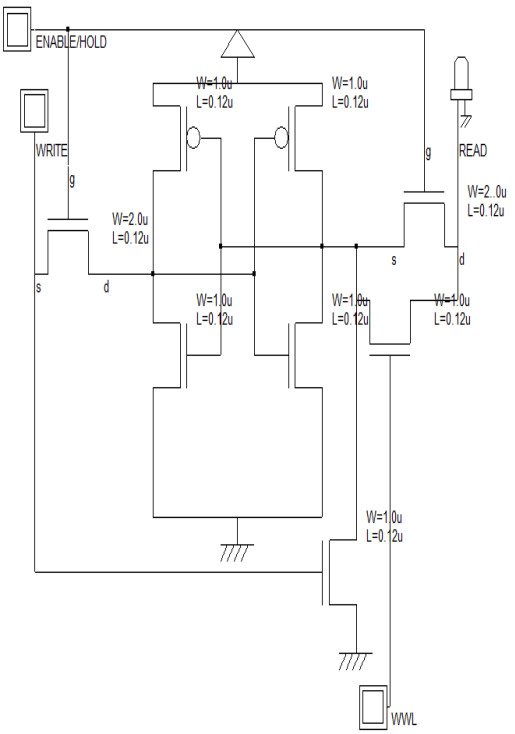

Figure 4: Proposed Read Error Reduced SRAM Cell with Reduced Transistor Count

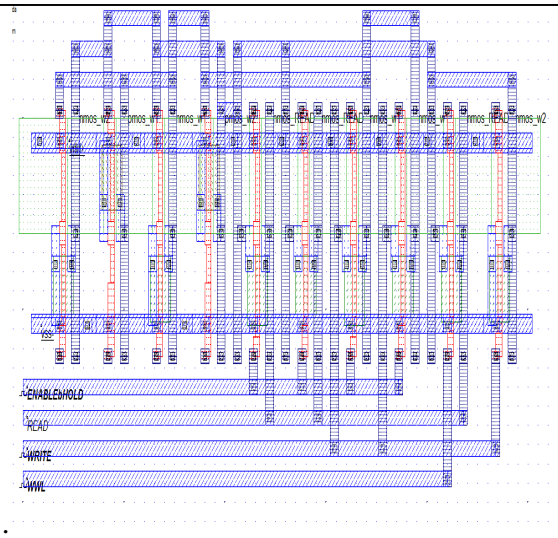

Figure 5: Layout of Proposed Design

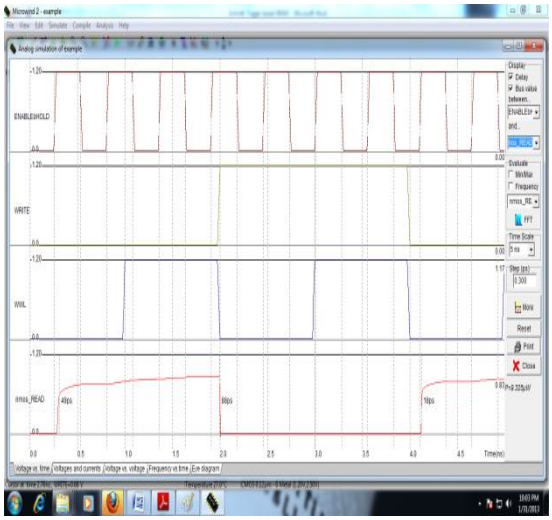

Figure 6: Power Analysis of Proposed Design

Tabulation & Results

Type	Power	Area
6T SRAM	0.288mW	266um^2
ST-2	0.251mW	247um^2
Proposed Method	2.890uW	14.2um^2

CONCLUSION

Our proposed design shows that much less power than the existing ones 2.890uw at the standard Our Proposed layout combined with 6T & Virtual grounding with read error reduction Ciruit concept 120nm technology. And it is having much reduced area than the conventional SRAM designs. Thus this design can be used for future SRAM core memories.

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