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An Overview of Charge Pump for Phase Lock Loop System for High Frequency Application



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Abstract - Phase lock loop is fundamental building block of modern communication system. Phase lock loop are typically used to provide local oscillator function in radio receiver or transmitter. The design methodology and test result of charge pump structure for phase lock loop application are presented. The structure is composed of two charge / discharge block. This paper provides study of various charge pump and discuss the technologies that is used to design charge pump.

Keywords— Charge Pump, various charge pumps, comparison of CP, difficulties regarding with charge pump.

I. INTRODUCTION

A Phase lock loop is a closed loop circuit that compares its output phase with of an incoming reference signal and adjust itself until both are aligned [1]. Once the loop is locked the frequency of output signal is multiple of input signal's frequency. One of most common implementation of integrated circuits Phase lock loop is in frequency synthesizer, where Phase lock loop are used to generate set of programmable.

Phase lock loop consists of phase / frequency, detector, charge pump, voltage control oscillator i.e. VCO and frequency divider. Phase detector detects change in phase and provides information to charge pump. Charge pump is an important block of Phase lock loop system which is DC to DC converter and uses capacitor as energy storage element. It converts phase error information into current to generate control voltage. A VCO is used to generate frequency which is divided by frequency divider and provide to phase detector. This paper discusses the design of charge pump to reduce charge sharing and charge injection problem for high frequency application.

II. ARCHITECTURE OF CHARGE PUMP

Charge pump is dc to dc converter and uses capacitor as energy storage element. In charge pump phase lock loop, the phase frequency detector measure phase/frequency difference between reference and VCO output to generate up/down pulses. Charge pump consist of two transistor switch (S_1 , S_2) which generate current pulses to perturb VCO control voltage on filter capacitor as shown in fig 1.

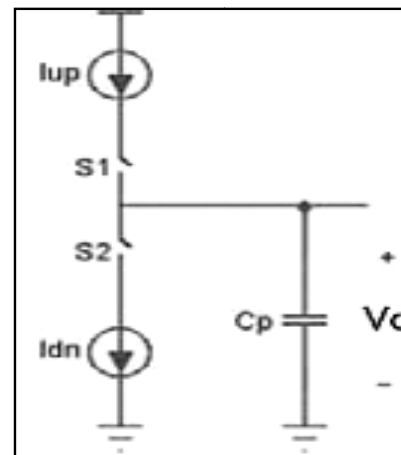


Fig. 1. Single ended charge pump model

When implemented in circuit phase / frequency and charge pump circuit have non – idealities. Non ideal behaviour of charge pump can contributes significantly to phase lock loop output jitter.

III. CHARGE PUMP

Bortecene Terlemez and John P. Uyemura proposed paper in 2004, differential charge pump design technique is explored to achieve low charge sharing and charge injection in low voltage Phase lock loop application [5]. It is implemented in 0.18 μm technology and utilises LC oscillator and loop filter 123dbc/Hz phase noise at 1 MHz frequency offset from the 2.5 GHz VCO frequency confirm the charge pump operation within a high performance phase lock loop system.

Proper differential operation is realized by the CMFB circuit, which also increases the output dynamic-range and charge/discharge symmetry. In this model, the common-mode voltage of the charge pump outputs, fast (FST) and slow (SLW), is sensed and compared to a common-mode reference VCMO, which is set to be the mid-rail voltage. Also the low-pass filter capacitor voltages, rather than the charge pump outputs, can be used to generate the common-mode voltage. The common-mode sensing circuit is basically a transconductance amplifier, whose linearity can be increased for a wide input range by using bigger resistors, R1 and R2. However, these bigger resistors pull the DC gain down, increasing the steady state error. The transistors M18, M20, M28, M29, M32, and M33 are inserted so that the charging and discharging currents can be more accurately scaled.

Shantanu, Abhishek and Rajendra proposed charge pump in 2004 in standard CMOS process suited for low voltage operation [4]. Each stage consists of cross-connected NMOS transistor with serial PMOS switches to ensure proper charge transfer from one stage to next stage. Double DC output can be achieved by PMOS transistor to avoid threshold voltage drop. The bulk of series pass PMOS switches are tied to the output of each stage and the bulk of NMOS are connected to GND as in traditional charge pump designs. Better performance can be achieved by tying bulk terminal of NMOS to the source. Simulation part shows proposed charge pump offers better performance in term higher output voltage as compared to Dickson and NCP-2 charge pump.

Rania H. Mekky and Mohamed Dessouky proposed gain boosting charge pump in 2007 which reduces the problem of channel length modulation but suffer from current mismatching [1,5]. Modified gain boosting charge pump which uses current mirror circuit to overcome the problem of current mismatching. In addition to gain-boosting used to increase the output impedance of the charge pump, a low voltage cascode current mirror is used to enhance current matching over process corners. A good matching between the two current sources of the charge pump can be achieved with current mismatch equal to 0.6% in typical condition and 1% over all process variation. The charge pump output compliance voltage range of .3-.2.2 volt is achieved for 2.5 volt using I/O devices of a 90 nm technology

Quan Sun and Yann Hu proposed paper in 2008, frequency multiplication phase lock loop, which employ voltage regulator to get stable power supplies [6]. In this CMOS phase lock loop is used for on-chip clock generation in MAPS i.e. monolithic active pixel sensor for solenoid tracker at RHIC [7]. An on-chip voltage regulator provides two stable power supplies to the analog circuit and VCO respectively. At 160MHz, jitter level is less which provides synchronously performance

of sensor. By using virtual grounded cascode compensation technique and connection in series, the voltage regulator achieves a maximum PSNR (Power Supply Noise Rejection) of -40 dB over the entire frequency Spectrum [8]. The circuit is fabricated in a .35 μm standard CMOS process and power consumption is 7mW.

Two identical PLLs have been included in the engineering run of STAR sensor, PHASE1. One of them will provide clock to the sensor. The other one with more pads will be used for testing performance.

Tsung-Hsien Lin, Ching-Lung Ti and Yao-Hong Liu proposed a paper in 2009 novel charge pump circuit and gate offset linearization technique to improve performance of delta sigma fractional -N phase lock loop system [10]. The phase/frequency detector charge pump nonlinear transfer characteristics are cause of nonlinearity in phase lock loop system. The nonlinearity in phase lock loop system is due to current mismatch and dead zone phenomena. Dead zone problem can be eliminated by adding proper delay in phase frequency detector reset path. But current mismatch problem is there. Two extra feedback transistors are added to circuit to compensate channel length modulation effect, so current mismatch is reduced.

The gated-offset technique described in the paper presents a compromise between the tradeoffs of design complexity and level of reference spurs. Compared with [12], the reference spur is improved in this work with just an addition of a simple gating circuit. On the other hand, the technique in [11] achieves the best reference spur suppression, but at the cost of more complicated design, which increases chip area and power consumption.

The reference spur is improved by adding simple gate circuit. The proposed technique is demonstrated in design of 2.4GHz.

Pin-En Su and S.Pamarti proposed a paper in 2010, charge pump circuit is an important source of spurious tones [13]. Mismatches between sourcing and sinking current source in charge pump in conjunction with quantization noise of Delta sigma fractional N phase lock loop causes tones. Two techniques are proposed which uses purely digital modulation for reduction spurious tones. First is naive mismatch shaping technique and second is proper mismatch shaping technique [15]. The second technique further spectrally shapes the residual charge pump mismatch errors to suppress close-in phase noise. No spurs are observed and -120 dBc/Hz phase noise is achieved at frequency offsets lower than 10 kHz in simulation. These techniques eliminate fractional spurs and Quantization noise caused by charge pump error. Both technique convert charge pump error power

into high pass shaped, spur free wide band noise which is suppressed by phase lock loop system [14].

Unlike the naïve technique, the proper mismatch shaping technique employs a finite state machine to not only high-pass shape the wide band noise, but to also ensure that it has a zero at dc.

IV. COMPARISON OF CHARGE PUMP

Dickson charge pump	Conventional charge pump	Single ended charge pump
Suffer from voltage drop	Suffer from channel length modulation	Suffer from charge ejection and sharing problem
NCP uses CTS but its output voltage is less	Uses gain boosting circuit but required high output impedance	Due to current and switch transistor reversed only charge sharing problem is removed

V. PROPOSED WORK

As discuss above, charge pump suffer from charge sharing and charge injection problem. To reduce this, channel length modulation and current mismatching should be reduces which can be done by using current mirror circuit.

V. CONCLUSION

Implementation of proposed work will reduces power of charge pump and also reduces charging sharing and charge injection problem. By using current mirror circuit, channel length modulation and current mismatching is reduced

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