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DESIGN OF LOW VOLTAGE LOW POWER OPERATIONAL AMPLIFIER

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Abstract- This Thesis presents a design of the Folded-cascade operational amplifier which leads to high gain as compared to a normal cascade circuit. In this project; specifications of analog systems into op amp level net-lists of library components is studied and simulated using XILINX. As the power-supply voltages because of the technology improvement and it are desired to reduce power supply to minimize power dissipation, many challenges are faced by the analog designer. One is to keep noise level as possible. The op-amp must be designed to with the ever decreasing power supply voltages. As the power supply voltages begin to approach 2Vt, new technique and new op-amp topology like folded cascade should be used.

Keywords- *complementary metal-oxide semiconductor, common-mode range, input common-mode range, Power-supply rejection ratio, CASCODE, Slew Rate.*

I. INTRODUCTION

The design of op amps continues to pose a challenge as the supply voltage and transistor channel length scale down with each generation of CMOS technologies. Operational amplifiers are the amplifier (controlled sources) that has sufficiently high gain so that when negative feedback is applied, the closed loop transfer function is practically independent of the gain of the op amp.

This principle has been exploited to develop many useful analog circuits and systems. The primary Requirement of an op amp is to have an open-loop gain that is sufficiently large to implement the negative feedback concept. Controlled linear sources and passive linear devices such as generic models for resistors, capacitors and inductors were presented [1-3]. This communication shows this Method is applicable to some active devices like high loop gain operational amplifiers (Op-Amps). A generic amplifier model is presented allowing for user defined feedback networks. As the channel lengths of CMOS technology decrease, the maximum allowable voltage will decrease. Also, as more components are included in the same area on integrated circuits, the power dissipation increases. Finally, the requirement for portable electronics implies battery operation which favors low voltage and low power circuits. These factors and others have caused many to suggest that future implementation of mixed analog digital circuits using standard CMOS will have power supplies of 1.5V or less an important factor concerning analog circuits is that the threshold voltages of future standard CMOS technologies are not anticipated to decrease much below what is available today[1,2]. It is necessary that the analog power supply be at least equal to the sum of the magnitudes of the n-channel and p-channel thresholds. This implies that low voltage analog circuits are incompatible with the CMOS technology trends of the future. Ways to circumvent this conflict are to develop technologies with lower thresholds, increase the lower voltage power supply by on-chip dc-dc converter, or develop circuit techniques that are compatible with future standard CMOS technology trends.

This paper will briefly review some of the limitations of analog circuits at low voltage. Next, circuit methods of using existing CMOS technology will be described that permit analog circuit operation at low voltages. Each of these methods alone cannot solve the problem but together they offer attractive solutions. One of these methods which are unique with this paper is the channel JFET and its operation and characterization are presented in detail. Next, it is shown how to use these methods to implement analog circuit building blocks such as current sinks/sources, differential amplifiers, and current mirrors. OP-AMP: An operational amplifier (op-amp) is a DC-coupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output. An op-amp produces an output voltage that is typically hundreds of thousands of times larger than the voltage difference between its input terminals.
Differential signaling is a method of transmitting information electrically with two complementary signals sent on two paired wires, called a differential pair. Since external interference tend to affect both wires together, and information is sent only by the difference between the wires, the technique improves resistance to electromagnetic noise compared with use of only one wire and an un-paired reference (ground). The technique can be used for both analog signaling, as in balanced audio, and digital signaling, as in RS-422, RS-485, Ethernet over twisted pair, PCI Express, Display Port, HDMI, and USB. The opposite technique is called single-ended signaling. Differential pairs are usually found on a printed circuit board, in cables (twisted-pair cables, ribbon cables), and in connectors

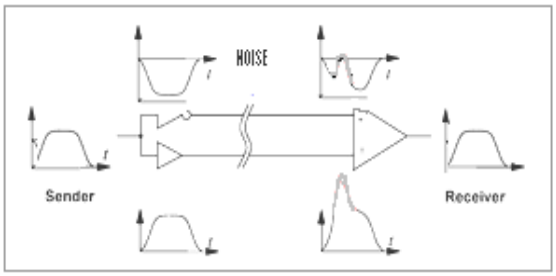

Fig1: Tolerance of ground offsets

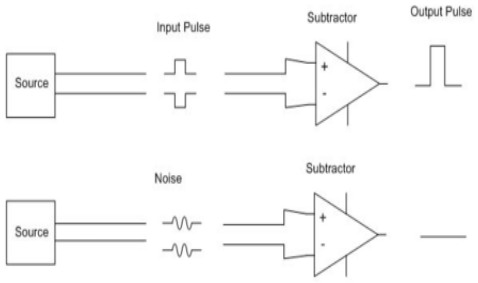

Fig2: Differential Signaling

In a system with a differential receiver, desired signals add and noise is subtracted away.At the end of the connection, the receiving device reads the difference between the two signals. Since the receiver ignores the wires' voltages with respect to ground, small changes in ground potential between transmitter and receiver do not affect the receiver's ability to detect the signal.

Operational amplifiers had their origins in analog computers, where they were used to do mathematical operations in many linear, non-linear and frequency-dependent circuits. Characteristics of a circuit using an op-amp are set by external components with little dependence on temperature changes or manufacturing variations in the op-amp itself, which makes op-amps popular building blocks for circuit design.

Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices. Many standard IC op-amps cost only a few cents in moderate production volume; however some integrated or hybrid operational amplifiers with special performance specifications may cost over $100 US in small quantities Op-amps may be packaged as components, or used as elements of more complex integrated circuits.

The op-amp is one type of differential amplifier. Other types of differential amplifier include the fully differential amplifier (similar to the op-amp, but with two outputs), the instrumentation amplifier (usually built from three op-amps), the isolation amplifier (similar to the instrumentation amplifier, but with tolerance to common-mode voltages that would destroy an ordinary op-amp), and negative feedback amplifier (usually built from one or more op-amps and a resistive feedback network).

Input Common Mode Voltage Range

The Input Common Mode Voltage is defined as the average voltage at the inverting and non-inverting input pins.

1. If the common mode voltage gets too high or too low, the inputs will shut down and proper operation ceases. The common mode input voltage range, CMVR, specifies the range over which normal operation is guaranteed.

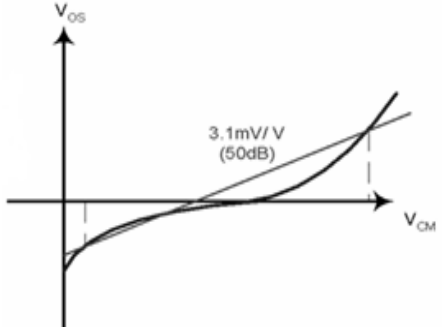

Fig3: Input offset voltage Vs common mode voltage

This graph shows Input Offset Voltage vs. Common Mode Voltage. The blue line is the actual measured value of the input common mode voltage. The red line is the calculated value.

1. The upper limit is determined by the saturation point of one of the two input transistors.
2. The lower limit is determined by the transistor which supplies the bias current.

Defining input common-mode range

When speaking of op amp inputs, input common-mode voltage (V_{ICM}) is one of the first terms of which an engineer thinks, but may lead to some initial confusion. V_{ICM} describes a particular voltage level and is defined as the average voltage at the inverting and non-inverting input pins.

Advantages of cascaded op-amp:

a) Good common-mode range
b) Self compensation
c) High gain
d) Relatively low power-dissipation
e) High output resistance

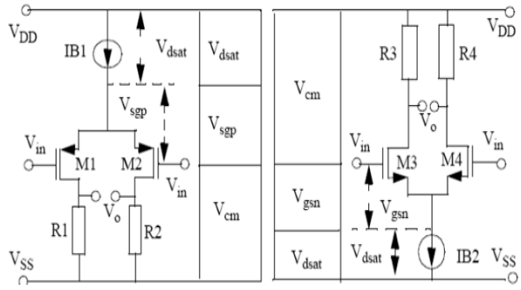

Fig4: The common-mode input range of a p-channel and an n-channel differential pair

For a p-channel pair, the common mode input voltage range is given by:
VSS ≤ Vcommon ≤ VDD– Vdsat – Vsgp
Where Vcommon is the common mode input voltage, Vsgp is the source-gate voltage of an input transistor, Vdsat is the voltage across a current source, VDD is the positive supply voltage, and VSS is the negative supply voltage. For an n-channel input pair, the common mode input voltage is given by:
VSS +Vgsn +Vdsat ≤ Vcommon ≤ VDD.
Where Vgsn is the gate source voltage of an n channel input transistor.

Low Voltage Low Power Techniques in Analog Circuit Design

1. Technology Consideration

Threshold voltage is not proportionally reduced for scaled down technologies. A natural solution is the use of multi-threshold process technologies. Unfortunately, this kind of technology is more expensive and frequently not easy to reproduce. Multi-threshold process technology is expensive due to fabrication process. Higher fabrication cost presents for a multiple threshold voltages technology that suffers from reliability problems. Some design advantage can be obtained by using BICMOS technology at the expense of additional cost, since more fabrication steps are involved [9].

2. Transistor model capable to provide performance and power tradeoff

For CMOS analog circuits, when the transistors operate in weak inversion region, gm/ID reaches the maximum, hence the minimum power consumption can be achieved due to the small quiescent current at the expense of large silicon area and slow speed. When MOS transistors operate in strong inversion, however, although good frequency response and small area are obtained, non-optimum larger power is consumed. For most analog circuits, the best tradeoff among area, power and speed can be achieved when the transistors work in moderate inversion region but conventional MOS transistor models provide different sets of equations for weak and strong inversion regions, even in computer simulation tools[10].

EXPERIMENTAL DESIGN

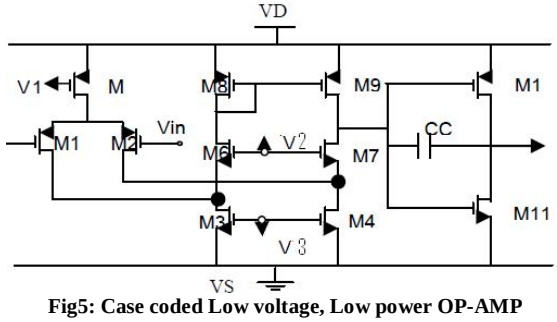

Fig5: Case coded Low voltage, Low power OP-AMP

This architecture does not require perfect balance of current in differential amplifier because excess dc current can flow into or out of the current mirror, because the drains of M1 and M2 are connected to drains of M4 an M5. The bias current I(M5), I(M3) and I(M4) are designed so that the dc current through current mirror never be zero. If this current goes to zero then, this requires a delay in turning the mirror back on because of the parasitic capacitances that must be charged. For example if Vid the differential voltage is large enough to turn M1 on and M2 off. Then all of the I(M5) flows through the M1 and none through M2, resulting in I(M5)=I(M1) and I(M2)=0. If I(M3) and (M4) are not greater than I(M5) then the current through M8 will be zero. To avoid this we have to take I(M3) and I(M4) normally between I(M5) and 2I(M5). In the current design this is I(M3)=I(M4)=1.5 times the I(M5).

SIMULATION AND RESULTS:

The objective of this section is to provide the background for simulating and testing a LVLP Op-amp. Consider the methods of simulating an Op-amp that are appropriate to Xilinx but the concepts are applicable to other types of computer simulation programs, because the simulation and measurements of the amplifier are almost identical and are presents simultaneously. The only differences found is in parasitic that are actual measurement introduce in the Op-amp circuit and the bandwidths of the instrumentation.

The categories of Op-amp measurements and simulation include open loop frequency response, common-mode gain, power supply rejection ratio, common mode input and output voltage ranges slew rate.

SIMULATION RESULTS

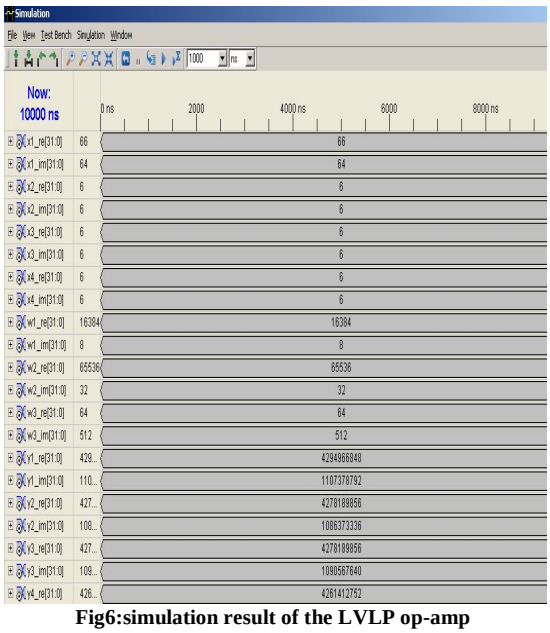

Fig6:simulation result of the LVLP op-amp

SYNTHESIS RESULTS
EXISTING TECHNIQUE

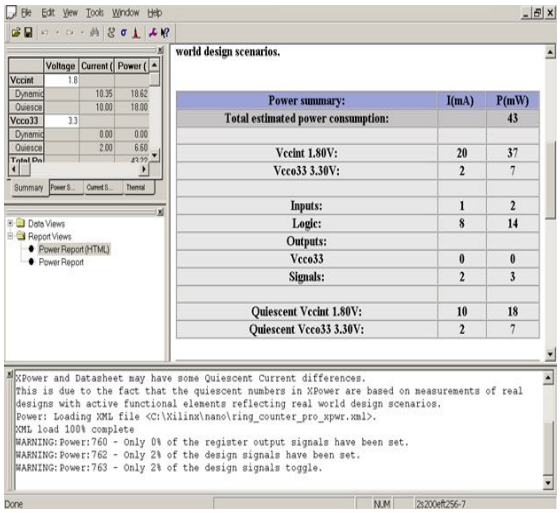

Fig7: Results of the existing system

PROPOSED TECHNIQUE

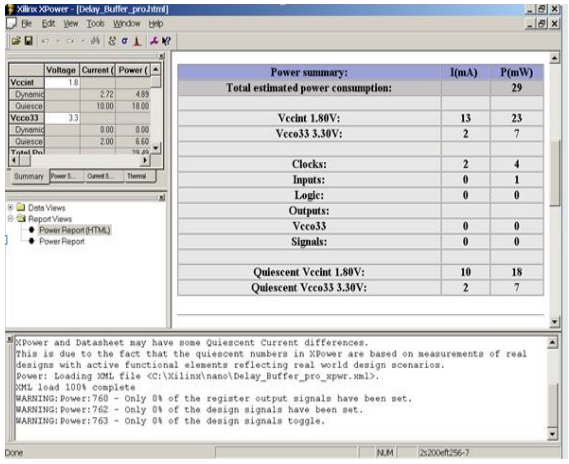

Fig8: Results of the proposed system

CONCLUSION:

As the analog content of large mixed signal integrated circuit increases, it is important to reduce power dissipation. Op-amp for minimum power dissipation is required for the required performance along with the means of increasing the output current when driving large capacitive loads. It was seen that a low power op-amp could be obtained at the expense of frequency response and other desirable characteristics. Most low power op-amp work in weak inversion mode to reduce power dissipation and therefore perform like BJT op-amp circuits.

As the power-supply voltages because of the technology improvement and it are desired to reduce power supply to minimize power dissipation, many challenges are faced by the analog designer. One is to keep the noise level as possible. The op-amp must be designed with the ever decreasing power supply voltages. As the power supply voltages begin to approach 2Vt, a new op-amp topology like folded cascode should be used.

This Thesis presents a complete behavioral, simulation and synthesis method in analog systems for cascaded op amp. Folded cascade op-amp is a better solution for low voltage low power operation as compared to conventional op-amp. It provides large ICMR and better frequency performance, which is required for low voltage operation and can be designed for low power operation also. Finally, by applying clock gating technique to cascaded op-amp; total dissipated power is reduced and enhanced op-amp is yielded.

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