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DESIGN &ANALYSIS OF DUAL STACK METHOD FOR FUTURE TECHNOLOGIES

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Abstract- As low power circuits are most popular now a days as the scaling increase the leakage power in the circuit also increases rapidly so for removing these kind of leakages and to provide a better power efficiency we are using many types of power gating techniques. In this paper we are going to analyse the different types of flip-flops using different types of power gated circuits using low power VLSI design techniques and we are going to display the comparison results between different nanometer technologies. The NMOS1mulations were done using Microwind Layout Editor & DSCH software and the results were given below.

I.INTRODUTION

The scaling of process technologies to nanometer regime has resulted in a rapid increase in leakage power disNMOS1pation. Hence, it has become extremely important to develop design techniques to reduce static power disNMOS1pation during periods of inactivity. The power reduction must be achieved without trading-off performance which makeNMOS1t harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques for reducing leakage power in sleep or standby mode. Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground). This device is turned-off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance.

Power gating technique uses high Vt sleep transistors which cut off VDD from a circuit block when the block is not switching. The sleep transistor NMOS1zing is an important design parameter. This technique, also known as MTCMOS, or Multi-Threshold CMOS reduces stand-by or leakage power, and also enableNMOS1ddq testing.

Power gating affects design architecture more than clock gating. It increases time delays as power gated modes have to be safely entered and exited. Architectural trade-offs exist between designing for the amount of leakage power saving in low power modes and the energy disNMOS1pation to enter and exit the low power modes. Shutting down the blocks can be accomplished either by software or hardware. Driver software can schedule the power down operations. Hardware timers can be utilized. A dedicated power management controller is another option. An externally switched power supply is a very baNMOS1c form of power gating to achieve long term leakage power reduction. To shut off the block for small intervals of time, internal power gating is more suitable. CMOS switches that provide power to the circuitry are controlled by power gating controllers. Outputs of the power gated block discharge slowly. Hence output voltage levels spend more time in threshold voltage level. This can lead to larger short circuit current.

Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies toparts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.
The quality of this complex power network is critical to the success of a power-gating design. Two of the most critical parameters are the IR-drop and the penaltieNMOS1n NMOS1licon area and routing resources. Power gating can be implemented using cell- or cluster-based (or fine grain) approaches or a distributed coarse-grained approach.

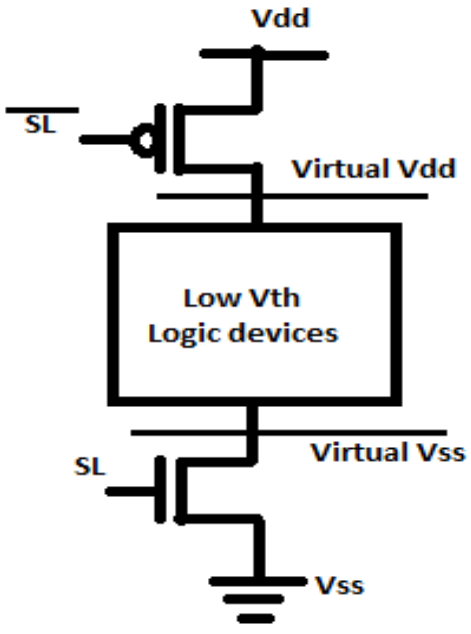

Figure:1 Powergating circuits

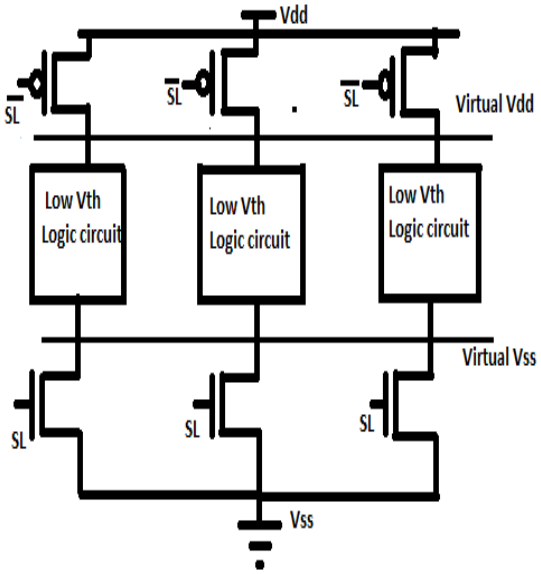

Figure:2 DSTN Structure

An example for Distributed sleep transistor network shown in Fig:2 While implementing sleep transistors in CMOS circuits, the perfonnance is found to be better when they are interconnected to form a network. There is much such architecture out of which most notable s tructure is the distributed sleep transistor network (DSTN).In a distributed sleep transistor network gates in a cluster are connected to the sleep transistor by virtual-ground wires. The spot at which sleep transistor is connected to logic gates is called tapping point. By adding more wires to form a mesh containing all virtual-ground wires, we obtain the DSTN structure Among the leakage reduction techniques, the power gating technique has become one of the most effective methods. With the circuit density being increased at nano scale, the scheduling of the sleep transistors plays a vital role in reducing the leakage power of the circuit.

II. POWER-GATING PARAMETERS

Power gating implementation has additional conNMOS1derations for timing closure implementation. The following parameters need to be conNMOS1dered and their values carefully chosen for a successful implementation of this methodology.

1. Power gate Size: The power gate Size must be selected to handle the amount of switching current at any given time. The gate must be bigger such that there is no measurable voltage (IR) drop due to the gate. As a rule of thumb, the gate Size is selected to be around 3 times the switching capacitance. Designers can also choose between header (P-MOS) or footer (N-MOS) gate. Usually footer gates tend to be smaller in area for the same switching current. Dynamic power analyNMOS1s tools can accurately measure the switching current and also predict the Size for the power gate.
2. Gate control slew rate: In power gating, thiNMOS1s an important parameter that determines the power gating efficiency. When the slew rate is large, it takes more time to switch off and switch-on the circuit and hence can affect the power gating efficiency. Slew rate is controlled through buffering the gate control Signal.
3. NMOS1multaneous switching capacitance: ThiNMOS1mportant constraint refers to the amount of circuit that can be switched NMOS1multaneously without affecting the power network integrity. If a large amount of the circuit is switched NMOS1multaneously, the resulting "rush current" can compromise the power network integrity. The circuit needs to be switched in stageNMOS1n order to prevent this.
4. Power gate leakage: NMOS1nce power gates are made of active transistors, leakage reduction is an important conNMOS1deration to maximize power savings.

i) Fine-grain power gating

Adding a sleep transistor to every cell that is to be turned off imposes a large area penalty, and individually gating the power of every cluster of cells creates timing issue NMOS 1ntroduced by inter-cluster voltage variation that are difficult to resolve. Fine-grain power gating encapsulates the switching transistor as a part of the standard cell logic. Switching transistors are designed by either the library IP vendor or standard cell designer. Usually these cell designs conform to the normal standard cell rules and can eaNMOS1ly be handled by EDA tools for implementation.

The Size of the gate control is designed conNMOS1dering the worst case scenario that will require the circuit to switch during every clock cycle, resulting in a huge area impact. Some of the recent designNMOS1mplement the fine-grain power gating selectively, but only for the low Vt cells. If the technology allows multiple Vt libraries, the use of low Vt deviceNMOS1s minimum in the design (20%), so that the area impact can be reduced. When using power gates on the low Vt cells the output must be isolated if the next stage is a high Vt cell. Otherwise it can cause the neighboring high Vt cell to have leakage when output goes to an unknown state due to power gating.

Gate control slew rate constraint is achieved by having a buffer distribution tree for the control Signals. The buffers must be chosen from a set of always on buffers (buffers without the gate control Signal) designed with high Vt cells. The inherent difference between when a cell switches off with

respect to another, minimizes the rush current during switch-on and switch-off.

Usually the gating transistor is designed as a high Vt device. Coarse-grain power gating offers further flexibility by optimizing the power gating cells where there is low switching activity. Leakage optimization has to be done at the coarse grain level, swapping the low leakage cell for the high leakage one. Fine-grain power gating is an elegant methodology resulting in up to 10 times leakage reduction. This type of power reduction makeNMOS1t an appealing technique if the power reduction requirement is not satisfied by multiple Vt optimization alone.

ii) Coarse-grain power gating
The coarse-grained approach implements the grid style sleep transistors which drives cells locally through shared virtual power networks. This approach is less senNMOS1tive to PVT variation, introduces lesNMOS1R-drop variation, and imposes a smaller area overhead than the cell- or cluster-based implementations. In coarse-grain power gating, the power-gating transistor is a part of the power distribution network rather than the standard cell.
There are two ways of implementing a coarse-grain structure:

1. Ring-based: The power gates are placed around the perimeter of the module that is being switched-off as a ring. Special corner cells are used to turn the power Signals around the corners.
2. Column-based: The power gates are inserted within the module with the cells abutted to.each other in the form of columns. The global power is the higher layers of metal, while the switched power iNMOS1n the lower layers.

III. CONVENTIONAL BCD ADDER

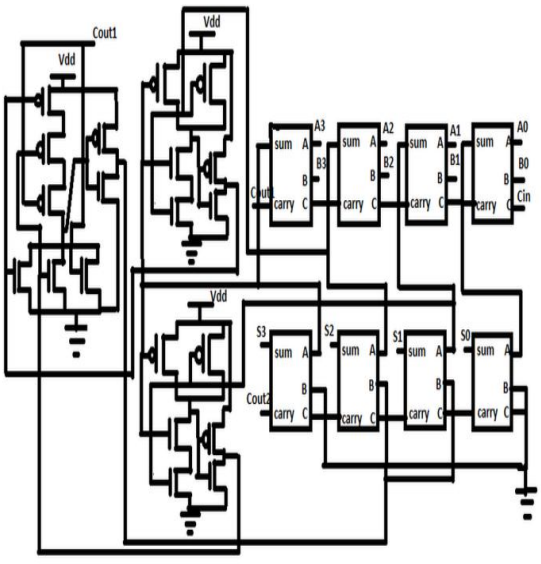

Figure:3 4 Bit conventional BCD ADDER

IV. VIRTUAL GROUNDING

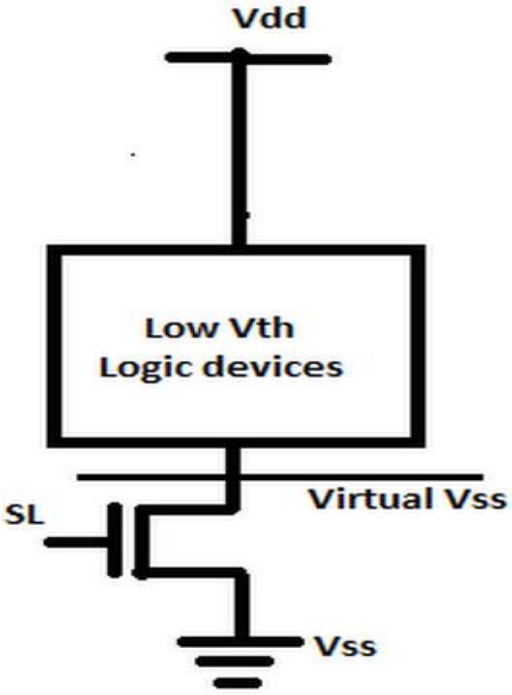

Figure:4 Power gating [Virtual grounding]

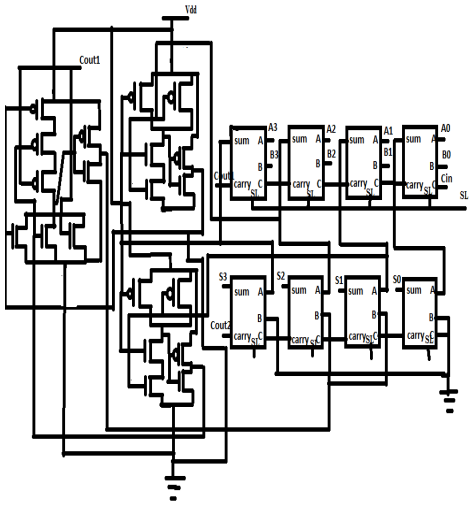

Figure:5 4 Bit BCD ADDER With Virtual Grounding

DUAL STACK TECHNIQUE

A variation of the sleep approach, the zigzag approach, reduces wake- up overhead caused by sleep transistors by placement of alternating sleep transistors assuming a particular pre-selected input vector [6]. Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half Size transistors [7] Then sleep transistors are added in parallel to one of the divided transistors. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel

to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a NMOS1gnificant matter for this approach NMOS1nce every transistor is replaced by three transistors and NMOS1nce additional wires are added for S and S', which are sleep Signals. Another technique called Dual sleep approach [8] uses the advantage of using the two extra pull- up and two extra pull-down transistorNMOS1n sleep mode either in OFF state or in ON state. NMOS1nce the dual sleep portion can be made common to all logic circuitry, less number of transistorNMOS1s needed to apply a certain logic circuit.

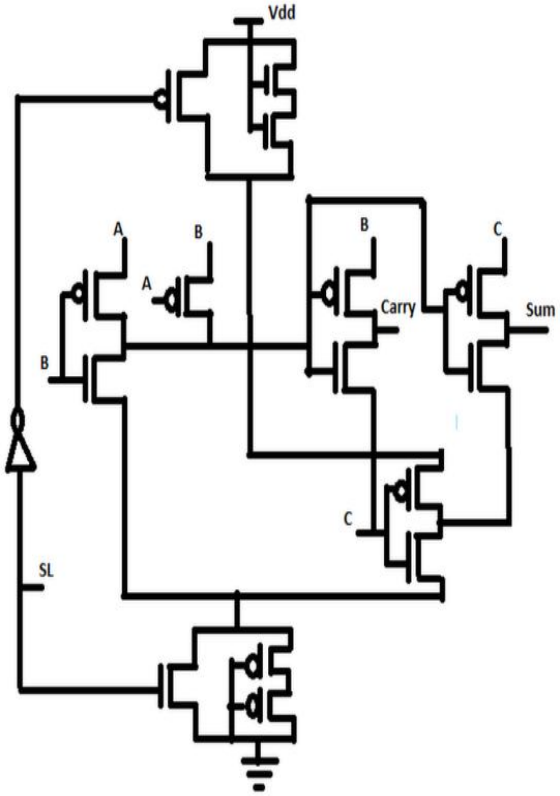

Figure:6 Full Adder With Dual Stack Approch

V. PROPOSED POWER GATING BASED SLEEP TECHNIQUE

There are several benefits of combining stacked sleep transistors. First the magnitude of power supply fluctuations sleep mode during mode transitions will be reduced because these transitions are gradual. Second, while conventional power gating uses a high-threshold device as a sleep transistor to minimize leakage, a stacked sleep structures can achieve the same effect with a normal threshold device.

By using Full adder with dual stack approach as shown in Fig 6. We design BCD ADDER as shown in fig 7.We are giving Virtual supply along with Virtual Ground. By this we can reduce more power compare to previous approach[DSTN].

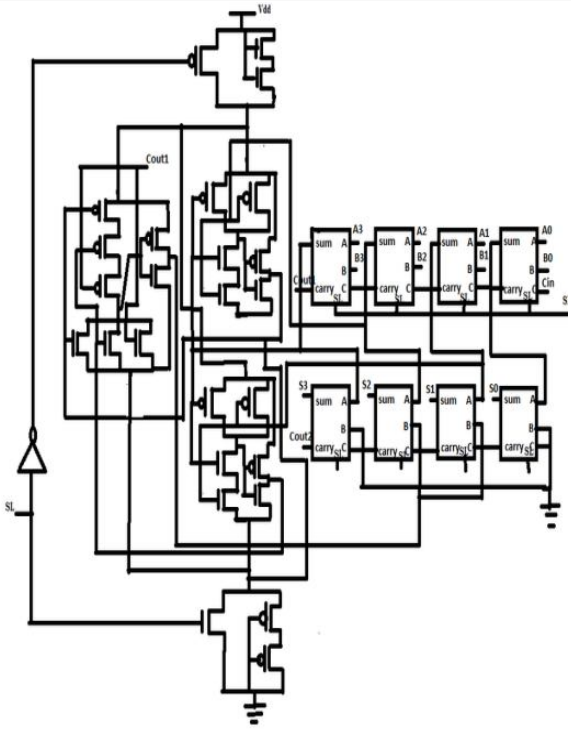

Figure:7 BCD ADDER With Dual Stack approach

VI. RESULTS

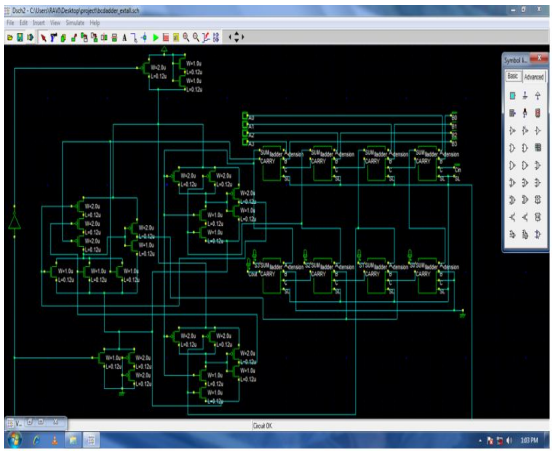

Figure:8 proposed design of 4bit BCD ADDER

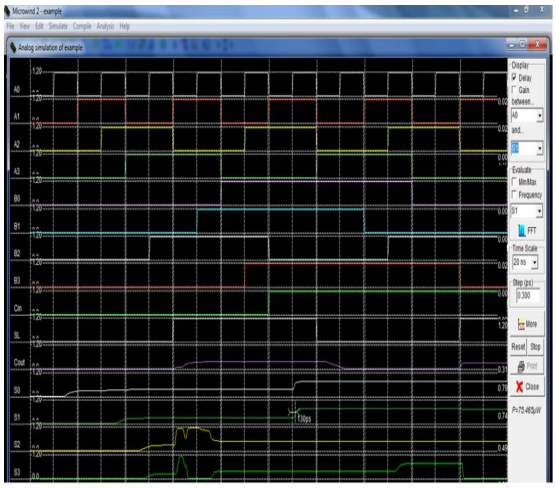

Figure:9 Power characteristics of proposed design

VII. TABULATION

Power Comparison Table

Type	Power consumption
Conventional BCD ADDER	0.189mw
BCD ADDER WITH VIRTUAL GROUND	0.169mw
BCD ADDER WITH DUAL STACK	75.46uw

VIII. CONCLUSION

In nanometer scale CMOS technology, sub threshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. In this paper, we provide novel circuit structure named "Dual stack" as a new remedy for designer in terms of static power and dynamic powers. Unlike the sleep transistor technique, the dual stack technique retains the original state. The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power product. Especially it shows nearly 50-60% of power than the existing normal or conventional flip-flops. So, it can be used for future integrated circuits for power & area Efficiency.

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