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IMPLEMENTATION OF HIGH SPEED-LOW POWER TRUNCATION ERROR TOLERANT ADDER

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Abstract- Now a Days in modern VLSI technology different kinds of errors are invitable. A new type of adder i.e. error tolerant adder(ETA) is proposed to tolerate those errors and to attain low power consumption and high speed performance in DSP systems. In conventional adder circuit, delay is mainly certified to the carry propagation chain along the critical path, from the LSB to MSB. If the carry propagation can be eliminated by the technique proposed in this paper, a great improvement in speed performance and power consumption is achieved. By operating shifting and addition in parallel, the error tolerant adder tree compensates for the truncation errors. To prove the feasibility of the ETA, normal addition operation present in the DFT or DCT algorithm is replaced by the proposed addition arithmetic and the experimental results are shown. In this paper we propose error tolerant Adder (ETA). In the view of DSP applications the ETA is able to case the strict restriction on accuracy, speed performance and power consumption when compared to the conventional Adders, the proposed one provides 76% improvement in power-delay product such a ETA plays a key role in digital signal processing system that can tolerate certain amount of errors.

Keywords- *Adders, digital signal processing (DSP), error tolerance high-speed integrated circuits, low-power design, VLSI, discrete cosine transform, distributed arithmetic, and XOR gate.*

I. INTRODUCTION

In conventional digital VLSI design, one usually assumes that a usable circuit/system should always provide definite and accurate results. But in fact, such perfect operations are seldom needed in our non digital worldly experiences. The world accepts "analog computation," which generates "good enough" results rather than totally accurate results The data processed by many digital systems may already contain errors. In many applications, such as a communication system, the analog signal coming from the outside world must first be sampled before being converted to digital data.

The digital data are then processed and transmitted in a noisy channel before converting back to an analog signal. During this process, errors may occur anywhere. Furthermore, due to the advances in transistor size scaling, factors such as noise and process variations which are previously insignificant are becoming important in today's digital IC design. Based on the characteristic of digital VLSI design, some novel concepts and design techniques have been proposed.

The concept of error tolerance (ET) and the PCMOS technology are two of them. According to the definition, a circuit is error tolerant if: 1) it contains defects that cause internal and may cause external errors and 2) the system that incorporates this circuit produces acceptable results. The "imperfect" attribute seems to be not appealing. However, the need for the error-tolerant circuit was foretold in the 2003 International Technology Roadmap for Semiconductors (ITRS). To deal with error-tolerant problems, some truncated adders/multipliers have been reported but are not able to perform well in either its speed, power, area, or accuracy .The" flagged prefixed adder" performs better than the non flagged version with a 1.3% speed enhancement but at the expense of 2% extra silicon area. As for the "low-error area-efficient fixed-width multipliers" it may have an area improvement of 46.67% but has average error reaching 12.4%. Of course, not all digital systems can engage the error-tolerant concept. In digital systems such as control systems, the correctness of the output signal is extremely important, and this denies the use of the error tolerant circuit. However, for many digital signal processing (DSP) systems that process signals relating to human senses such as hearing, sight, smell, and touch, e.g., the image processing and speech processing systems, the error-tolerant circuits may be applicable.

II. ERROR TOLERANT ADDER

Need for Error-Tolerant Adder:

Increasingly huge data sets and the need for instant response require the adder to be large and fast. The traditional ripple-carry adder (RCA) is therefore no longer suitable for large adders because of its low-speed performance. Many different types of fast adders, such as the carry-skip adder (CSK), carry-select adder (CSL), and carry-look-ahead adder (CLA) have been developed.

Also, there are many low-power adder design techniques that have been proposed. However, there are always trade-offs between speed and power. The error-tolerant design can be a potential solution to this problem. By sacrificing some accuracy, the ETA can attain great improvement in both the power consumption and speed performance.

Error Tolerant Addition:
The definitions of some commonly used terminologies in Error Tolerant Addition shown as follows.

• Overall error (OE): OE= , where is the result obtained by the adder, and denotes the correct result (all the results are represented as decimal numbers).
• Accuracy (ACC): In the scenario of the error-tolerant design, the accuracy of an adder is used to indicate how "correct" the output of an adder is for a particular input. It is defined as: ACC= Its value ranges from 0% to 100%.
• Minimum acceptable accuracy (MAA): Although some errors are allowed to exist at the output of an ETA, the accuracy of an acceptable output should be "high enough" (higher than a threshold value) to meet the requirement of the whole system. Minimum acceptable accuracy is just that threshold value. The result obtained whose accuracy is higher than the minimum acceptable accuracy is called acceptable result.
• Acceptance probability (AP): Acceptance probability is the probability that the accuracy of an adder is higher than the minimum acceptable accuracy. It can be expressed as AP=P , with its value ranging from 0 to 1.

Addition Arithmetic:
The input operands into two parts: an accurate part that includes several higher order bits and the inaccurate part that is made up of the remaining lower order bits. The length of each part need not necessary be equal. The addition process starts from the middle (joining point of the two parts) toward the two opposite directions simultaneously. In the example of Fig. 1,

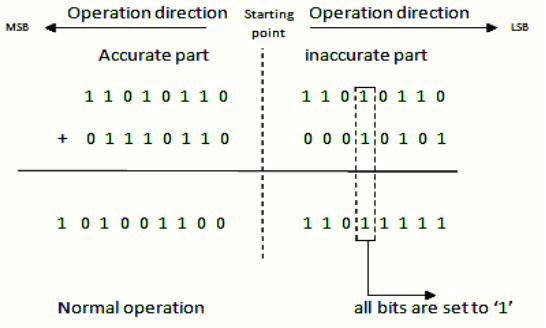

Figure 1. Proposed addition arithmetic

the two 16-bit input operands, A= "1101011011010110" (54998) and B= "0111011000010101" (30229), are divided equally into 8 bits each for the accurate and inaccurate parts. The addition of the higher order bits (accurate part) of the input operands is performed from right to left (LSB to MSB) and normal addition method is applied. This is to preserve its correctness since the higher order bits play a more important role than the lower order bits. The lower order bits of the input operands (inaccurate part) require a special addition mechanism. No carry signal will be generated or taken in at any bit position to eliminate the carry propagation path. To minimize the overall error due to the elimination of the carry chain, a special strategy is adapted, and can be described as follow: 1) check every bit position from left to right (MSB to LSB); 2) if both input bits are "0" or different, normal one-bit addition is performed and the operation proceeds to next bit position; 3) if both input bits are "1," the checking process stopped and from this bit onward, all sum bits to the right are set to "1." The addition mechanism described can be easily understood from the example given in Fig. 1 with a final result of "10100110011011111" (85215). The example given in Fig. 1 should actually yield "10100110011101011" (85227) if normal arithmetic has been applied. The overall error generated can be computed as OE=85227-85215=12.The accuracy of the adder with respect to these two input operands is ACC=(1-12/85227) . By eliminating the carry propagation path in the inaccurate part and performing the addition in two separate parts simultaneously, the overall delay time is greatly reduced, so is the power consumption.

PROPOSED METHOD
The error tolerant adder consists of two parts: an accurate part and inaccurate part. Here a 32-bit adder is used as an example for our illustration of the design methodology and circuit implementation of an ETA.

Dividing Approach of the Adder
The first step of designing a proposed ETA is to divide the adder into two parts in a specific manner. The dividing strategy is based on a guess-and-verify stratagem, depending on the requirements, such as accuracy, speed, and power. First, we define the delay of the proposed adder as Td=max(Th,Tl), where Th is the delay in the accurate part and Tl is the delay in the inaccurate part. With the proper dividing strategy, we can make Th approximately equal to Tl and hence achieve an optimal time delay.

With this partition method defined, we then check whether the accuracy performance of the adder meets the requirements preset by designer customer. This can be checked very quickly via some software programs. For example, for a specific application, we require the minimum acceptable accuracy to be 95% and the acceptance probability to be 98%. The proposed partition method must therefore have at least 98% of all possible inputs reaching an accuracy of better than 95%. If this requirement is not met,

then one bit should be shifted from the inaccurate part to the accurate part and have the checking process repeated. Also, due to the simplified circuit structure and the elimination of switching activities in the inaccurate part, putting more bits in this part yields more power saving. Having considered the above, we divided the 32-bit adder by putting 12 bits in the accurate part and 20 bits in the inaccurate part.

III. RELATIONSHIPS BETWEEN MINIMUM ACCEPTABLE ACCURACY:

Acceptance Probability, Dividing Strategy, and Size of Adder The accuracy of the adder is closely related to the input pattern. Assume that the input of an adder is random; there exists a probability that we can obtain an acceptable result (i.e., the acceptance probability). The accuracy attribute of an ETA is determined by the dividing strategy and size of adder. In this subsection, the relationships between the minimum acceptable accuracy, the acceptance probability, the dividing strategy, and the size of adder are investigated.

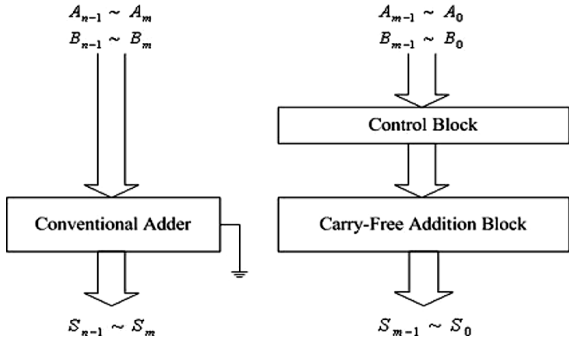

Figure 2:Block diagram of Error tolerant adder

We first consider the extreme situation where we accept only the perfectly correct result. The minimum acceptable accuracy in this "perfect" situation is 100%. According to the proposed addition arithmetic, we can obtain correct results only when the two input bits on every position in the inaccurate part are not equal to "1" at the same time. Wecan therefore derive an equation to calculate the acceptance probability associated with the proposed ETA with different bit sizes and dividing strategies. This equation is given as follows where the total number of bits is in the input operand (also regarded as the size of the adder) and is the number of bits in the inaccurate part (which is indicating the dividing strategy). In situations where the requirement on accuracy can be somewhat relaxed are investigated, the result will be different. C program is engaged to simulate a 16-bit adder that had adopted the proposed addition mechanism. As modern VLSI technology advances, the size of the adder has to increase to cater to the application need. The trend of the accuracy performance of an ETA is therefore investigated in Fig. 2. The five curves are associated with different minimum acceptable accuracies, 95%, 96%, 97%, 98%, and 99%, respectively. Note that all adders follow the same dividing strategy whereby the inaccurate part is three times larger than that of the accurate part. Since small numbers will be calculated at the inaccurate part of the adder, the proposed ETA is best suited for large input patterns.

The block diagram of the Error Tolerant adder that adapts to our proposed addition arithmetic is shown in Fig. 2. This most straightforward structure consists of two parts: an accurate part and an inaccurate part. The accurate part is constructed using conventional adder such as the Ripple- Carry Adder (RCA). The carry-in of this accurate part adder is connected to ground. The inaccurate part constitutes two blocks: a carry-free addition block and a control block. The control block is used to generate the control signals to determine the working mode of the carry-free addition block. In addition, the Least Significant Bit (LSB) of the multiplier (bit B(0)) is used as control bit P for both accurate part and inaccurate part of the proposed adder. For B(0) is one, the adder cells performs normal addition operation. For B(0) equals to zero, the adder cells are brought into OFF state with NMOS and PMOS transistor driven by P brought into open state and the line from supply to ground is cut off , thus minimizing leakage power dissipation. Based on the proposed methodology, an 8-bit Error tolerant adder is designed by considering 4 bits in accurate part and 4 bits in inaccurate part.

A. Design of the accurate part:
In our proposed 32-bit ETA, the inaccurate part has 20 bits as opposed to the 12 bits used in the accurate part. The overall delay is determined by the inaccurate part, and so the accurate part need not be a fast adder. The ripple-carry adder, which is the most power-saving conventional adder, The Ripple Carry Adder, being the simplest one, uses the least hardware circuitry when compared to all other traditional adder circuits in use is show in fig 3.The delay of the ripple Carry adder increases linearly with the number of bits with a worst case delay of O(n).This worst case delay makes it slow when large bit sizes are used.

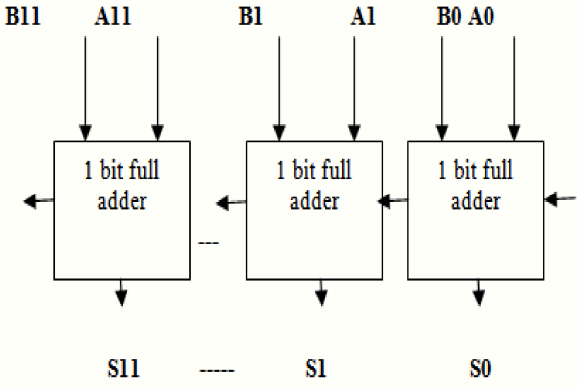

Fig. 3: Implementation of accurate part modified 12-bit ripple carry adder.

B. Design of the inaccurate part:

The inaccurate part consist of 20 bits and it is the most essential section in the proposed ETA as it determines the accuracy, speed performance, and power consumption of the adder. The inaccurate part consists of two blocks: the carry free addition block and the control block. The function of the control block is to detect the first bit position when both input bits are "1," and to set the control signal o n this position as well as those on its right to high. It is made up of 20 control signal generating cells (CSGCs) and each cell generates a control signal for the modified XOR gate at the corresponding bit position in the carry-free addition block. Two types o f CSGC, labeled as type I and II are designed, and the schematic implementations of these two types of CSGC are provided.

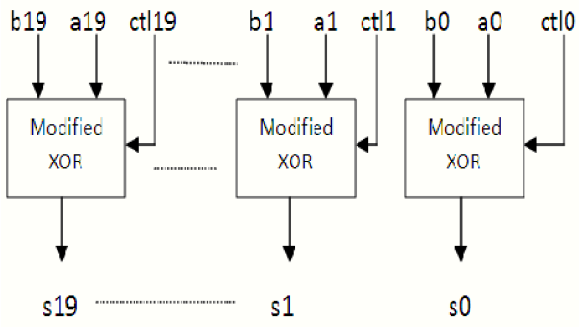

Fig 4: Carry -free addition block: Overall architecture

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C: Carry free addition block:

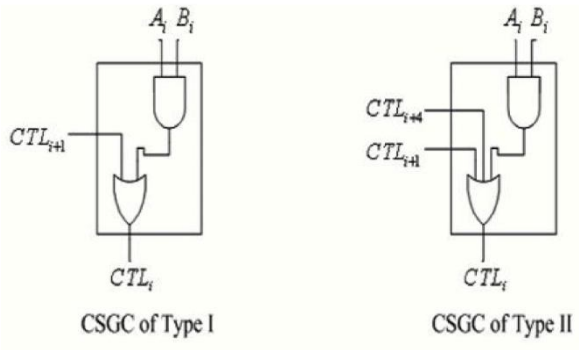

Fig 5: Graphical implementations of CSGC

The carry-free addition block is made up of 20 modified XOR gates, and each of which is used to generate a sum bit. The block diagram of the carry-free addition block and the schematic implementation of the modified XOR gate are XOR gate is designed by using the CMOS logic. It consists of three inputs namely A, B and CTL. CTL is the control signal coming from the control block and is used to set the operational mode of the circuit.

When CTL=0, leaving the circuit to operate in the normal XOR mode. When CTL=1, connecting the output node to VDD, and hence setting the sum output to "1." Hence The novel adder is designed. To prove the feasibility of the ETA, normal addition operation present in the DFT or DCT algorithm can be replaced by the proposed addition arithmetic.

IV.ARCHITECTURE OF THE 1-D 8-POINT DFT OR DCT:

The1-D 8-point DFT or DCT architecture can be constructed using a DA-Butterfly-Matrix that includ es two DA even processing elements (DAEs), a DA odd processing element DAO) and 12 adders/subtractions, and 8 ETAs.

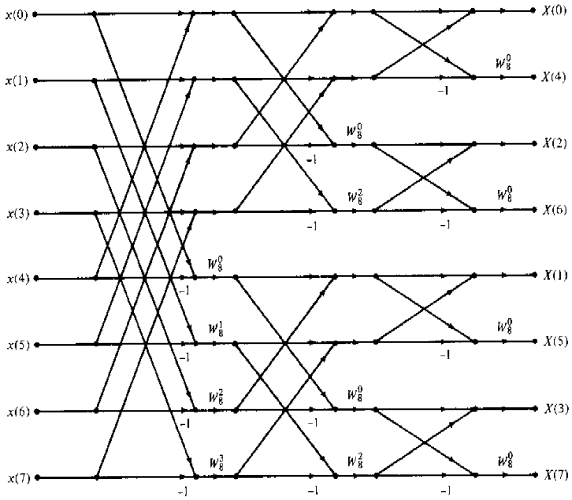

Fig 6.1: Carry-free addition block: Overall architecture.

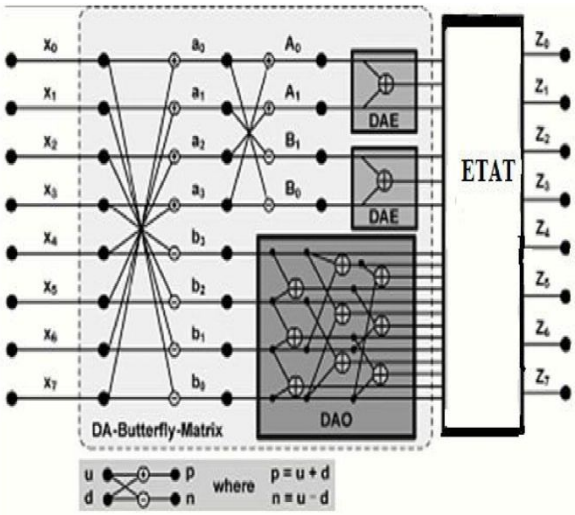

Fig 6.2: Architecture of the 1-D 8-point DFT OR DCT.

V. EXPERIMENTAL RESULTS AND COMPARISON:

To demonstrate the advantages of the proposed ETA, we simulated the ETA along with four types of conventional adders, i.e., the RCA,CSLA by using XILINX 9.2 using VERILOG HDL code and simulated using modelsim 6.5e To evaluate the efficiency of the proposed architecture,

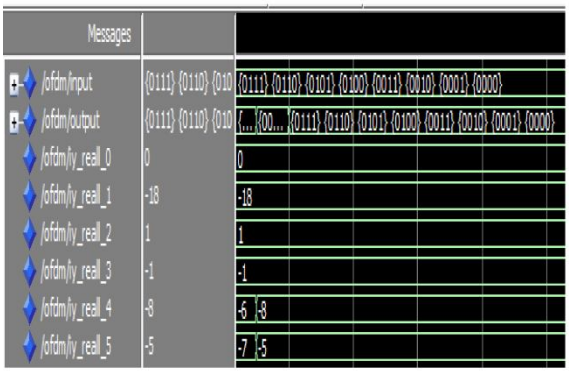

Fig7. simulation wave from for Error Tolerant adder.

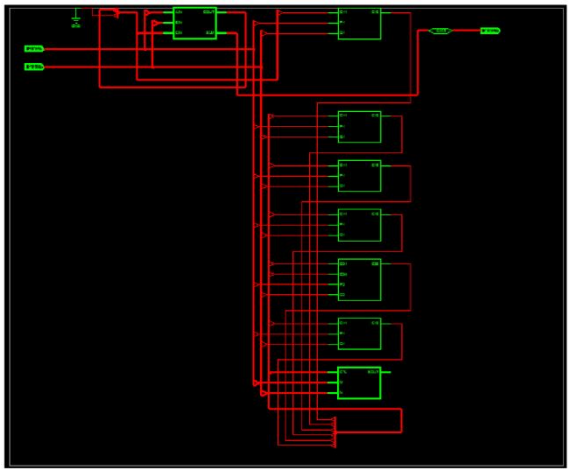

Figure 7.1 RTL view of ETA

Fig 7.2 Synthesis Design Summary of Error Tolerant Adder.

TABLE 1
POWER AND AREA RESULTS

Type	Power (mw)	Delay (ns)	No. of Transistor
RCA	30	10 .25	96
CSLA	31	13 .00	140
ETA	23	6.250	110

VI. APPLICATION OF ERROR TOLERANT ADDER IN DSP.

In image processing and many other DSP applications, fast Fourier transformation (FFT or DFT) is a very important function. The computational process of FFT or DFT involves a large number of additions and multiplications. It is therefore a good platform for embedding our proposed ETA. To prove the feasibility of the ETA, we replaced all the common additions involved in a normal FFT Or DFT algorithm with our proposed addition arithmetic. As we all know, a digital image is represented by a matrix in a DSP system, and each element of the matrix represents the color of one pixel of the image. To compare the quality of images

Fig8(a) Image processed with conventional adder

Processed by both the conventional FFT or DFT and the inaccurate FFT that had incorporated our proposed ETA, we devised the following experiment. An image was first translated to a matrix form and sent through a standard system that made used of normal FFT and normal reverse FFT. The matrix output of this system was then transformed back to an image and presented in Fig. 8. The matrix of the same image was also processed in a system that used the inaccurate FFT and inaccurate reverse FFT, where both FFTs had incorporated the 32-bit ETA described in Section III, with the processed image given in Fig.8(b).

Fig. 8(b) Image processed with the proposed ETA.

Although the two resultant matrices of the same image were different, the two pictures obtained (see Fig.8) look almost the same. Fig. 8(b) is slightly darker and contains horizontal bands of different shades of gray. With a MAA setting of 95%, the AP of the matrix representation of Fig.8(b). Is 98.3% as compared to the matrix representation of Fig8(a).The comparison between the two images in Fig. 8 shows that the quality loss to the image using our proposed ETA is negligible and can be completely tolerated by human eyes. These simulation results have proven the practicability of the ETA proposed.

VII. CONCLUSION:

In this paper, the concept of error tolerance is introduced in VLSI design. A novel type of adder, the error-tolerant adder, which trades certain amount of accuracy for significant power saving and performance improvement, is proposed. By eliminating the carry propagation path in the inaccurate part and performing the addition in two separate parts simultaneously, the overall delay time is greatly reduced . Then the ETA is applied to the 1 -D 8point DFT or DCT. The normal addition operation is replaced by the proposed addition arithmetic. The proposed ETA is well in terms of power and area when compared to the conventional ripple carry adder RCA). In future modification can be made by replacing the XOR gate using CMOS logic by Transmission gates where he number of transistors can be reduced. Therefore transistor gate counts will be reduce so the area is also been reduced.

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