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DESIGN OF LOW POWER AND HIGH PERFORMANCE PULSE TRIGGERED FLIP FLOP USING CONDITIONAL PULSE ENHANCEMENT METHOD

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Abstract- In this paper, a novel low-power high performance pulse-triggered flip-flop using conditional pulse enhancement design method is presented. Our proposed design is Enhanced Pulse Triggered Low-power Flip Flop (EPTLFF). Its design is done by the pulse generation control logic, an AND function, is removed from the critical path to facilitate a faster discharge operation. A simple two-transistor AND gate design is used to reduce the circuit complexity. The EPTLFF avoids unnecessary internal node transitions to reduce power consumption. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving. Various layout simulation results comparison between previously reported design and modified design is based on 90nm and 50nm technology. The proposed design features the best power-delay-product performance in five FF designs under comparison. Its maximum power saving compared to the conventional P-FF designs is up to 18.6%.

Keywords- Flip-flop, Low power, Pulse-triggered.

I. INTRODUCTION

Flip-Flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. The digital designs nowadays often adopt intensive pipelining techniques and employ many FF rich modules and also estimated that the power consumption of clock system, which consists of clock distribution networks and storage elements is as high as 20% to 45% of the total system power [1]. Pulse triggered flip flop (P-FF) is considered as a popular alternative to the conventional master slave based FF in the application of high speed operations. Besides the speed advantage, its circuit simplicity is also beneficial to lowering the power consumption of the clock tree system. A P-FF consists of a pulse generator for generating strobe signals and a latch for data storage. Since triggering pulses generated on the transition edges of the clock signal are very narrow in pulse width, the latch acts like an edge-triggered FF. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master slave configuration, and is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. P-FFs are thus less sensitive to clock jitter. The pulse generation circuitry requires delicate pulse width control in the face of process variation and the configuration of pulse clock distribution network [13]. Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit. In an implicit type P-FF, the pulse generator is a built in logic of the latch design, and no explicit pulse signals are generated. In an explicit-type P-FF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. This is because the former merely controls the

discharging path while the latter needs to physically generate a pulse train. Implicit-type designs, however, face a lengthened discharging path in latch design, which leads to inferior timing characteristics. The situation deteriorates further when low power techniques such as conditional capture, conditional precharge, conditional discharge, or conditional data mapping are applied. In this paper a Enhanced Pulse Triggered Low-power Flip Flop(EPTLFF) is proposed that has reduced the number of transistors and avoids unnecessary internal node transitions, as well as reduce power consumption and delay compared to conventional P-FF.

II. CONVENTIONAL P-FF DESIGNS

Some conventional implicit-type P-FF designs, which are used as the reference designs in later performance comparisons, are reviewed.

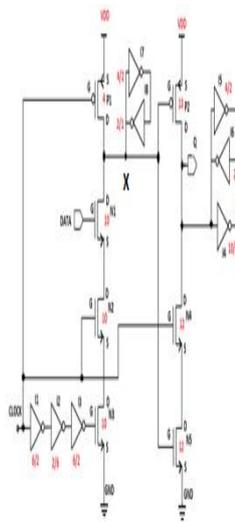


Fig 1(a). ip-DCO

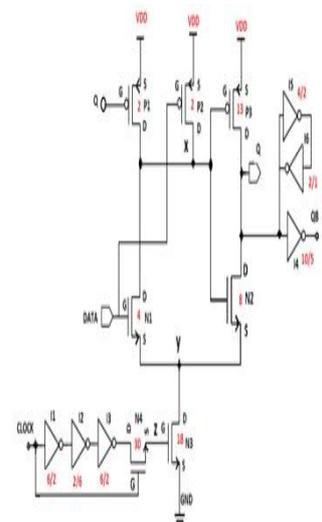


Fig 1(b). MHLLF

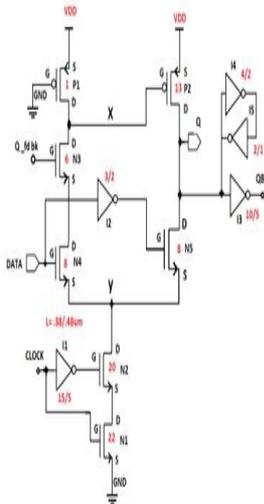


Fig 1(c). SCCER

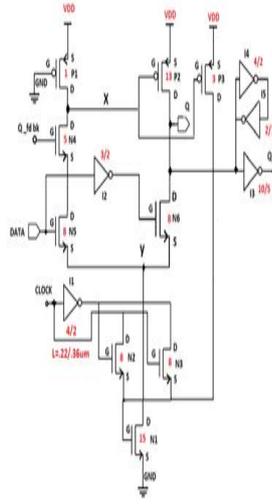


Fig 1(d).PTL based Pulse- Triggered Flip-Flop

A. ip-DCO : Implicit pulse data close to output

Fig. 1(a) shows the IP-DCO, it consists of pulse generator and semi dynamic latch structure [3]. A state-of-the-art P-FF design, named ip-DCO, is given in Fig 1(a) [3]. It contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node X. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, NMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node X controls two larger MOS transistors (P2 and N5). The large capacitive load to node X causes speed and power performance degradation.

B. MHLLF: Multi Hybrid Latch Level Flip-flop

Fig. 1(b) shows an improved P-FF design, named MHLLF, by employing a static latch structure presented in [6]. Node x is no longer precharged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node X level at high when Q is zero. This design eliminates the unnecessary discharging problem at node X. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" to "1" transitions because node X is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node X becomes floating when output Q and input data both equal to "1". Extra DC power emerges if node X is drifted from an intact "1". The other problem is that node X controls two larger MOS transistors (P2 and N5). The large capacitive load to node X causes speed and power performance degradation.

C. SCCER: SINGLE- ENDED CONDITIONAL CAPTURE ENERGY RECOVERY

Fig. 1(c) shows a refined low power P-FF design named SCCER using a conditional discharged technique [4], [7]. In this design, the keeper logic (back-to-back inverters I7 and I8 in Fig. 1(a)) is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node X [7]. The discharge path contains NMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node X, an extra NMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node X is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

D. PTL based Pulse-Triggered Flip-Flop (P-FF):

Fig.1 (d) shows pass transistor logic based on the Pulse-Triggered Flip-Flop, which adopts two measures to overcome the problems associated with P-FF Fig1(a),(b),(c) designs. The first one is reducing the number of NMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." Refer to Fig. 1(d), the upper part latch design is similar to the one employed in SCCER design [7]. As opposed to the transistor stacking design in Fig. 1(a) and (c), transistor N2 is removed from the discharging path. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate [8], [9] to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time.

When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node Z can be reduced due to a diminished voltage swing. Unlike the MHLLF design [6], where the discharge control signal is driven by a single transistor, parallel conduction of two NMOS transistors (N2 and N3) speeds up the operations of pulse generation. With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N5 can also be reduced.

III. PROPOSED EPTLFF

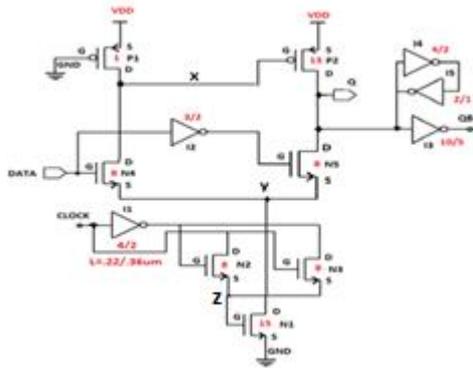


Fig 2. Schematic of the proposed EPTLFF design

Fig. 2 shows our proposed design Enhanced Pulse Triggered Low-power Flip Flop (EPTLFF), for high-speed operation of data storage and a popular alternative to Master slave flip-flop. The enhanced pulse triggered low-power flip flop (EPTLFF) with pulse control scheme consists of pulse generator for generating Strobe signals and a latch for data storage. It reduces the number of transistors stacked in the discharging path and also reduces the overall switching delay. Refer to Fig. 2, the upper part latch design and lower part enhanced pulse generation. This particular clock pulse is used to a two-input pass transistor logic, N2, N3 a two-input pass transistor logic based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node Z can be reduced due to a diminished voltage swing. Where the discharge control signal is driven by a single transistor, parallel conduction of two NMOS transistors (N2 and N3) speeds up the operations of pulse generation. In this design reduced the discharging path X, avoids unnecessary internal node transitions to reduce power consumption and delay.

IV. SIMULATION RESULTS

The operating condition used in simulations is 500 MHz/1.0V. Since pulse width design is crucial to the correctness of data capturing as well as the power consumption, the pulse generator logic in all designs are first sized to function properly across process variation. All designs are further optimized subject to the tradeoffs between power and D-to-Q delay, i.e., minimizing the product of the two terms. The target technology is the UMC 90-nm CMOS & UMC 50-nm CMOS process is used. The simulation results are schematic circuits designed in Tanner Tool as

shown in Fig. 3(a) IP-DCO, Fig. 3(b) MHLFF, Fig. 3(c) SCCER, Fig. 3(d) PTL based P-FF, Fig. 3(e) EPTLFF, Fig. 3(f) EPTLFF symbol. The layout design in Soft Ware Microwind tool is shown in Fig. 4(a) IP-DCO, Fig. 4(b) MHLFF, Fig. 4(c) SCCER, Fig. 4(d) PTL based P-FF & Fig. 4(e) EPTLFF. The layout simulation window appears with inputs and output as shown in Fig. 5(a) IP-DCO, Fig. 5(b) MHLFF, Fig. 5(c) SCCER, Fig. 5(d) PTL based P-FF & Fig. 5(e), the power consumption is also shown on the right bottom portion of the window. The EPTLFF simulation output Window using tanner Tool as shown in Fig.5(f).

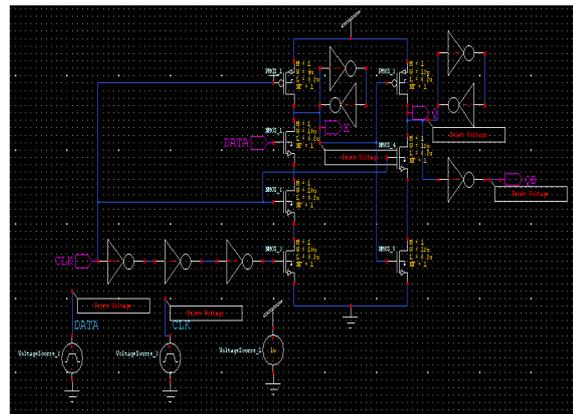


Fig 3(a). ip-DCO Schematic in Tanner Tool

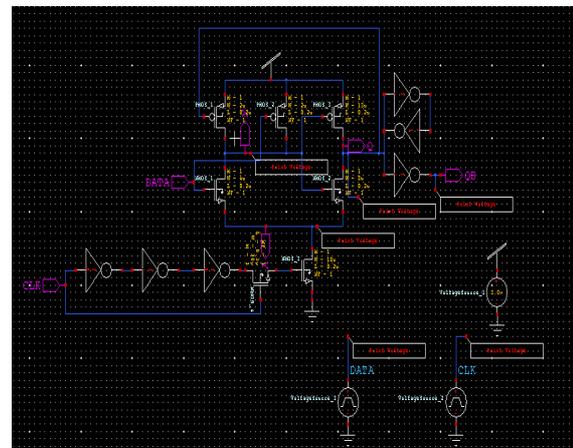


Fig 3(b). MHLFF Schematic in Tanner Tool

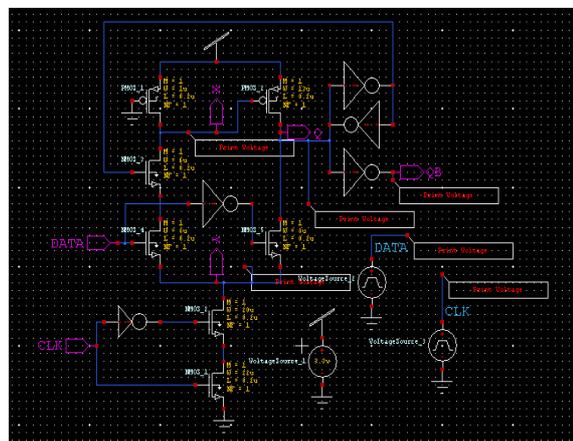


Fig 3(c). SCCER Schematic in Tanner Tool

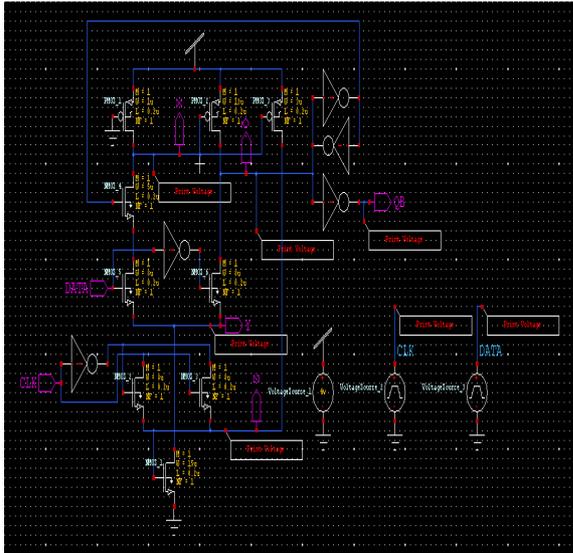


Fig 3(d). PTL based P-FF Schematic in Tanner Tool

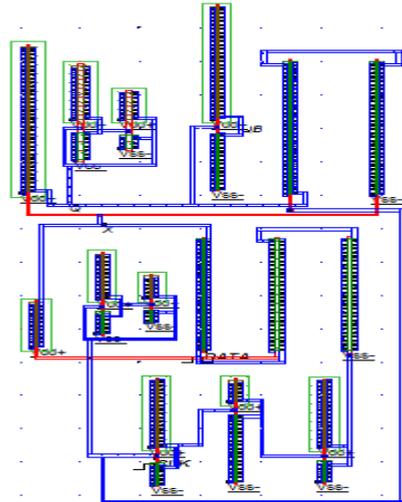


Fig 4(a). ip-DCO layout in Soft Ware Microwind tool

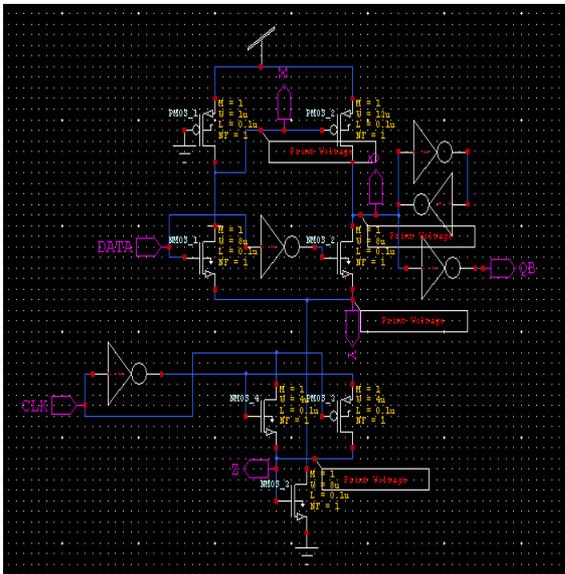


Fig 3(e). Proposed EPTLFF Schematic in Tanner Tool

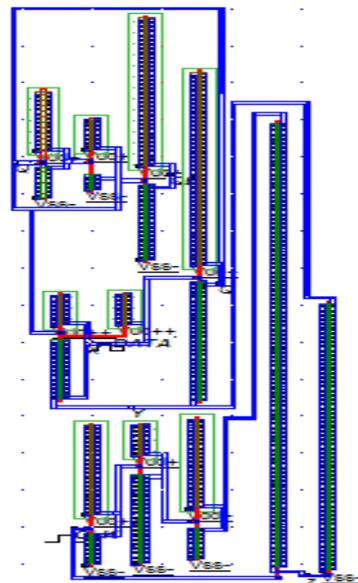


Fig 4(b). MHLLF layout in Soft Ware Microwind tool

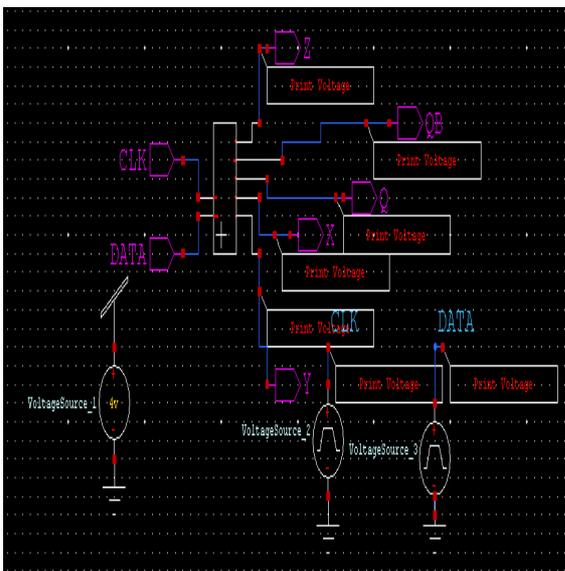


Fig 1(f). Proposed EPTLFF Symbol in Tanner Tool

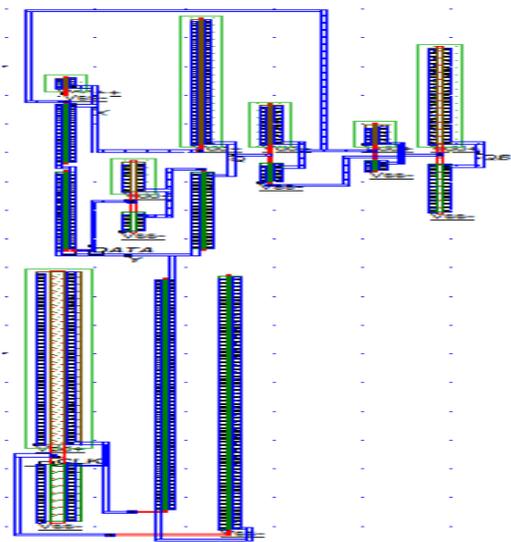


Fig 4(c). SCCER in Soft Ware Microwind tool

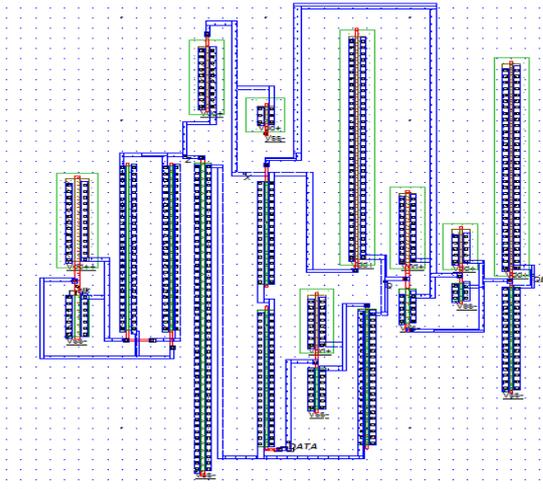


Fig 4(d). PTL based P-FF layout in Soft Ware Microwind tool

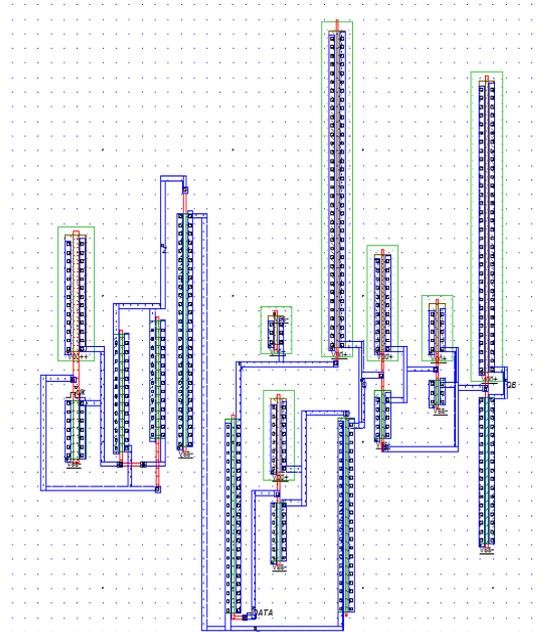


Fig 4(e). Proposed EPTLFF layout in Software Microwind tool

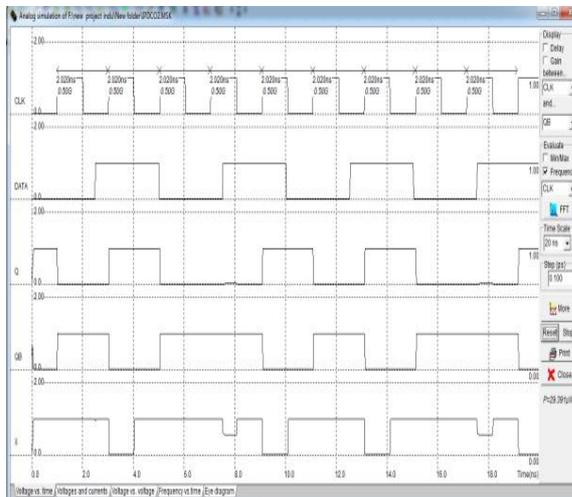


Fig 5(a). Power consumed by ip-DCO in Soft Ware Microwind tool

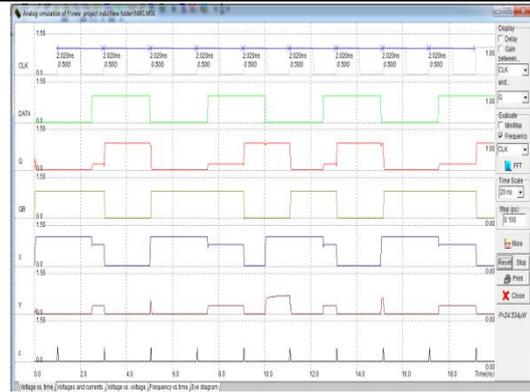


Fig 5(b). Power consumed MHLFF in Soft Ware Microwind tool

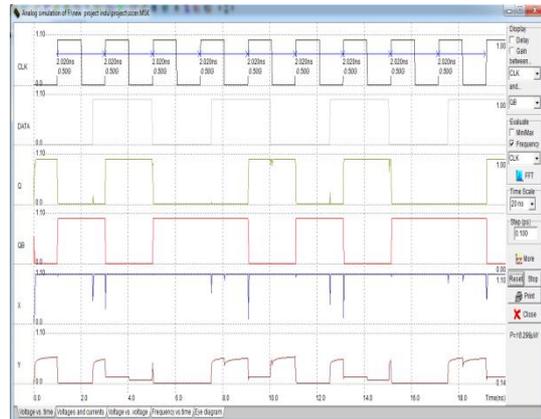


Fig 5(c). Power consumed by SCCER in Soft Ware Microwind tool

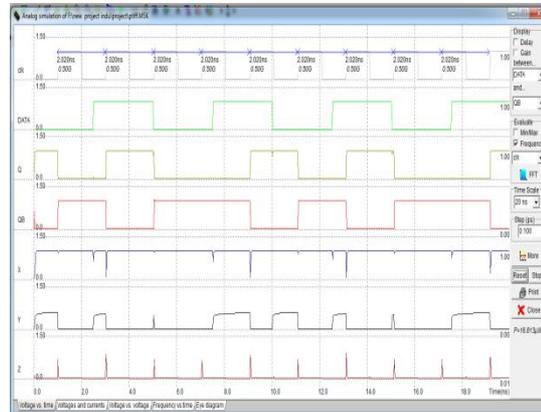


Fig 5(d). Power consumed by PTL based P-FF in Soft Ware Microwind tool

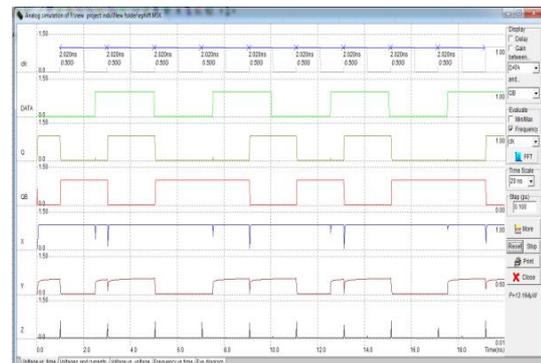


Fig 5(e). Power consumed by EPTLFF in Soft Ware Microwind tool

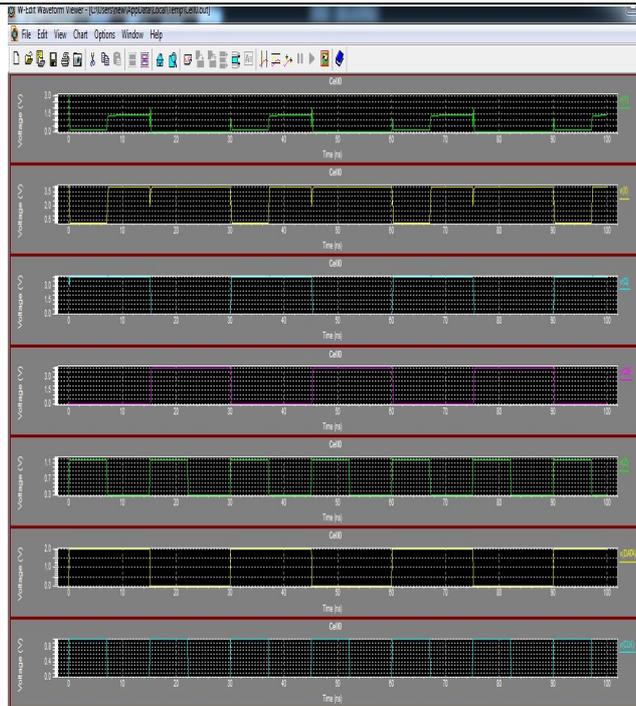


Fig 5(f). Power consumed by PROPOSED EPTLFF in Tanner Tool

V. RESULT COMPARISON

The comparison of result summarizes some important performance indexes of these P-FF designs as shown

in Table1. These include transistor count, Area, D to Q Delay & Power in UMC 90-nm & UMC 50-nm technology.

Table 1. Comparison of various P-FF designs

P-FF	Ip-DCO	MHLLF	SCCER	PTL based P-FF	EPTLFF
No. of transistors	23	19	17	19	17
Area μm^2	414	451.6	610.5	394.5	376
D TO Q Delay(ps)	410	360	400	380	340
Propagation delay (CLK to Q)ps	457	155	134	150	134
Avg. Power (μW) Using UMC CMOS-90nm Technology.(μW).	29.39	24.53	18.3	16.82	13.16
Average Power(μW)using UMC CMOS-50nm Technology.(μW).	8	7.2	5.47	4.72	2.86

VI. CONCLUSION

In this paper, the various Flip Flop designs like, ip-DCO, MHLFF, SCCER, PTL based P-FF & Proposed EPTLFF are discussed. The enhanced pulse triggered low-power FF (EPTLFF) design successfully reduces the number of transistors stacked along the discharging path by incorporating a simple two-transistor AND gate logic. The EPTLFF avoids unnecessary internal node transitions to reduce power consumption. These P-FFs are designed in Tanner tool & Soft Ware Microwind tools and the result waveforms are also discussed. Simulation results indicate that the proposed design excels rival designs in performance indexes such as power, D to Q delay. The comparisons of five P-FF are shown in Table 1 to verify the designed methods using UMC CMOS 90-nm & UMC CMOS 50-nm technology. With all these results proposed EPTLFF speed performance and power are better than ip-DCO and MHLFF and SCCER and PTL P-FF designs.

REFERENCES

- [1] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," *IEEE J. Solid-State Circuits*, vol.33, no. 5, pp. 807–811, May 1998.
- [2] A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, "A novel high speed sense-amplifier-based flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 11, pp. 1266–1274, Nov. 2005.
- [3] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors," in *Proc. ISPLED*, 2001, pp. 207–212.
- [4] P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and low power conditional discharge flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 5, pp. 477–484, May 2004.
- [5] C. K. Teh, M. Hamada, T. Fujita, H. Hara, N. Ikumi, and Y. Oowaki, "Conditional data mapping flip-flops for low-power and high-performance systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Systems*, vol. 14, pp. 1379–1383, Dec. 2006.
- [6] S. H. Rasouli, A. Khademzadeh, A. Afzali-Kusha, and M. Nourani, "Lowpower single- and double-edge-triggered flip-flops for high speed applications," *Proc. Inst. Electr. Eng.—Circuits Devices Syst.*, vol. 152, no. 2, pp. 118–122, Apr. 2005.
- [7] H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra low power clocking scheme using energy recovery and clock gating," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, pp. 33–44, Jan. 2009.
- [8] P. Zhao, J. McNeely, W. Kaung, N. Wang, and Z. Wang, "Design of sequential elements for low power clocking system," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, to be published.
- [9] Y.-H. Shu, S. Tenqchen, M.-C. Sun, and W.-S. Feng, "XNOR-based double-edge-triggered flip-flop for two-phase pipelines," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 2, pp.138–142, Feb. 2006.

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