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FAST LOW POWER FREQUENCY SYNTHESIS APPLICATIONS BY USING A DCVSL DELAY CELL

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Abstract- In this paper, we proposed two new structures for differential cascode voltage switch logic (DCVSL) pull-up stage. In conventional DCVSL structure these lies a drawback i.e. low-to-high propagation delay is larger than high-to-low propagation delay which could be reduced by using DCVSL-R. Using resistors in DCVSL-R structure, parasitic effects are coming into picture and it occupies more area on the chip [1]. To minimize these problems we propose a new Ultra Low Power Diode (ULPD) structures in place of resistors. This provides the minimum parasitic effects and occupies less area on the chip. Second one uses Complementary Pass Transistor Logic (CPTL) structure, which provides complementary outputs. This is an alternate circuit for conventional DCVSL structure. The performances of the proposed circuits are examined using cadence and model parameters of a 180nm CMOS process. This simulation result of the two circuits is presented and is compared. These circuits are suitable for VLSI implementation. Secondly, we proposed two new CMOS Schmitt trigger circuits. These Schmitt trigger circuits are evaluated both analytically and numerically with the sources from proposed ULPD ring oscillators. The hysteresis curves of the circuits are presented. The Schmitt triggers introduced here are most suitable for high speed applications. The proposed circuits havebeen designed in TSMC-0.18µm 1.8v CMOS technology and analyzed using spectre from cadence Design systems at 50MHz and 103MHz.

Keywords- *DCVSL,CPTL, ULPD.*

I. INTRODUCTION

As handheld and wireless devices become a central part of everyday life, low-power circuit techniques are becoming increasingly important for enhanced battery life. The frequency synthesizer is one of the key building blocks of any wireless transceiver system. Since it is active during both transmit and receive modes, the frequency synthesizer consumes a significant fraction of the overall power.

The key power-hungry circuits in a frequency synthesizer are the voltage-controlled oscillator (VCO) and the frequency dividers [1], especially the programmable dividers that operate at the RF frequency. Along with frequency of operation and technology speed, the circuit design technique of the frequency dividers is key in determining their and their driving buffer's power consumption. Until recently, Current Mode Logic (CML) circuits [2], [3]

In this paper, we explore the Differential Cascode Voltage-Switch Logic (DCVSL) circuit design methodology, and propose an improvement to DCVSL for use in the RF dividers of a frequency synthesizer. The key benefits of DCVSL are its low input capacitance, differential nature and low power consumption. However, DCVSL delay cells have a delay asymmetry; their low-to-high-transition propagation Delay T_{PLH} is inherently larger than their high-to-low-transition propagation delay T_{PHL} .

The outline of this paper is as follows. Section II discusses various circuit topologies and offers DCVSL circuits as a candidate to implement the RF frequency dividers of frequency synthesizers. Section III analyzes the delay behavior of DCVSL inverters and proposes a closed-form model to describe the inherent delay asymmetry of the DCVSL circuits. Then, in Section IV we propose a circuit solution, which we term Differential Cascode Voltage Switch Logic with Resistive-enhancement (DCVSL-R), to overcome this delay asymmetry and reduce T_{PLH} and hence reduce the total propagation delay T_{PLH}+ T_{PHL} . Since DCVSL-R resolves the asymmetric output problem of DCVSL circuits, it can better implement the differential clock signals for the following stages of dividers and ring oscillators. It also features smaller parasitic capacitances in it's input and output nodes, when compared to it's counterparts such as CML and TSPC. The proposed circuit in high-frequency programmable dividers of low-power synthesizers, and in the delay cells of ring oscillators. Section V discusses the implementation of two ring-oscillator-based VCOs in 0.13 m CMOS technology, that utilize DCVSL and DCVSL-R delay cells and demonstrates the performance improvement of the latter through measurements. Then, in Section VI we implement a frequency synthesizer in 0.18 m CMOS technology that uses the proposed DCVSL-R technique in it's RF dual modulus prescaler (DMP). The frequency synthesizer generates 2.4 GHz quadrature outputs and it's measured performance is suitable for low power transceiver applications such as IEEE 802.15.4/ZigBee. We demonstrate that, the DCVSL-R based DMP achieves 40% lower power when compared to other similar reported DMPs that employ other circuit techniques, and decreases the power consumption of the high-frequency buffer that drives it. Section VII concludes this paper.

II. CIRCUIT TECHNIQUES FOR FREQUENCY DIVIDERS

A commonly used circuit technique in the high frequency dividers of wireless radio synthesizers is CML [4], [5]. A CML latch is shown in Fig. 1. CML circuits enable high-speed operation with small signal swing. Their constant DC bias current minimizes switching noise, and their differential nature makes them immune to common-mode noise. However, CML, though high speed, consumes considerable power due to it's DC bias current and has limited headroom due to stacked transistors. Load resistance and bias current values determine the output swing and DC common mode level, putting a lower limit on the bias current value. Moreover, a CML D-flip-flop requires two CML latches of Fig. 1, using fourteen transistors and four resistors for a single flip-flop, resulting in much more area than traditional flops.As an alternative to CML, TSPC circuits implement the frequency dividers of wireless-radio frequency synthesizers [6]–[8]. Fig.2 shows a rising-edge triggered TSPC D-flip-flop. They consume no static power and use fewer transistors. However, they have stacked transistors that present large bias-dependent capacitive loading.

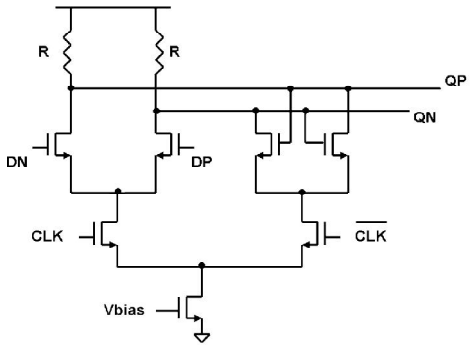

Fig. 1. Schematic of a CML latch.

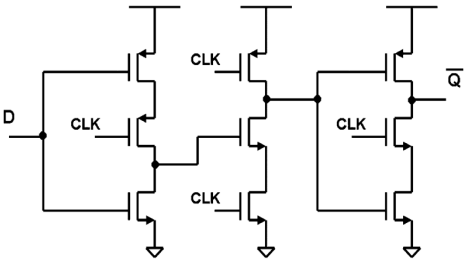

Fig. 2 Schematic of a TSPC D-flip-flop.

In a PLL, frequency dividers are driven either by a buffer or directly by the VCO, and VCO architectures are often differential. Single-ended frequency dividers such as TSPC, result in an asymmetrical loading at the VCO output, which leads to mismatch at the LO signals of a transceiver Differential-to-single-ended conversion buffers may also be employed; however, at high frequency these buffers consume large power. [6] uses such a buffer followed by an inverter chain and while the TSPC significantly reduces the dual-modulus-presale (DMP) power, the buffers consume as much power as the DMP. [7] uses a modified version called E-TSPC to avoid stacked transistors. A simple DCVSL inverter is shown in Fig.3.One drawback of this circuit technique occurs while the PMOS load transistors are in latching mode. For a brief period, both PMOS and PMOS transistors in at least one of the differential branches are on at the same time, leading to crowbar current for a short time.

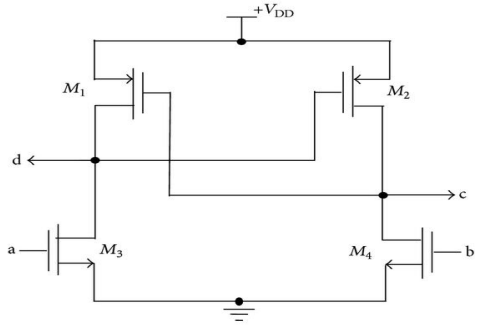

Fig. 3. Schematic of a DCVSL inverter.

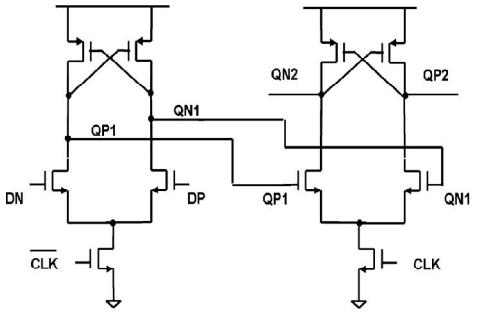

Fig. 4. Two-clock-phase DCVSL flip-flop.

However, this transition period also smoothens the instantaneous current switching of these logic gates and generates less switching supply noise compared to hard-switching, static, full-CMOS logic. Several DCVSL based flip-flops are discussed and compared in. The D-flip-flop (DFF) of Fig. 4 shows the best candidate for high speed applications due to its simplicity and low transistor count. By avoiding recharge schemes, additional PMOS clock transistors are eliminated. Due to its small number of transistors, this flip-flop is fast.

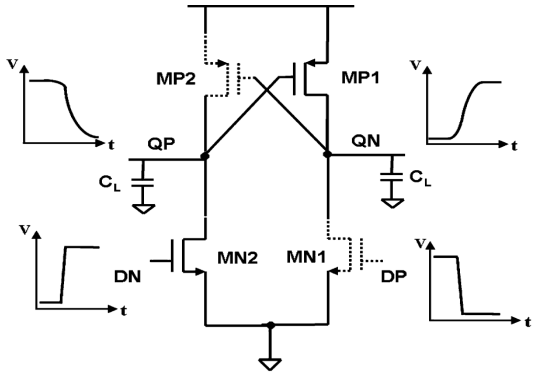

Fig. 5. DCVSL inverter setup for transient delay analysis.

III. DELAY ANALYSIS FOR DCVSLCIRCUITS

Digital circuits' speed is characterized by their propagation delays, i.e., the low-to-high switching propagation delay T_{PLH} (the delay from the input falling from logic high to low to the output rising from logic low to high) and the high-to-low switching propagation delay T_{PHL}To understand the transient behavior of DCVSL circuits, we analyze the propagation delay of a simple DCVSL inverter. where α is a unit less technology dependent parameter for a given transistor length and is derived from simulations as described in. V_{DSO} And I_{DO} are the drain saturation voltages and drain current respectively, of the transistor VGS = VDS = VDD; and VTH is the threshold Voltage For the target applications of the DCVSL cells in this work we can safely assume that the DCVSL cells are driven by other DCVSL cells with similar delays.

$$T_{tn} = C_L \frac{\mathrm{VDD}}{I_{DOP}} \left(\frac{0.9}{0.8} + \frac{V_{DSOP}}{0.8 \times \mathrm{VDD}} \ln \left(\frac{10 \times \mathrm{VDD}}{e \times \mathrm{VDD}} \right) \right)$$
$$T_{tp} = C_L \frac{\mathrm{VDD}}{I_{DON}} \left(\frac{0.9}{0.8} + \frac{V_{DSON}}{0.8 \times \mathrm{VDD}} \ln \left(\frac{10 \times \mathrm{VDD}}{e \times \mathrm{VDD}} \right) \right) \quad \text{- (1)}$$

Where C_L is the load capacitance; $I_{DOP,}$ V_{DSOP} and $I_{DON,}V_{DSON}$ are the drain currents; and saturation voltages of the PMOS and NMOS transistors of the driving stage, respectively. Moreover ,to derive T_{PHL} Then, the derivation of T_{PHL} of a DCVSL inverter is similar to that of a standard CMOS inverter, and we can use the expression derived in are the ratios of the threshold voltages of NMOS and PMOS transistors to the supply voltage.

$$T_{PHL} = T_{05-HL} - \frac{Ttn}{2} \quad \text{--- (2)}$$

$$T_{05\_HL} = Ttn\left(\frac{v_{TN} + \alpha_N}{1 + \alpha_N} + C_L \frac{VDD}{2I_{DON}}\right) \quad \text{-- (3)}$$

Where and

$$v_{TN} = \frac{V_{THN}}{VDD}, v_{TP} = \frac{V_{THP}}{VDD} \quad \text{--- (4)}$$

To derive T_{PHL} of a DCVSL inverter, Fig. 6(b) shows the case where the QN output is rising. Note thatMP1, the transistor that pulls QN up, is triggered by QP, not DP. In other words, the input signal for the rising output QN, is QP. However, propagation delay T_{PHL} is defined as the delay between the time when the rising output (in this case QN) and the falling input (DP) of the inverter reaches VDD/2. Then, as shown in Fig. 6(b), we can represent T_{PHL} as the summation of two delay components,t_1 and t_2 .

$$T_{PLH} = t_1 + t_2 \quad \text{--- (5)}$$

Where t_1 is determined by the speed of the NMOS pull-down transistor MN2 and is given by (7)

$$t_{1|} = T_{05-HL} - \frac{Ttp}{2}. \quad \text{---(6)}$$

To find 2 t , we approximate QP as a linear ramp, just as we do with the input signals DN and DP when deriving (2), since we assumed that the input and output signals have similar slew rates. Then, we obtain 2 t just like we found PHL T , as shown in Fig. 6(c) where QPA is the linearly approximated QP

$$t_2 = T_{tp}\left(\frac{v_{TP} + \alpha_P}{1 + \alpha_P} + C_L \frac{VDD}{2I_{DOP}}\right) - \frac{T_{tp}}{2} \quad \text{-- (7)}$$

As mentioned earlier, the expressions for T_{PHL} and T_{PLH} (given in (3) to (8)),are derived ignoring the brief current conduction of NMOS transistor (MN1) for T_{PLH} and that of PMOS loads (MP2) for T_{PHL} This assumption results in optimistic delay expressions.

$$T_{PHL} = K_{HL} \times \left[T_{tn}\left(\frac{v_{TN} + \alpha_N}{1 + \alpha_N} + C_L \frac{VDD}{2I_{DON}}\right) - \frac{T_{tn}}{2}\right] \quad \text{-- (8)}$$

This reduction creates an error factor in the delay model that is related to the ―internal configuration ratio (WP/WN assuming same length). Therefore, we propose the following DCVSL equations:

Where

$$T_{PLH} = K_{LH} \times \left[T_{tn}\left(\frac{v_{TN} + \alpha_N}{1 + \alpha_N} + C_L \frac{VDD}{2I_{DON}}\right) - \frac{T_{tp}}{2} + T_{tp}\left(\frac{v_{TP} + \alpha_P}{1 + \alpha_P} + C_L \frac{VDD}{2I_{DOP}}\right) - \frac{T_{tp}}{2}\right] \quad \text{--- (9)}$$

$$K_{HL} = \left(\gamma_N + \frac{\varsigma_N}{(WP/WN)}\right)^{-1}$$

$$K_{LH} = \left(\gamma_P + \frac{\varsigma_P}{(WP/WN)}\right)^{-1} \quad \text{-- (10)\&(11)}$$

Note that P, P. and N. , N. are empirical correction factors obtainable from simulations, and should be constant across transistor sizes and loading conditions for a given technology. Note the T_{PLH} correction factor, K_{LH} , is proportional to (WP/WN), because T_{PLH} strongly depends on the NMOS transistor, for the PMOS pull-up transistor is controlled by the falling output, as explained earlier.

The voltage dependence of the load capacitance should be considered when calculating C_L. For a DCVSL inverter under test (IUT), load capacitance includes the input capacitance of the following fan-out stages; interconnect capacitance of the routing and capacitance due to the PMOS load transistor of the IUT itself. Note that the transition of interest is

from VDD to VDD/2 and from 0 to VDD/2 for falling and rising outputs, respectively. We demonstrated that T_{PLH} is T_{PHL} inherently larger than For the falling output QP, since QN will wait for QP, MP1 will be in saturation while QP falls to VDD/2. For the rising output QN, we can assume that QP will fall enough for MP2 to have before QN begins rising, due to the inherent delay asymmetry of DCVSL. Then, MP2 will be in saturation during the transition of QN from 0 to VDD/2. Therefore, we safely assume that the PMOS transistors of the IUT (MP2 for QN and MP1 for QP) contribute saturation gate capacitance to the output.

Table I lists the simulated and calculated values of the propagation delays for various transistor ratios as well as the values of $\gamma_N \gamma_P$ and $\zeta_P \zeta_N$ and that we use for each technology. Note that the model error—defined as the ratio of the difference between the calculated and simulated delays over the simulated delay—is within ± 4% for T_{PLH} and within ± 8 % for T_{PLH} , quite good for a closed-form model that avoids complex expressions and provides insight to the designer.

IV. ULPD AND CPTL

IV.1.CPTL DCVSL INVERTER STRUCTURE

DCVSL Implementation Using CPTL Structure Figure 3 depicts the schematic diagram of CPTL inverter circuit. The CPTL uses series of transistors to select between possible inverted output values of the logic, the output of which drives an inverter to generate the non-inverted output signal. Inverted and non-inverted inputs are needed to drive the gates of the pass-transistors. The main advantages are full swing, elimination of static power in the inverter through level restorer and pass transistor. Since restorer is made active while the input V_I is high, the level restoration transistor improves capacitance and takes away pull down current at point "p" strife between level restoration transistor and input transistor (slower switching). Hence level restoration transistor is also to be sized to its minimum level

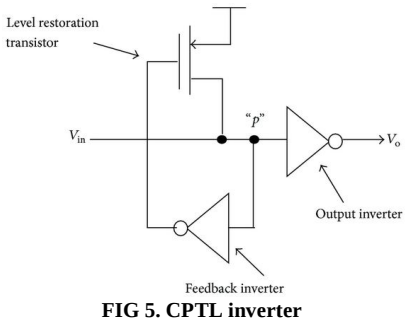

FIG 5. CPTL inverter

IV.2.DCVSL Implementation Using ULPD

A new Ultra-Low-Power Diode- (ULPD-) based DCVSL circuit is shown in Figure 5. ULPD is a combination of PMOS and NMOS transistors where in PMOS transistor gate is connected to the NMOS source and NMOS gate is connected to the PMOS source by using depletion mode type MOSFETS . By replacing a resistor with a ULPD [10], we can eliminate the condition $T_{PLH} > T_{PHL}$ and parasitic effects. ULPD offers a strongly reduced leakage current when compared to the standard diode connected MOSFET while maintaining similar forward current drive capability. When ULPD is reverse biased, both transistors operate with negative V_{gs} voltages. This leads to minimum leakage current compared to the standard diodes. Depending on the threshold voltages the ULPD can also be used in moderate or strong inversion regions. In this circuit, ULPD acts as a resistor. To operate the ULPD as a resistor, the transistors operate in linear region.

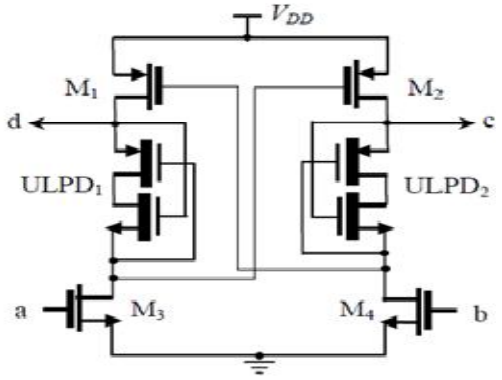

Figure 6. Proposed ULPD-DCVL structure

If we consider the switching conditions of the ULPD, while applying the complementary inputs to the pull-down network, one of the pull-down networks is put in ON condition. Thus pull-down network establishes a path to ground. When logic "1" is applied to the M_3 transistor, then it turns ON and starts conducting current, and the drain of the M_3 transistor quickly drops because of the additional load to PMOS gate. The output voltage of M_3 transistor quickly reaches the M_2 and then M_2transistor reaches ON condition and output "c" is connected to theV_{DD} As the other input of the pull-down network of M_4 transistor is logic "0" that means it does not establish a path to ground then M_1 transistor is set to OFF condition.By adding the ULPD as a load to the drain of the NMOS transistors and increase the voltage drop at the gates of PMOS to turn on the PMOS transistors operate faster and minimize the waiting time. So $T_{PLH}=T_{PHL}$ and it results in symmetrical output waveforms. More importantly, due to the reduced T_{PLH}, the total delay of the DCVSL circuit comes down.

V. RING OSCILLATOR IMPLEMENTATION BY USING THE ULTRA LOW POWER DIODE

Ring Oscillators have been widely employed in most clock generators and frequency synthesizers for their small die size, quadrature or multiphase outputs, and easy integration in standard CMOS technologies.

Because the oscillation frequency of ring oscillators is mainly determined by the propagation delay of each delay cell, the maximum frequency of single-loop ring oscillators is limited by the delay time of the delay cells. Several techniques have been reported to explore the maximum frequency levels of ring oscillators. Ring oscillators are formed by an odd number of digital inverters connected into a ring, as shown in Fig.5.1 Because of the uneven number of inverters the feedback from the final stage inverts the input to the first stage.

Ring oscillators are simple to make, can self-start, and are used in applications including clock recovery circuits, phase locked loops, crystal-free oscillators, multi frequency oscillators, random number generators, and process variability analysis. Consider the output for low to high propagation delay time (tdlh), which is defined as the time delay to reach the output voltage at 50% of its maximum value VDD. When the input of an inverter switches from high to low, the NMOS transistor goes into cutoff region. In that moment load capacitor C charges through PMOS transistor and the charging current is given by

$$I_{DP} = \frac{CdV_{out}}{dt}$$

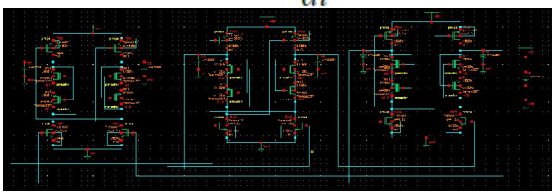

Fig7.1. Proposed ULPD Three Stage Ring Oscillator

A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of π/N, where N is the number of delay stages. The remaining π phase shift is provided by a dc inversion [7]. This means that for an oscillator with single-ended delay stages, an odd number of stages are necessary for the dc inversion. If differential delay stages are used, the ring can have an even number of stages if the feedback lines are swapped.

The ring oscillators designed with a chain of delay stages have created great interest because of their numerous useful features. These attractive features are: (1) It can be easily designed with the state-of-art integrated circuit technology (ULPD), (2) It can achieve its oscillations at low voltage, (3) It can provide high frequency oscillations with dissipating low power, (4) It can be electrically tuned, (5) It can provide wide tuning range and (6) It can provide multiphase outputs because of their basic structure. These outputs can be logically combined to realize multiphase clock signals, which have considerable use in a number of applications in communication systems. The oscillation frequency of an RO depends on the propagation delay Td per stage and the number of stages used in the ring structure. To achieve self sustained oscillation, the ring must provide a phase shift of 2p and have unity voltage gain at the frequency of oscillation. In an m-stage ring oscillator, each stage provides a phase shift of p/m and dc inversion provides the remaining phase shift of p. Therefore, the oscillating signal must go through each of the m delay stages once to provide the first phase. The proposed 3 stage ring oscillator is operated at 103 MHZ frequency. From the output of the ring oscillator we are getting sine wave as output.

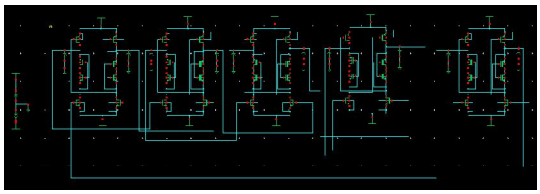

Fig.7.2. Proposed ULPD five stage Ring Oscillator

VI. RESULTS

The performance of the proposed Ultra Low Power Diode (ULPD) DCVSL and Complementary Pass Transistor Logic structures are examined using Cadence and the model parameters of a 180 nm CMOS process. The simulations were carried out with supply voltage VDD=1.8 V. A comparison with existing or already reported designs is included which shows the advantage of the proposed designs good delay performance and the results are shown in Table I. For each transition, the delay is measured from 50% of the input voltage swing to 50% of the output voltage swing. The maximum delay is taken as the cell delay. It is apparent that amongst the existing conventional DCVSL cells, the proposed ones are having lower delays as shown Table I. From the results obtained in Table 1, the following observations has made The pass transistor logic based DCVSL achieves 35% lower delay than the general DCSVSL cell. The Ultra Low Power Diode based DCVSL cells achieves 38% lower delay than the DCVSLR cell.

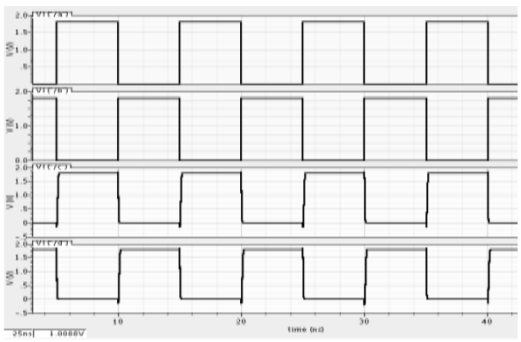

Fig.8. Proposed CPTL DCVSL output simulated results

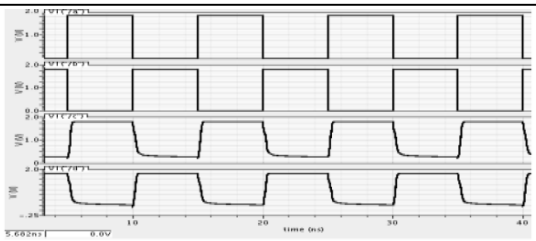

Fig. 9. Simulated input & output waveforms of proposed DCVSL using ULPD structure

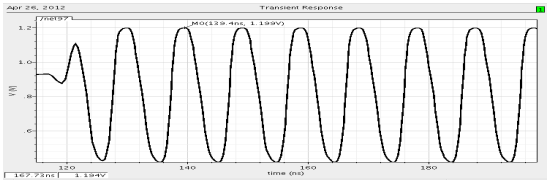

Fig.10. Proposed ULPD three stage ring oscillator output wave form

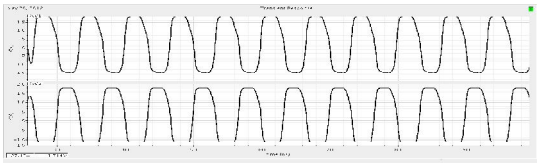

Fig.11. Proposed ULPD five stage ring oscillator output wave form.

Table.1 Delay (ps) for various Supply voltage comparison of all logic structure with VDD = 1.8 V and f = 100 MHz's.

Supply Voltage (v)	DCVSL	CPTL	DCVSL-R	ULPD
1.2	200	410	351	110
1.4	150	256	186	80
1.6	135	188	130	66
1.8	96	151	78	55
2	75	138	60	51
2 .2	89	120	57	42
2.4	32	97	51	40
2.6	31	86	43	37
2.8	28	79	38	32
3	24	74	35	30

VII. CONCLUSION

In this project, we have presented two modified pull-up stages using Ultra Low Power Diode (ULPD) and Complementary Pass Transistor Logic (CPTL). These circuits provide regular and compact layout structure and reduce the diffusion capacitances (since it eases diffusion sharing). The proposed pull-up stage structures are eliminating the delay in the existing DCVSL design and achieve good delay performance. The proposed designs i.e. ULPD based DCVSL and CPTL DCVSL having the best delay in comparison with the other designs. Finally, while implementing high performance complex structures, such as multipliers, ALU (arithmetic logic unit), counters and mobile communications, the intrinsic benefits of proposed ones could be fully exploited.

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