International Journal of Electronics and Electrical Engineering

Volume 3 | Issue 3 Article 12

January 2015

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BAJPAI, DEEKSHA and UPADHYAY, AVNISH KUMAR (2015) "ANALYSIS OF ELECTRICAL BEHAVIOR OF SOI LDMOSFET WITH RESPECT TO TEMPERATURE AND DOPING USING T-CAD SIMULATOR," *International Journal of Electronics and Electrical Engineering*: Vol. 3 : Iss. 3 , Article 12.
Available at: https://www.interscience.in/ijeee/vol3/iss3/12

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# ANALYSIS OF ELECTRICAL BEHAVIOR OF SOI LDMOSFET WITH RESPECT TO TEMPERATURE AND DOPING USING T-CAD SIMULATOR

**DEEKSHA BAJPAI[1], AVNISH KUMAR UPADHYAY[2]**

**Abstract-** In this paper, the effect of temperature variation and doping variation of p-body on various parameters like Breakdown voltage, on resistance, drain leakage current, threshold voltage etc of SOI laterally diffused MOSFET has been analyzed. Since power mosfet is designed for radio frequency power amplifiers which is used in wireless system-on-a-chip applications. The device is fabricated on a thin-film SOI wafer in order to reduce the leakage current and also prohibit the formation of parasitic diode with substrate. On the basis of analysis we are able to prove that this SOI LDMOSFET has +ve temperature coefficient for breakdown voltage, negative temp coefficient for threshold voltage, positive temperature coefficient for on resistance and +ve temperature coefficient for drain leakage current.

***Index Terms-*** *Breakdown voltage, on resistance, drain leakage current threshold voltage, LDMOSFET, SOI, doping cons.*

## I. INTRODUCTION

The first basic device in a high voltage integrated circuit (HVIC) is a DMOSFET (Double-diffused MOSFET) which are extended into two parts: VDMOSFET (Vertical Double-diffused MOSFET) which uses both sides of the chip because it has electrodes on both sides of chip, and LDMOSFET (Lateral Double-diffused MOSFET) having electrodes located only on the top of chip similarly with conventional MOSFET. From this point of view, a LDMOSFET is more compatible with low voltage CMOS/BiCMOS process than a DMOSFET. In addition, a LDMOSFET is preferred in high voltage integrated circuits due to ease to realization of high packing density.

The electronic control system of automobiles needs high temperature operation, typically over 400 K. On the other hand, electronic system of an artificial satellite needs the operation of a power LDMOSFET at low temperature, typically less than 200 K. For the applications in high and low temperature, the temperature characteristics of power LDMOSFET should be investigated. In this paper, we have measured and analyzed the electrical characteristics of power LDMOSFET in the temperature range of 300 K -600 K.

## II. EXPERIMENTS

A. Device Structure

A 2-D view with the help of Sentauris TCAD tool of the n-channel power LDMOSFET under study is shown in Fig. 1. From fig it can be seen that it consists of p-substrate having doping concentration of Boron dopant is $1x10^{16}$ atoms/cm$^3$ with length of 6µm and width of 0.5µm, Buried oxide layer having width of 0.5µm, p-body with boron concentration of $3x10^{17}$ atom/cm$^3$ and length of 3.0µm, N-drift region having doping concentration of Arsenic Dopant is $1x10^{16}$ atom/cm$^3$ and length of 3µm, width active area in which whole device is fabricated is1µm.

The dimension of the device is also given in the Fig-1.

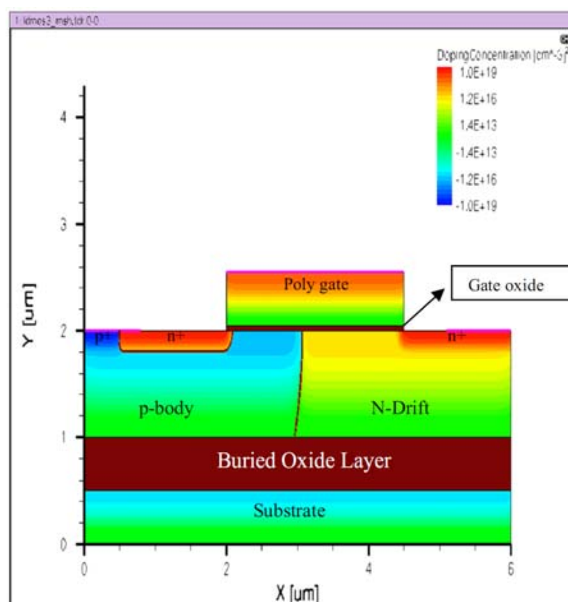


**Fig .1. 2-D View of LDMOSFET with various region,dimensions and doping.**

## III. RESULTS

A. Measurement of Threshold Voltage Variation with temperature

Mathematical expression for threshold voltage is given by the following equation

$$V_T = \varphi_t - \sqrt{2qNa\varphi_t\varepsilon_s} / Co \quad (1)$$

Here Surface potential at threshold voltage is given as

$$\varphi_t = 2V_t \ln \frac{N_a}{n_i}$$

where, $N_a$ is acceptor ion concentration, $C_o$ is oxide capacitance and $\varepsilon_s$ is permittivity of silicon .

From above equation it is clear that on increasing the value of temperature threshold voltage decreases. It can also be seen from the TCAD simulated result with $V_{GS}$=03v and $V_{DS}$=50v.

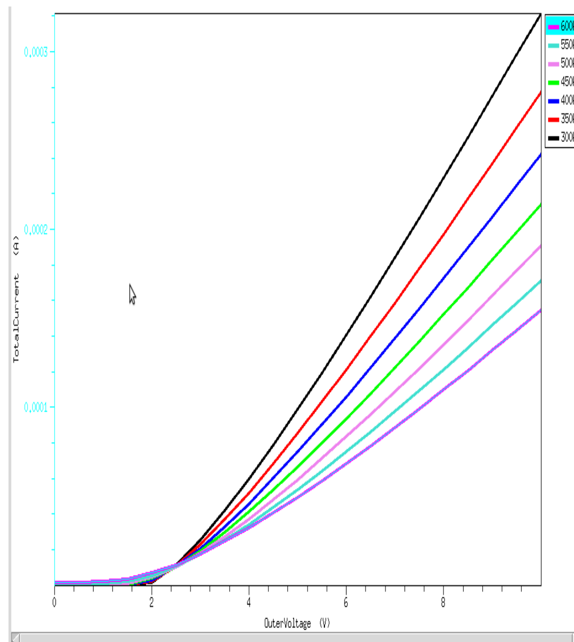


**Fig .2. $I_d$ Vs $V_{gs}$ curve with $V_{GS}$=03v and $V_{DS}$=50v**

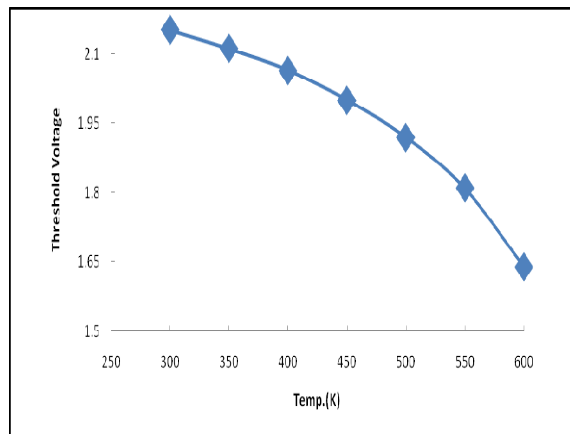


**Fig.3. Threshold voltage variation with temperature**

The data shows the maximum threshold voltage slope is -3.4 mV/K, at higher temperature range which is higher than the variation typically observed in conventional CMOS. This results has been obtained from the heavier doping in double-diffused channel (Impurity concentration of measured device: 3 x $10^{17}$ $cm^{-3}$). From these data, the additional threshold voltage margin is necessary.

B. Measurement of On Resistance Variation with temperature

Since the electron has to flow through Source/Drain contact, p-body and N-Drift, therefore on-resistance depends upon three main components: channel resistance, drift region resistance and the spreading resistance at gate and drain ends of the drift region. Except for relatively low breakdown voltage devices (BV<100V), on-resistance of power LD-MOSFET is mainly determined by the drift region resistance and the expression for drift resistance is given as

$$R_{on} \cong R_d = \frac{L_d}{q^* \mu_{eff} {}^* Q_d {}^* W} \qquad (2)$$

where, $L_d$ is the drift region length, $\mu_{eff}$ is the effective electron mobility, W is the channel & drift region width and $Q_d$ is drift region charge.

From above expression it is clear that drift resistance shows positive temperature coefficient because there is decrement in value of effective mobility of electron resulting increment in drift resistance.

Similar result can be given for the on resistance of LDMOSFET

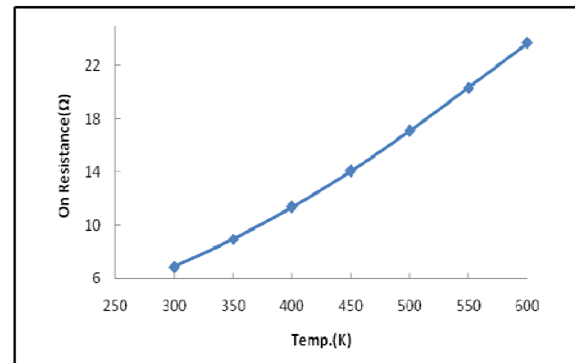


**Fig.4. On resistance variation with temperature**

C. Measurement of Breakdown Voltage Variation with temperature

Breakdown voltage is a one of the major important factor in order to analyses the performance of a power semiconductor device. It depends on junction strength formed due to the concentration gradient in a semiconductor device. In Sintaures Simulator, breakdown voltage is mainly calculated by adding the avalanche effect file . In simulation process this file considers the impact ionizations. Here, it is important to note that the breakdown voltage of a power LD-MOSFET is written as [11]

$$BV_{dss} = \varepsilon_s E_{s,cr}(N_D)\left[\frac{E_{s,cr}(N_D)}{2q(N_D)} + \frac{1}{C_o}\right] \qquad (3)$$

where, $E_{s,cr}$ is a critical electric field.

Breakdown occurs when the carriers gain an ionizing amount of energy in traveling a lattice-scattering mean free path. .A specific energy gain over a given distance, however, corresponds to a specific electric field. In other words, breakdown occurs when the electric field in the depletion region reaches some critical value (Es,cr(ND) in model (3).

$$\lambda = \lambda_o \tanh\left(\frac{E_P}{2kT}\right) \quad (4)$$

As the temperature increases, the mean free path decreases, requiring a higher field to allow the carriers to obtain sufficient energy to initiate impact ionization. Therefore, breakdown voltage increases with temperature. Fig. 4 plots measured the off-state breakdown of a power LDMOSFET over the temperature range of 300 K - 600 K. As depicted from the figure, the breakdown voltage increases 0.04 V per 1K.

This drain-source breakdown voltage is measured with VGS = 0v and the applied drain-source voltage should be greater than or equal to the rated voltage of the device .For this device we kept it at 200v.

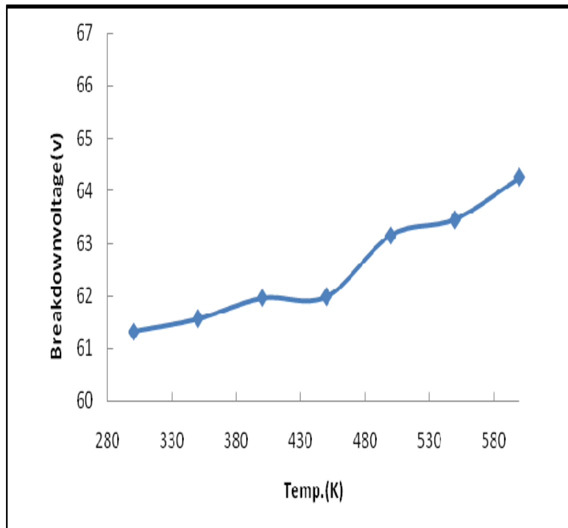


**Fig.5. Temperature Variation of Breakdown Voltage**

D .Measurement of Drain Leakage Current Variation with temperature

This is the drain current for a drain-source voltage of 100 % of rated voltage that drain voltage value must be near to breakdown voltage, with VGS = 0. Since on increasing the value of temperature the concentration of minority charge carriers will increase result increment in the drain leakage current. Hence we can say that drain leakage current shows positive temperature coefficient.

Figure 6 shows the variation of Log $I_{DSS}$ variation with temperature range of 300k to 600k.

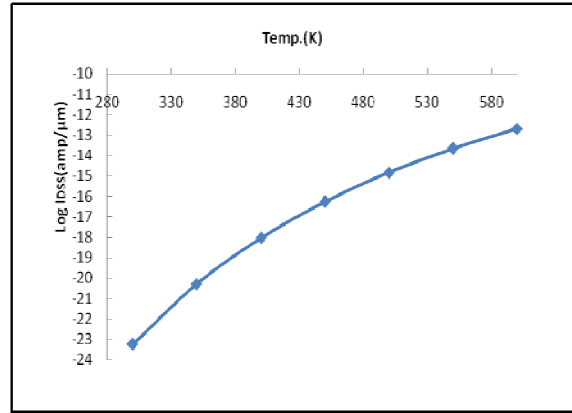


**Fig.6. Temperature Variation Of Log $I_{DSS}$**

E .Measurement of Electron Current Density Variation with temperature

For analysis of electron current density we kept our device in ambient condition with $V_{DS}$=50v and $V_{GS}$=3v. From the result shown by the simulator there is a increment in the e-current density which is mainly due to breaking of covalent bonds resulting generation of extra electrons participating in current due to electrons. Figure 7 shows the variation of maximum electron current variation with temperature range of 300k to 600k.

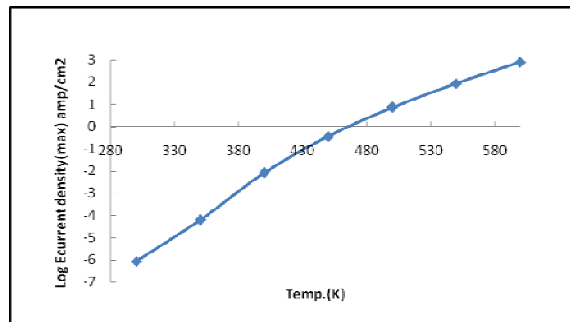


**Fig.6. Temperature variation of Electron current density**

F .Measurement of Specific ON Resistance Variation with P-body Doping Concentration

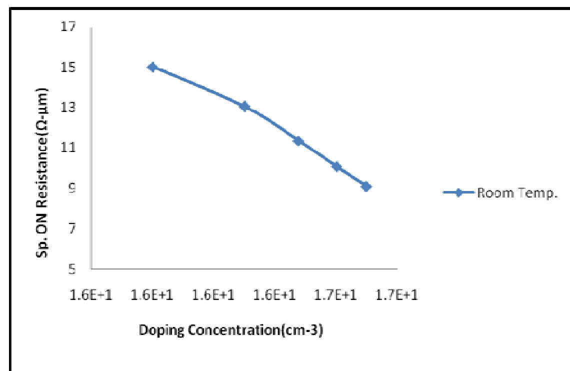


**Fig.7. Sp. ON Resistance Variation with log of Doping Conc.**

With the reference of eq.2 on increasing the doping concentration of p-body we are directly increasing the value of charge associated with the channel and hence decreasing the value of ON-Resistance .

Sentaurus simulator shows the approximately linear decrement in ON- Resistance value which can be shown in Fig.7.

G .Measurement of Breakdown Voltage Variation with P-body Doping Concentration

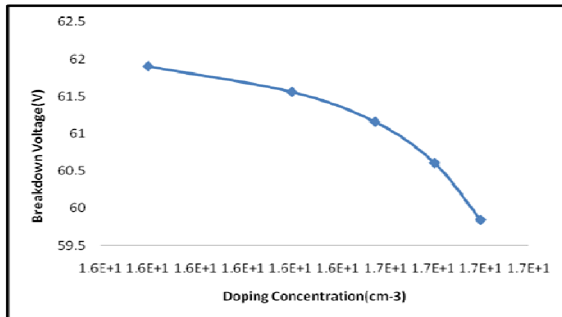


**Fig.8. Breakdown Voltage Variation with log of Doping Conc.**

As Fig.8. shows a non linear declinement of Breakdown voltage with the variation of p-body Doping concentration .It is quite obvious thing because in above section we saw the variation of on resistance with respect to doping concentration and also breakdown voltage and on resistance are directly proportional quantities. Hence this parameter shows decrement with the increase of doping concentration of p-body.

## IV. CONCLUSION

In this paper, we have investigated the temperature characteristics and doping concentration variation of power LDMOSFET, which are widely used in high temperature applications, such as electronic control system of automobiles and low temperature applications such as artificial satellite systems. The results of this study indicate, as temperature goes up, specific on-resistance increases exponentially with the exponent of 2.2. And, maximum threshold voltage changes with variation rate of -3.4 mV/K, which is higher than the variation typically observed in conventional CMOS. This is due to the heavier doping in the double-diffused channel. Also, off-state breakdown voltage increases linearly with a slope of 100 mV/K. This ratio is lower than that of specific on-resistance. As temperature goes up, device performance is degraded by the increase of Ron/BV. So, this effect makes a difficult to satisfy the specification of application systems. Otherwise, a device faces up with low breakdown voltage. Therefore, extraction of optimum drift region length, in consideration of temperature characteristics, is very important.

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