International Journal of Electronics and Electical Engineering

Volume 3 | Issue 3 Article 7

January 2015

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DESIGN AND IMPLEMENTATION OF TWO PHASE INTERLEAVED DC-DC BOOST CONVERTER WITH DIGITAL PID CONTROLLER

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Abstract- DC-DC converters are widely used in Industrial, Commercial and Non Renewable energy applications and also especially in Switch Mode Power Supplies. The two phase interleaved DC-DC boost converter (IBC) for low input voltage applications is designed and implemented with digital controller. The interleaved concept is used to meet the increased demands and also a low current ripple in source current due to this reducing the size of the filter component in input and output. Using interleaving concept can reduces stress on the devices, increases in efficiency, faster dynamics, light weight, compactness and higher power density. The digital controller was designed and implemented by using Field Programmable Gate Array (FPGA). The proto type model was developed and tested in Laboratory. The digital controller gives improved augment time as well as settling time.

Keywords- *FPGA, Interleaved Boost converter, PV array, PID, SISO tool , Spartan-3,VHDL, Xilinx ISE.*

I. INTRODUCTION

In recent years, the demand for DC- DC converters has increased as the front end stage for the battery sources and the renewable energy applications such as the solar arrays and the fuel cells. Two Phase Interleaved DC-DC Boost converter are introduced to meet the increased demands such as low current ripple, high efficiency, faster dynamics, light weight and higher power density. Interleaving also called multi-phasing, is a technique that is useful for reducing the size of filter components [6]. The input to these converters is an unregulated and low DC voltage, which is obtained by photovoltaic (PV) array output voltage. There will be variations in the output voltage due to change in the intensity of the solar radiations. The interleaved boost converter will act as pre-regulator in the PV system. Interleaved boost converter are suitable for universal input applications, provided load voltage is always remains greater than the input voltage [1, 3].

The Two Phase Interleaved Boost Converter was analyzed using state space averaging technique [2, 4] for finding transfer function of the converter. The Digital PID controller was designed using the FPGA. This paper is proposed, to design and implementation interleaved boost converter with digital controller in FPGA [5, 7].

This paper presents with the design and implementation of interleaved DC-DC Boost converter with digital PID controller. Section II presents working principle of IBC with duty cycle d (0.5<d<1). Section III describes the design of digital PID controller for two phase IBC. Section IV deals with implementation of FPGA based digital PID controller using Xilinx block sets. Section V describes the design and system development. Section VI gives the simulation results and also experimental results. Finally section VII concludes the paper.

II. TWO PHASE INTERLEAVED BOOST CONVERTOR

The two phase interleaved boost converter is shown in Fig-1. There are two parallel converter channels in the circuit. The first channel is composed of inductorL_1, Switch S_1, and Diode D_1, whereas the second channel consists of L_2, S_2 and D_2. The two converter channels are essentially connected in parallel but operate in an interleaved mode. They share the same filter capacitor C at the output. It is assumed that the parameters of the two channels are identical. The gating arrangement and the inductor current waveforms of the converter are shown in Fig-1.a. With the interleaving design, the gating signals S_1(vg1) and S_2(vg2) for switch S_1 and S_2 are identical but shifted by 360°/2=180°, where 2 is the no. of converters which are connected in parallel. The total input current I_{in}, which is the sum of the two inductor currents i_{L1} and i_{L2} are shown in Fig-1a.

Mathematical model for the two phase interleaved boost converter is developed for duty cycle (0.5<d <1). In this case there are four switching modes for the converter, Mode-1: Switch S_1 is closed D_2 conducting; Mode-2 the devices S_2, S_1 are conducting; Mode-3 the devices are S_2, D_1 are conducting; Mode-4 the devices S_1,S_2 are conducting, The equations for these four different circuits are developed, the detailed equations are given here, and the corresponding state models are obtained.

By applying KVL and KCL to the below circuit, Mode-1

$$\frac{di_{L_1}}{dt} = -\left(\frac{(r_{l1}+r_{s1})}{L_1}\right) i_{L1} + \frac{V_s}{L_1} \quad \ldots\ldots\ldots\ldots (1)$$

$$\frac{di_{L2}}{dt} = \frac{V_s}{L_2} - \frac{V_{d2}}{L_2} - \frac{RV_C}{L_2(R+r_C)} - i_{L2}\left[(r_{L2}+r_{S2}) + \frac{Rr_C}{(R+r_C)}\right]\frac{1}{L_2}$$

…… (2)

$$\frac{dV_C}{dt} = i_{L2}\frac{R}{C(R+r_C)} - \frac{V_C}{C(R+r_C)} \text{ ……. (3)}$$

Write the equations (1), (2) and (3) in matrix form
We get,

$$\dot{X} = AX + BU$$

$$X = \begin{bmatrix} i_{L1} \\ i_{L2} \\ V_C \end{bmatrix}, \quad U = \begin{bmatrix} V_s \\ V_{d1} \\ V_{d2} \end{bmatrix}$$

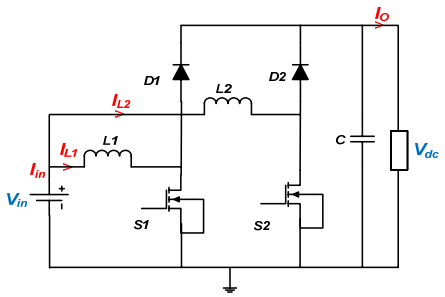

Fig.1 Two Phase Interleaved Boost Converter

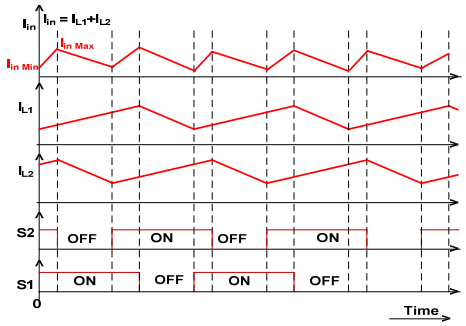

Fig-1a Typical Waveforms of Inductor currents (d > 0.5)

$$A1 = \begin{bmatrix} -(r_{L1}+r_{S1})/L1 & 0 & 0 \\ 0 & -\left[(r_{L2}+r_{S2}) + \frac{Rr_C}{R+r_C}\right]/L2 & -R/(R+r_C)L2 \\ 0 & R/C(R+r_C) & -1/C(R+r_C) \end{bmatrix}$$

$$B1 = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & \frac{1}{L_2} & -\frac{1}{L_2} \\ 0 & 0 & 0 \end{bmatrix}$$

Output equation

$$V_O = \frac{RV_C}{(R+r_C)} + i_{L2}\frac{Rr_C}{(R+r_C)} \text{ ……. (4)}$$

$$Y = C^T X$$

$$C1^T = \begin{bmatrix} 0 & \frac{Rr_C}{(R+r_C)} & \frac{R}{(R+r_C)} \end{bmatrix}$$

Mode-2 and Mode-4

$$\frac{di_{L1}}{dt} = -\left(\frac{(r_{L1}+r_{S1})}{L_1}\right)i_{L1} + \frac{V_s}{L_1} \text{ …… (5)}$$

$$\frac{di_{L2}}{dt} = \frac{V_s}{L_2} - i_{L2}[(r_{L2}+r_{S2})]\frac{1}{L_2} \text{ …… (6)}$$

$$\frac{dV_C}{dt} = -\frac{V_C}{C(R+r_C)} \text{ …….. (7)}$$

$$A2 = \begin{bmatrix} -\frac{1}{L_1}(r_{L1}+r_{S1}) & 0 & 0 \\ 0 & -\frac{(r_{L2}+r_{S2})}{L_2} & 0 \\ 0 & 0 & -\frac{1}{C(R+r_C)} \end{bmatrix}$$

$$B2 = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 \\ 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

Output equation

$$V_O = \left(\frac{R}{R+r_C}\right)V_C \text{ …….. (8)}$$

$$C2^T = \begin{bmatrix} 0 & 0 & \frac{R}{(R+r_C)} \end{bmatrix} \text{ …… (9)}$$

Mode-3

$$\frac{di_{L1}}{dt} = \frac{V_s}{L1} - \frac{V_{d1}}{L1} - \frac{RV_C}{L1(R+r_C)} - i_{L1}\left[\frac{Rr_C+(R+r_C)(r_{L1}+r_{S1})}{(R+r_C)}\right]\frac{1}{L1}$$

.....(10)

$$\frac{di_{L2}}{dt} = \frac{V_s}{L_2} - \frac{1}{L_2}(r_{L2}+r_{S2})i_{L2} \text{ ……. (11)}$$

$$\frac{dV_C}{dt} = i_{L1}\frac{R}{C(R+r_C)} - \frac{V_C}{C(R+r_C)} \text{ …… (12)}$$

$$A3 = \begin{bmatrix} -\frac{1}{L1}\left(\frac{Rr_C+(R+r_C)(r_{L1}+r_{S1})}{(R+r_C)}\right) & 0 & -\frac{R}{L1(R+r_C)} \\ 0 & -\frac{(r_{L2}+r_{S2})}{L2} & 0 \\ \frac{R}{C(R+r_C)} & 0 & -\frac{1}{C(R+r_C)} \end{bmatrix}$$

$$B3 = \begin{bmatrix} \frac{1}{L_1} & -\frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

Output equation

$$V_O = \frac{RV_C}{(R+r_C)} + i_{L1}\frac{Rr_C}{(R+r_C)} \text{ ……. (13)}$$

$$C3^T = \begin{bmatrix} \frac{Rr_C}{(R+r_C)} & 0 & \frac{R}{(R+r_C)} \end{bmatrix}$$

Analysis

Averaged state space model over one particular cycle can be written as

$$\dot{x} = Ax + BV_s \text{ ……. (14)}$$

We can write

$$A = D\sum_{i=1}^{N} A_{2i-1} + \left(\frac{1}{N} - D\right)\sum_{i=1}^{N} A_{2i} \text{ ……(15)}$$

$$B = D\sum_{i=1}^{N} B_{2i-1} + \left(\frac{1}{N} - D\right)\sum_{i=1}^{N} B_{2i} \text{ ……(16)}$$

$$C = D\sum_{i=1}^{N} C_{2i-1} + \left(\frac{1}{N} - D\right)\sum_{i=1}^{N} C_{2i} \text{ ……(17)}$$

Substitute N=2(for two phase) in above equations

$A = (A_1+A_3)(1-D) + (2D-1)A_2$

$B = (B_1+B_3)(1-D) + (2D-1)B_2$

$C = (C_1+C_3)(1-D) + (2D-1)C_2$

To investigate the small-signal behavior, we now assume that d varies from cycle to cycle. Equations (15) (16) and (17) and the perturbations in the input voltage, in the duty ratio and in the states are introduced to (14). By neglecting the non-linear second-order term, the perturbed state-space equation for an

N-phase interleaved converter is obtained as

$$\dot{X} = AX + BV_S + A\dot{X} + B\dot{V}_S + [\sum_{i=1}^{N}(A_{2i-1} - A_{2i})X + \sum_{i=1}^{N}(B_{2i-1} - B_{2i})V_S]\bar{d}$$

When all perturbations are set to zero, the steady-state model is obtained as

$$K = [(A_1 + A_2 - 2A_3)]$$

$$T = [(B_1 + B_2 - 2B_3)]$$

$$P = [(C_1 + C_2)(1 - D) + (2D - 1)C_3]$$

$$Q = (2C_3 - C_1 - C_2)$$

Finally, the transfer function of output to variations in the duty ratio is expressed as

$$\frac{\hat{v}_0(s)}{\hat{d}(s)} = P[sI - A]^{-1}[(K)X + (T)V_S] + [QX]$$

III. DESIGN OF DIGITAL PID CONTROLLER

The two phase interleaved boost converter is analyzed using state space averaging technique with duty cycle d (0.5<d<1). The circuit is analyzed in four modes of operation by considering parasitic elements. The transfer function of output voltage to variations in the duty ratio is obtained using small signal analysis is taken into consideration. The design values are based on the Table-1 converter specifications for the design of FPGA based digital PID controller.

After getting the transfer function of the converter, the same is fed into the SISO (Single Input Single Output) design tool command in the MATLAB to generate bode of the system, loop bode, closed loop step response of compensated system, closed loop bode plots and PID controller design values are obtained K_p, K_i and K_d=0. These values are brought together to create a digital PID controller.

One of the most powerful but complex controller mode operations combines the proportional, integral, and derivative modes with a control loop feedback mechanism. Fig-2 shows the basic structure of the digital PID controller [7].

The analytical equation for Digital PID controller is

$P = K_p e + K_i \int e\,dt + K_d (de/dt) + P_I(0)$…… (18)

Where,

K_p = Proportional gain

K_d = Derivative gain

e = Error in % of full scale range

K_i = Integral gain

$P_I(0)$ = value of integral term at t=0

Taking Laplace transform of equation (18) will results in,

$$P(S) = K_p E(S) + \frac{K_i}{S}E(S) + K_d S E(S)$$…… (19)

Also the transfer function of PID controller is

$$D(S) = K_p + \frac{K_i}{S} + K_d S$$ …… … (20)

Where, Transforming equation (20) into digital domain gives the transfer function of digital PID controller.

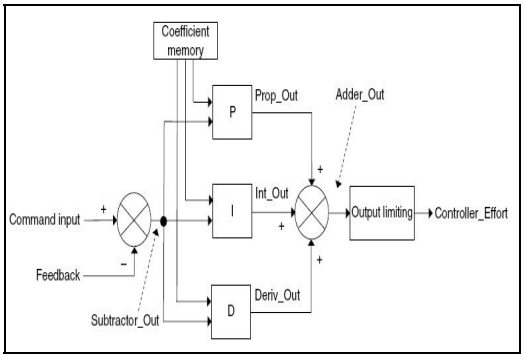

Fig-2 Digital PID Controller

$$D(z) = K_p + K_i\frac{T(z+1)}{2(z-1)} + K_d\frac{1(z-1)}{T(z+0)}$$…… (21)

Equation (21) can be realized to direct form structure as:

$$D(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}}$$ …… (22)

Normally for digital controller b2=0 and b1=-1 [7] therefore, coefficients a_0, a_1 and a_2 can be given as $a_0 = K_p + K_i\frac{T}{2} + \frac{K_d}{T}$, $a_1 = K_p + K_i\frac{T}{2} - 2\frac{K_d}{T}$, $a_2 = \frac{K_d}{T}$ Where K_p, K_i, K_d are proportional, integral and derivative parameters, respectively of digital PID controller and T is sampling period. Fig-3 shows the direct form structure of digital PID controller corresponding to equation (22).

IV. IMPLEMENTATION OF DIGITAL PID CONTROLLER

The implementation of digital PID controller using controller design values are based on the Table-1 converter specifications. The Kp, Ki and Kd are found from the SISO design tool in the MATLAB are given below: Kp=0.010086, Ki=848.4191and Kd=0. These values are brought together to create a digital PID controller. The system generator is associated with the presented co simulation methodology/tools using automatic bit stream generation. The system generators a Xilinx tool box available with MATLAB for design a digital PID controller.

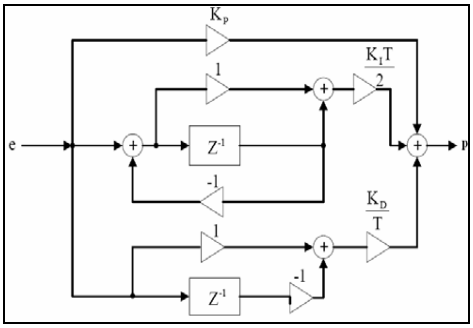

Fig-3 Direct Form Structure of Digital PID Controller

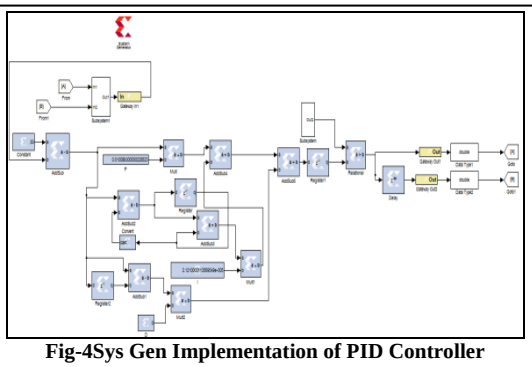

Fig-4Sys Gen Implementation of PID Controller

The implementation of digital PID controller using the Xilinx blocks, the controller is designed based on the direct form structure of digital PID Controller shown in Fig.3. The K_p, K_i & K_d values are multiplied with the error signal. The error signal is generated by comparing with reference voltage and output voltage of the converter. The subsystem1 block consists of two phase interleaved boost converter simulated using Table-1designed values of converter. The converter model as shown in the subsystem1block Fig-5.The ramp signals are generated with switching frequency 10 kHz using up counter from the Xilinx blocks shown in subsystem block Fig-6. The ramp signal and PID controller output is compared and produce the pulses and the same are shifted by180° phase shift to drive the two switches S_1 and S_2 respectively.

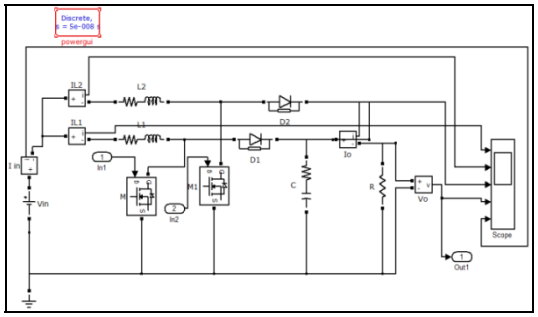

Fig-5 Subsystem1 Block

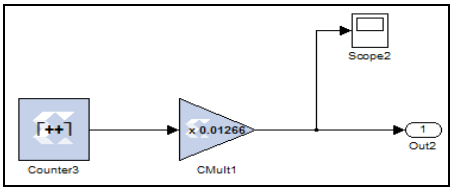

Fig-6 Subsystem Block

V. SYSTEM DEVELOPMENT

Table-1, Design Values of Two Phase IBC

Output voltage(V0)	30	Volts
Output current I0=	0.5	Amps
output power	15	watts
input current I_L=	1.25	Amps
Inductor L	5.9	m H
L_1	3	m H
L_2	3	m H
r_L	0.22	Ω
Δi_L	0.115	Amps
I_{L1}	0.625	Amps
I_{L2}=	0.625	Amps
Resistance R=	60	Ω
Capacitance C =	111	µF
i_{Lmax} =	1.31	Amps
i_{Lmin} =	1.19	Amps
ΔV_o	0.3	Volts
r_C=	230	mΩ
Efficiency = η =	97.77%	

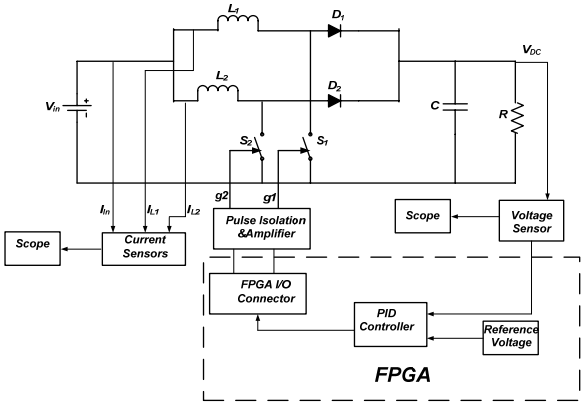

Fig-7 Block Diagram of Control and Power Scheme

A laboratory prototype of interleaved boost converter is designed for two phase for experimentation. The complete schematic diagram of the system is as shown in Fig-7 shows the block diagram representation of power and control scheme. The output voltage is sensed and then compared to the reference voltage. The error is feed to PID controller and PID controller output is compared to reference ramp signal to generate the firing pulses for the switches. The firing pulses after proper isolation and amplification are given to switching devices.

VI. SIMULATION & EXPERIMENTAL RESULTS

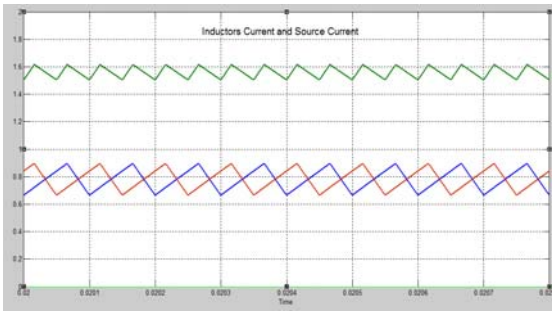

Fig-8 Inductors Current and Source Current Waveforms

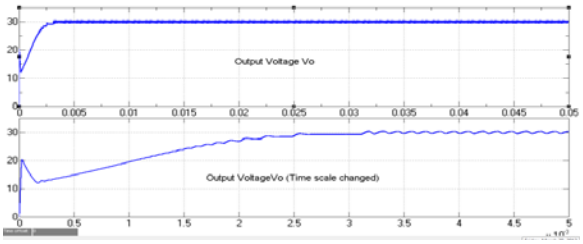

Fig-9 Output Voltage Waveforms in Simple PID Control (Stabilizing at 3.1 ms)

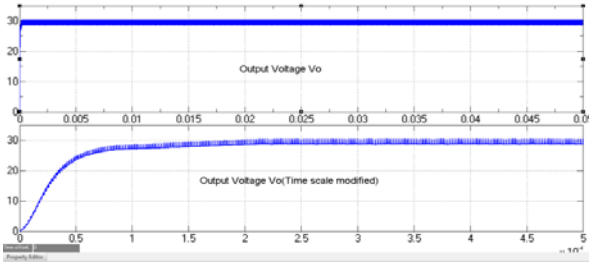

Fig-10 Output Voltage Waveforms in FPGA Based Digital PID Control (Stabilizing at 250 µs)

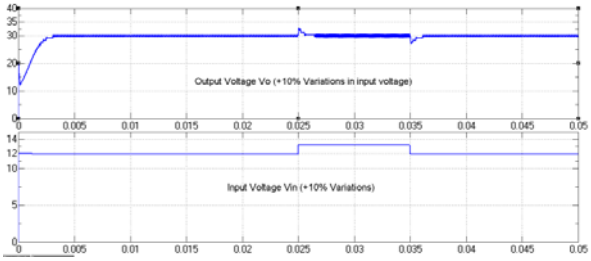

Fig-11 Output Voltage Waveform in Simple PID Controller (+10% Variations in Input Voltage)

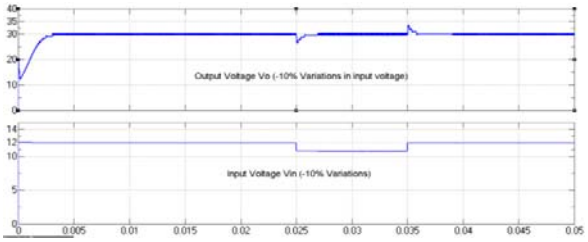

Fig-11a Output Voltage Waveform in Simple PID Controller (10% Variations in Input Voltage)

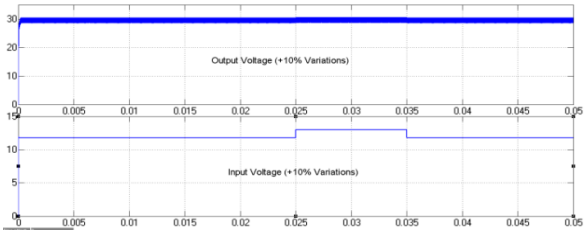

Fig-12 Output Voltage Waveform in FPGA Based Digital PID Controller (±10% Variations in Input Voltage)

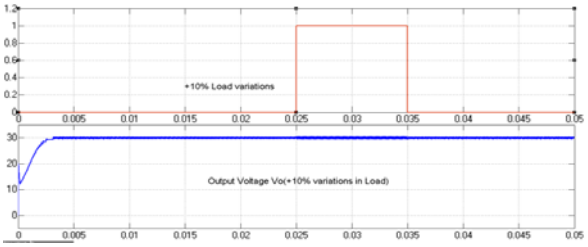

Fig-13 Output Voltage Waveform in Simple PID Controller (+10% Variations in Load)

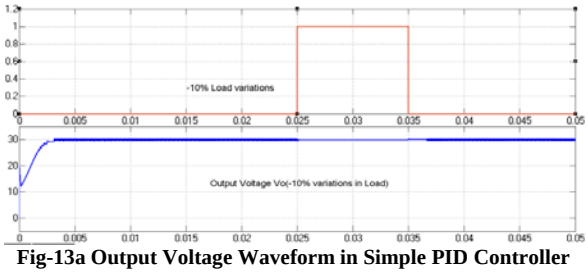

Fig-13a Output Voltage Waveform in Simple PID Controller (-10% Variations in Load)

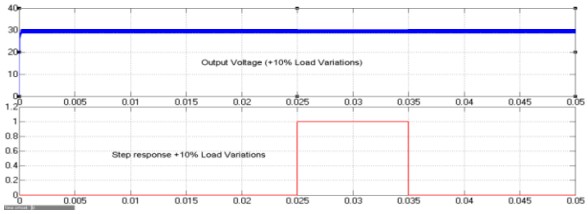

Fig-14 Output Voltage Waveform in FPGA Based Digital PID Controller (+10% Variations in Load)

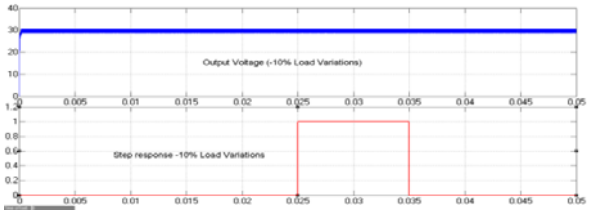

Fig-14a Output Voltage Waveform in FPGA Based Digital PID Controller (+10% Variations in Load)

EXPERIMENTAL RESULTS

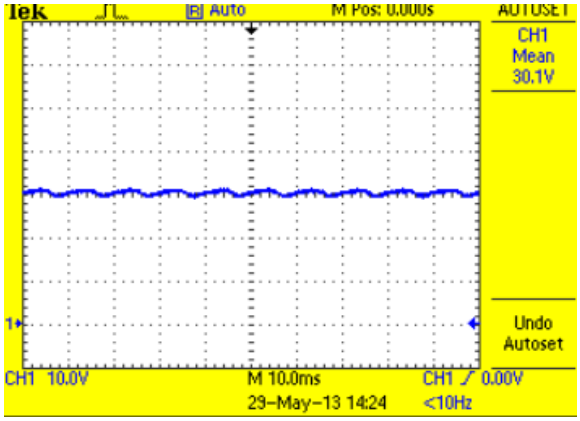

Fig-15 Output Voltage Waveform

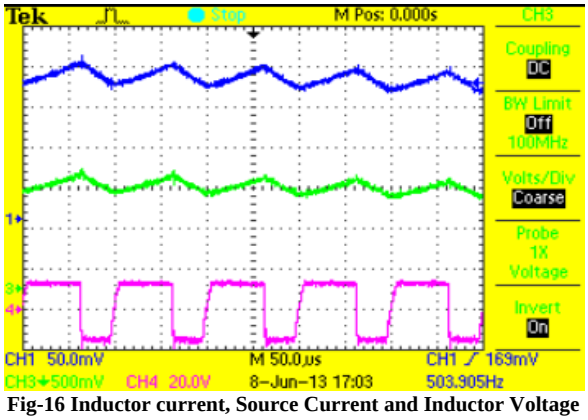

Fig-16 Inductor current, Source Current and Inductor Voltage Waveform

Figure-8 shows simulation results of inductors current waveforms and source current waveform. The source current I_{in} is the sum of I_{L1} and I_{L2} as they are in phase opposition, therefore the ripple cancellations in the source current ripple get reduced. An observed in the current waveform I_{in} the ripple current Δi_L is 5.33A.Whereas the ripple current in individual inductor is 10A. Figure-9 and 10 shows the output voltage waveforms in simple PID control and FPGA based digital PID controller. In simple PID control the initial voltage transient of 20 volts and reduced to 12 volts and from 12 volts the voltage is linearly increased and stabilized at 3.1 ms to rated output voltage 30 volts.

In FPGA based digital control the voltage linearly varied and the voltage is stabilizing at 250 µs to rated output voltage 30 volts with better rise time and settling time.

Figure-11 and 11a shows the simulation results of output voltage waveforms with ±10% variations in input voltage in simple PID controller. The transients at the output voltage waveforms are observed in the rise time and fall time. In the rise time the voltage observed 32 volts and in fall time 28 volts for 1ms time period. Figure-12 shows the output voltage waveform with ±10% variations in input voltage in FPGA based digital PID controller.

There are no transients while changing over in input voltage. Figure-13 and 13a shows the simulation results of output voltage waveforms with ±10% load variations in simple PID controller. An observed the output voltage almost constant and the slight ripples are observed while increasing in load. Figure-14and 14a shows the output voltage waveforms with ±10% load variations in FPGA based digital PID controller. An observed the output voltage is almost constant 30 volts with increase or decrease in load. Fig-15 shows the output voltage waveform in experimental results the output voltage is 30.1 volts and ripple are observed 0.5 volts it is near to simulation results. Fig-16 shows the inductor current and source current and voltage across the inductor.

The inductor currents are in-phase opposition the ripple in the source current get reduced and observed in the waveform the ripple in source current ΔI_{in}=0.15amps and individual inductor ripple is ΔI_{L1}= ΔI_{L2}=0.25amps. The FPGA based digital PID controller is synthesis using Xilinx ISE design tools resulted in the above simulation results for a Spartan3 as target FPGA.

VII. CONCLUSIONS

The two phase interleaved boost converter has advantages based on comparison with a single boost converter. The input current and output voltage ripple will be reduced and also the size of filtering component at the output. With the increase in number of phases of converter, will results in size of the filter and source current ripples can be reduced further increase the power density and efficiency of the converter. And also due to current sharing the stress on the devices gets reduced and also lower current rating devices can be used for higher power density converters by this can reduce the cost of the converter.

FPGA based digital PID controller gives better rise time as well as settling time as seen in the simulation results. The design and implementation of digital PID controller on FPGA gives faster time response, accuracy, reduced power consumption, compactness, and cost improvement as compared to simple PID controller.

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