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# A CURRENT-MODE RMS-TO-DC CONVERTER BASED ON TRANSLINEAR PRINCIPLE

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**Abstract-** In this paper a low-power current-mode RMS-to-DC converter is proposed. The proposed converter includes absolute value circuit, squarer/divider circuit, low-pass filter and square root circuit which employ CMOS transistors operating in weak inversion region. The RMS-to-DC converter has low power consumption (<1µW), low supply voltage (0.9V), wide input range (from 50 nA to 500 nA), low relative error (<3 %), and low circuit complexity. Comparing the proposed circuit with two other current-mode circuits shows that the former outperforms the latters in terms of power dissipation, supply voltage, and complexity. Simulation results by HSPICE show high performance of the circuit and confirm the validity of the proposed design technique.

***Keywords***- *current-mode; RMS-to-DC converter; weak inversion; low power; low voltage ;*

## I. INTRODUCTION

The RMS-to-DC converter as an electronic measuring circuit is employed for computing of the average energy content in an electronic signal. This converter is widely used in instrumentation devices and biomedical Ics.

Recently, researchers focus on small size, low power consumption and capable to operate under low supply voltage while the performance still maintains. Most of RMS-to-DC converters with CMOS transistor in saturation region have power consumption of about 100uW and required the supply voltage of about 1.5V [1-2], which is not suitable for very low power applications such as in biomedical Ics [3]. In addition, a micro power CMOS true RMS-to-DC converter has been proposed [4], however they design based on CMOS transistor operating in saturation region combination with FG-MOS operating in weak inversion region which is complicated synthesis for the integrated circuit. The two approaches exist for designing RMS-to-DC converter: 1) current-mode approach, 2) voltage-mode approach. A current-mode circuit enables current processing and has certain important advantages against a voltage-mode circuit, such as, wide bandwidth, high slew rate, low power consumption, and simple circuitry [5-6].

The proposed circuit of RMS-to-DC converter in this paper includes four current-mode blocks; (a) absolute value (b) squarer (c) averaging (d) square root. All of them designed based on the use of CMOS transistors operating in weak inversion region where their power consumption of about 250nA. The main features of this circuit is its low-power (<1µW), requires low supply voltage of 0.9V for the input range of 50nA to 500nA and simplicity of the circuit design. The other feature of this circuit is that the converter doesn't have additional power source, then it causes lower power compared to other converter.

The paper is organized as follows. In section II the basic principle of converter is described. Circuit design of the proposed converter is explained in section III and the circuit analysis of the proposed converter is presented. The characteristics and the performances of the converter are presented by HSPICE simulation results in section IV and conclusion is provided in section V.

## II. BASIC PRINCIPLE

One of the most notable instances of nonlinear dynamic operation from a practical viewpoint is the RMS-to-DC conversion. In its basic form, and assuming input and output currents, such operation can be described by the equation :

$$I_{out} = \sqrt{\langle I_{in}^2 \rangle} \qquad (1)$$

Where $I_{in}$ and $I_{out}$ are the input and output currents of the RMS-to-DC converter, respectively, and the operator $\langle \cdots \rangle$ represents a time averaging. Fig. 1 shows the block diagram of the current-mode RMS-to-DC converter which consists these two operations.

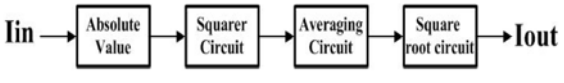


**Figure 1. Block diagram of RMS-to-DC converter**

## III. CIRCUIT ANALYSIS OF THE PROPOSED CONVERTER

Circuit of the first block is shown in Fig.2. Its circuit structure consists of the transistors M3-M6 operating as a current mirror, the transistor M2 connected in cascade to the mirror input and the transistor M1 is used for biasing. In the case of the positive input and

the transistor M1 is used for biasing . in the mirror input

mirror input and the transistor M1 is used for biasing. In the case of the positive input signal current is passed through node X and $V_{SG2} > 0$ the transistors M2 is ON, therefore, the output signal current of the absolute-value circuit $I_{ABS}$ is equal to the input signal current $I_{in}$, ($I_{ABS} = I_{in}$). In the case of the negative input signal current is passed through node X and $V_{SG2} < 0$ the transistor M2 is OFF, the transistor M3 can be copied the current through the transistor M6 ($I_{D3} = I_{D6}$). Therefore the output signal current equals to the absolute of its input signal current, $I_{ABS} = |I_{in}|$.

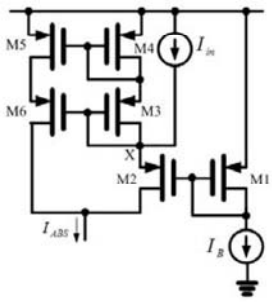


Figure 2. Absolute-value circuit of the RMS-to-DC converter

Fig. 3 shows the current-mode squarer with the absolute-value circuit. Transistors M7-M9 act as a current mirror which copy output current of absolute-value circuit. Also transistors M10-M11 form a current mirror which copy output current of absolute-value to the squarer circuit. The transistors M12-M15 stand in a translinear loop that doing squaring. From the translinear loop, the relation of the transistor M12-M15 in the circuit can be described as [7]:

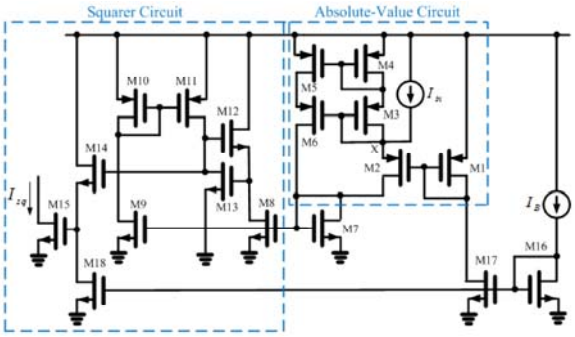


Figure 3. The squarer with the absolute-value circuit

$$V_{gs12} + V_{gs13} = V_{gs14} + V_{gs15} . \quad (2)$$

The drain current of MOS transistor that operates in weak inversion is given by[8]:

$$I_D = I_0 (\frac{w}{l}) e^{\frac{V_{gs}}{nV_T}} (1 - e^{\frac{-V_{DS}}{nV_T}}) , \quad (3)$$

Where is $V_T$ the thermal potential, $I_0$ is a device dependent coefficient, n represents the subthreshold slop, W is the width of the gate and L is the length of the gate.

If $V_{DS} > 4V_T$ then equation (3) can be changed to:

$$I_D = I_0 (\frac{w}{l}) e^{\frac{V_{gs}}{nV_T}} . \quad (4)$$

From equations (2) and (4), it can be deduced:

$$nV_T \ln\left(\frac{I_{12}}{\left(\frac{W}{L}\right)_{12} I_0}\right) + nV_T \ln\left(\frac{I_{13}}{\left(\frac{W}{L}\right)_{13} I_0}\right) = nV_T \ln\left(\frac{I_{14}}{\left(\frac{W}{L}\right)_{14} I_0}\right) + nV_T \ln\left(\frac{I_{15}}{\left(\frac{W}{L}\right)_{15} I_0}\right) . \quad (5)$$

$$\frac{I_{12}}{\left(\frac{W}{L}\right)_{12} I_0} \cdot \frac{I_{13}}{\left(\frac{W}{L}\right)_{13} I_0} = \frac{I_{14}}{\left(\frac{W}{L}\right)_{14} I_0} \cdot \frac{I_{15}}{\left(\frac{W}{L}\right)_{15} I_0} . \quad (6)$$

If $(W/L)_{12}.(W/L)_{13} = (W/L)_{14}.(W/L)_{15}$, then equation (6) can be shown as :

$$I_{12}.I_{13} = I_{14}.I_{15} . \quad (7)$$

From the circuit analysis in Fig. 3, $I_{15} = I_{sq}$, $I_{14} = I_B$ and $I_{12} = I_{13} = |I_{in}|$, thus equation (7) can be rewritten as :

$$|I_{in}|^2 = I_B I_{sq} \rightarrow I_{sq} = |I_{in}|^2 / I_B , \quad (8)$$

Where $I_{sq}$ is the output current of the squarer circuit.

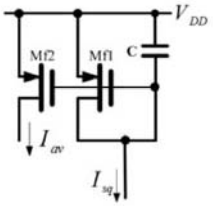


Figure 4. First-order current-mode low-pass filter

Fig. 4 shows the averaging circuit or the first-order current mode low-pass filter, which consist of the current mirror Mf1-Mf2 and the capacitance C connected parallel to the mirror input [9]. From equation (8) and circuit analysis in this figure, the output current $I_{av}$ can be expressed as :

$$I_{av} = \frac{1}{I_B \tau} \int_0^\tau I_{in}^2(t) dt , \quad (9)$$

Where $\tau = C / g_{m16}$ is the time constant of the filter and the transconductance of the transistor Mf1. In order to give a good performance and accuracy of more than 1% for the required frequency range, the value of capacitor C must be chosen such that [10] :

$$C \geq \frac{5 I_{av,\max}}{n V_T (2\pi f_{\min})} . \quad (10)$$

Where $f_{\min}$ is the lowest frequency of the interested frequency range. For example, if the amplitude of the sinusoidal input current $I_M = 500nA$ , $f_{\min} = 100Hz$ and ripple error of 1%, then the averaging capacitance of $C = 35nF$ must be chosen. Considering equation (10), It's obvious if frequency increases then the capacitance of C decreases. therefore, the ripple error diminishes by increasing of frequency.

Fig. 5 shows the current-mode square root circuit that follows translinear principle. Transistors M1,M2,M4,M5 form a translinear loop. According to Fig. 5 and translinear principle, it can be deduced that :

$$V_{gs1} + V_{gs2} = V_{gs4} + V_{gs5} . \quad (11)$$

Considering equation (4), equation (11) can be rewriting as :

$$nV_T \ln\left(\frac{I_1}{\left(\frac{W}{L}\right)_1 I_0}\right) + nV_T \ln\left(\frac{I_2}{\left(\frac{W}{L}\right)_2 I_0}\right) = nV_T \ln\left(\frac{I_4}{\left(\frac{W}{L}\right)_4 I_0}\right) + nV_T \ln\left(\frac{I_5}{\left(\frac{W}{L}\right)_5 I_0}\right) . \quad (12)$$

$$\frac{I_1}{\left(\frac{W}{L}\right)_1 I_0} \cdot \frac{I_2}{\left(\frac{W}{L}\right)_2 I_0} = \frac{I_4}{\left(\frac{W}{L}\right)_4 I_0} \cdot \frac{I_5}{\left(\frac{W}{L}\right)_5 I_0} . \quad (13)$$

From the circuit analysis in Fig. 5, $I_1 = I_3, I_4 = I_{av} - I_B$ $I_5 = I_B, I_2 = (I_{out} + I_B)/2, I_1 = (I_{out} - I_B)/2$ And $2(\frac{W}{L})_1 = 2(\frac{W}{L})_2 = (\frac{W}{L})_4 = (\frac{W}{L})_5$, thus equation (13) can be rewritten as :

$$\frac{I_{out}^2 - I_B^2}{4} = \frac{1}{4}(I_{av} - I_B)(I_B). \quad (14)$$

Therefore, $I_{out}$ is equal to :

$$I_{out} = \sqrt{I_{av} . I_B} = \sqrt{\frac{1}{\tau}\int_0^{\tau} I_{in}^2(t)dt}. \quad (15)$$

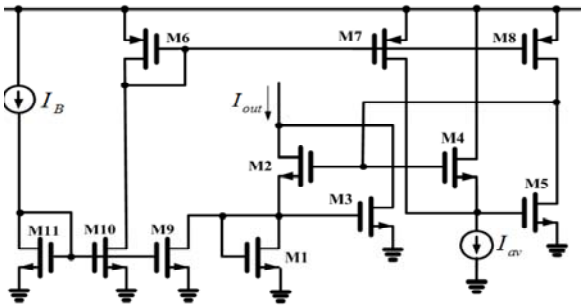


Figure 5. The proposed square root circuit.

The equation (15) clearly indicates that the output current $I_{rms} = I_{out}$ is the root-mean-square value of the input current $I_{in}$ . The complete circuit diagram of the proposed RMS-to-DC converter is depicted in Fig. 6.

## IV. SIMULATION RESULTS

The performance of the circuit has been studied through simulation results using HSPICE by level 49 parameters (BSIM3v3.2) in 0.18µm standard CMOS technology., and where employed. The aspect ratio of transistors is shown in Table I. The simulation results in Fig. 7 and Fig. 8 show output of the converter for the input signals of sinusoidal and triangular waveform, respectively, with the peak amplitude of 200nA at frequency of 100Hz.

TABLE I. TRANSISTOR ASPECT RATIO

| Transistor | W/L (µm/µm) | Transistor | W/L (µm/µm) |
|---|---|---|---|
| M1-M2 | 2/0.5 | M3-M6 | 2/1 |
| M7-M9 | 2/0.5 | M10-M11 | 2/1 |
| M12-M15 | 2.5/0.5 | M16-M22 | 2/0.5 |
| M23-M30 | 2/1 | M31-M32 | 4/1 |

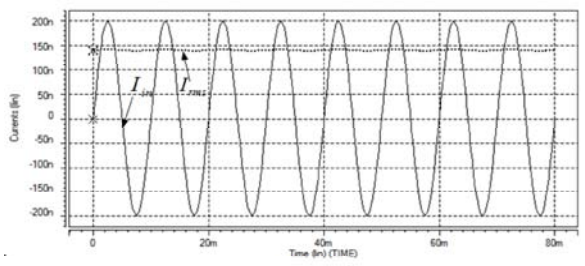


Figure 7. Time response of a sinusoidal input current (solid) and output current (dotted) of the converter.

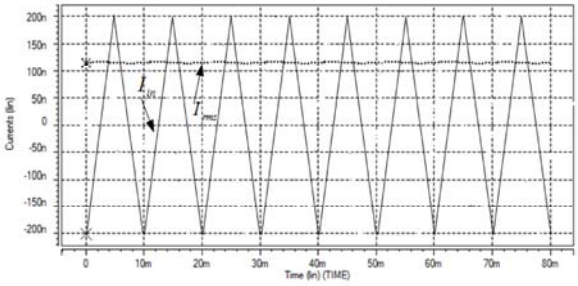


Figure 8. Time response of a triangular input current (solid) and output current (dotted) of the converter.

The relative error, calculated by equation (16), is depicted in Fig. 9 for sinusoidal and triangular waves. A less than 3% and 2.7% error is achieved for amplitudes between 50nA and 500nA of triangular and sinusoidal waves, respectively. We can notice that the ripple at low frequencies is higher than the high frequency. This is due to that, in this case, the capacitor C is selected for $f_{min} = 100Hz$ . Maximum ripple error is 1% for amplitude of 500 nA at frequency of 100 Hz.

Simulation results shows that, bandwidth of the converter is 3.7 MHz and also the power consumption of the circuit for maximum accepted input current (500 nA) is less than 1 µW.

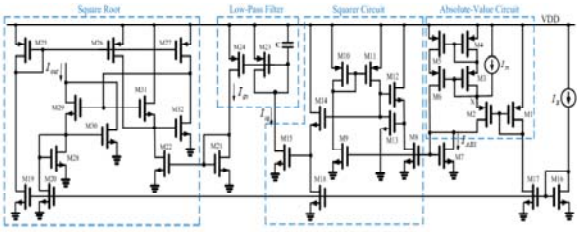


Figure 6. Complete circuit diagram of the proposed RMS-to-DC converter.

$$\text{Relative error} = \frac{I_{rms}(theoretical) - I_{rms}(simulated)}{I_{rms}(theoretical)} \times 100\% \quad (16)$$

To provide more insight into the technique proposed here, a comparison was made between simulation results of this work and measurement results of the formerly reported CMOS RMS-to-DC converters. Table II summarizes this comparison by showing some important parameters of the converters.

TABLE II. Comparison between RMS-to-DC converters

| Parameter | Ref.[11] | Ref.[12] | Proposed circuit |
|---|---|---|---|
| Technology | 0.18µ | 0.5 µ | 0.18 µ |
| Supply voltage | 1 V | 1.5 V | 0.9 V |
| Power dissipation | <3 µW | >100 µW | <1µW |
| Circuit complexity (transistor no.) | 42 MOS | 40 MOS | 32 MOS |
| Input range | 50nA-500nA | 12µA-22µA | 50nA-500nA |
| Maximum Relative Error | 3% | 3% | 3% |
| Bandwidth | 3MHz | Not reported | 3.7MHz |

## V. CONCLUSION

In this paper, a very low-power, low-voltage current-mode RMS-to-DC converter based on MOS translinear principles operating in weak inversion region is presented. Simulation results have been given to confirm the validity of the theoretical analysis. According to results, the converter has low power consumption (<1µW), low power supply voltage (0.9V), and wide input range (50nA to 500nA).

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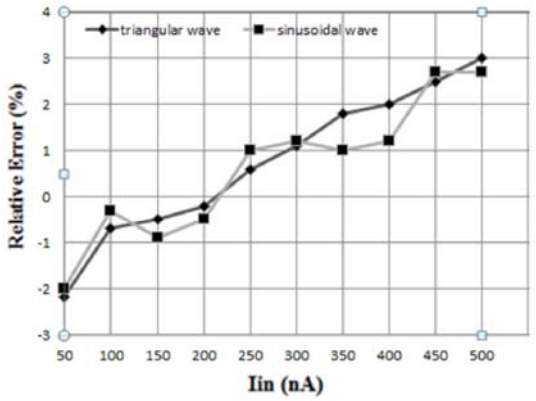


Figure 9. Relative error versus input current of the converter.

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