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Abstract- This paper describes the characteristics comparison of bulk FINFET and SOI FINFET. The scaling trend in device dimension require limit on short channel effect through the control of subthreshold slope and DIBL characteristics.It can be achieved by proper device design. The subthreshold characteristics are plotted with the variation of gate voltage for different doping profile .This paper also compares the performance improvement of Multi-gate Bulk and SOI MOSFET over Single-gate bulk and SOI MOSFET.The simulation results are obtained with the help of TCAD 3-D device simulator are well matched with the ideal characteristics.

Keywords *- Silicon-On-Insulator,FINFET, Short channel effect, DIBL, Subthreshold Slope(SS), 3-D Sentaurus TCAD tool.*

I. INTRODUCTION

To make transistors smaller is to pack more and more devices in a given chip area. Smaller ICs allow more chips per wafer and reducing the price per chip[1]. But the continuous scaling of conventional planar MOSFETs has been facing problems such as subthreshold swing degradation, significant DIBL, fluctuation of device characteristics, and leakage.High channel doping is used to reduce "short channel effects".But high channel doping has major disadvantageous of lower carrier mobility,high tunneling effect, degradation in subthreshold performance and larger parasitic capacitance.Multi-gate structures has been proved better solution to solve these problems[2][3].DG-MOSFET is one of the Multi-gate MOSFET which is used to obtain more control of gate on channel.Fig1

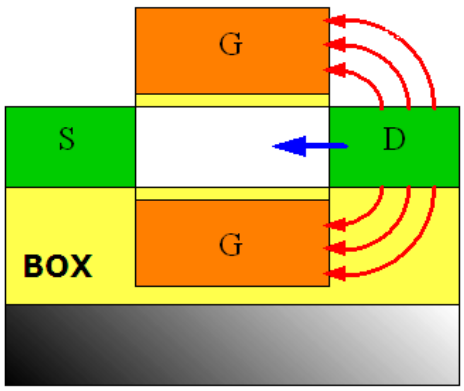

Fig. 1.1 : Planner DG-MOSFET

The major problems of planner DG MOSFET are 1) definition of both gates to the same image size accurately, 2) self-alignment of the source/drain regions to both top and bottom gates, and alignment of the two gates to one another[4][5]. The DG FinFETs (built on bulk silicon or SOI wafers) among 3-D devices are very promising candidate for future nano-scale CMOS technology and high-density memory application[6]as in Fig1.2.The Process technology of FinFET is easy and compatible with conventional fabrication process.

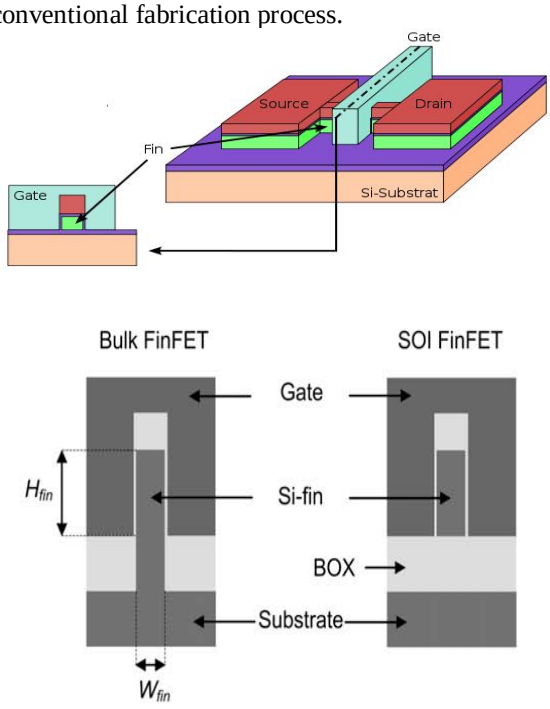

Fig. 1.2 : Finfet 3-D structure and cross-sectional view

Structurally bulk FinFETs and SOI FinFETs are similar except for the fact that bulk FinFETs use an isolation oxide layer (SiO_2) between the gate electrode bottom and the bulk Si surface to avoid gate electrode contacting the Si wafer (as shown schematically in Fig1. 2.

The sailient features of Bulk DG FINFETs over SOI DG FINFET are low wafer cost, low defect density, less back gate-bias effect, high heat transfer rate to substrate and good process compatibility. Most of the bulk FinFET processes reported using a large

isolation oxide to reduce the parasitics. The bulk FinFETs use a heavy fin doping to control the OFF-state leakage, which causes a significant mobility degradation.[7].

II. DEVICE SIMULATION AND RESULT:

Sentaurus TCAD simulation tool is used for different MOSFET structures from Single gate to Multi-gate FINFET (bulk and SOI structure)[8]. With the scaling trend in device dimension it is required to limit short channel effects(SCE) and therefore high channel doping is used .But it has adverse effect of lower carrier mobility,high tunneling effect , degrades subthreshold performance and larger parasitic capacitance.It is observed that for single gate MOSFET the subthreshold slope changes with the change in doping level while in FD SOI MOSFET structure, the subthreshold slop is independent of cannel doping as in Fig2.1&2.2

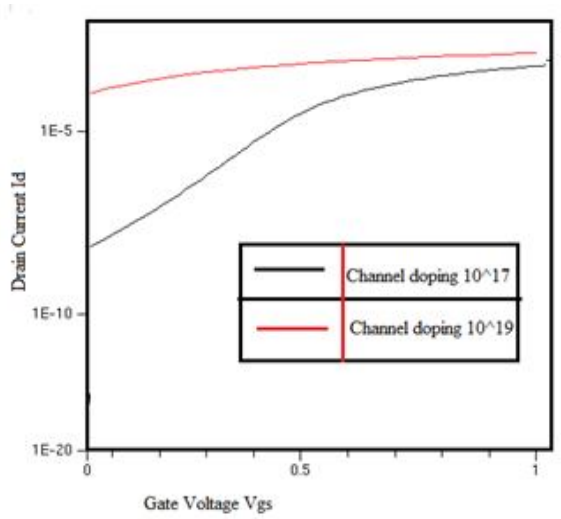

Fig. 2.1: Dependence of subthreshold slope on channel doping

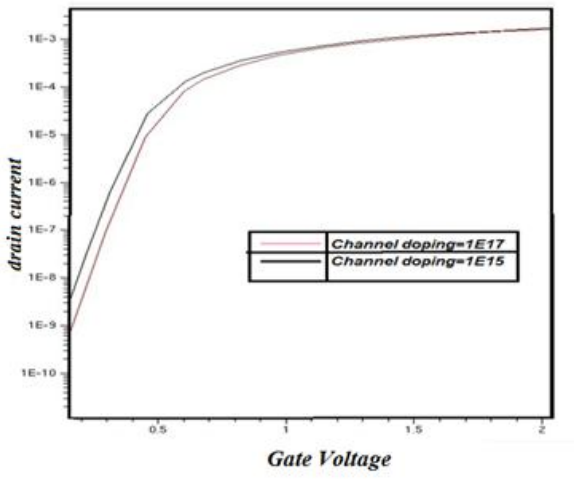

Fig. 2.2 : Subthreshold behavior of FD-SOI under different channel doping

The Simulation results shows the comparative analysis of SOI FINFET and Bulk FINFET for different profile.

DG SOI FINFET:

To study the characteristics varition of SOI FINFET a schematic cross-sectional view of the SOI FINFET is simulated using 3-D Sentaurus device simulator [8], is shown in fig2.3 In this structure the channel length is 65nm,Fin hight is 60nm and metal gates are separated with channel 20nm thick oxide layer

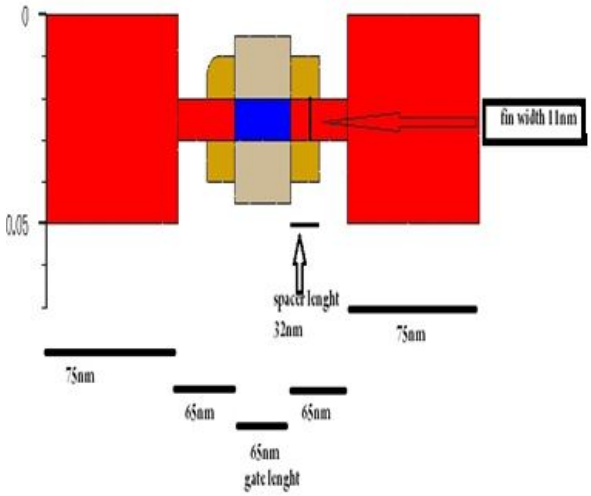

Fig. 2.3 : Device Structure

SOI FinFET is fully depleted SOI MOSFET with dual gate . It shows nearly ideal characteristics. With the help of 3-D device simulation we have obtained the subthreshold and transfer characteristics between drain current and gate voltage of DG SOI FINFET for different channel doping.Fig2.4.Simulation result of SOI FINFET is also compared with Bulk FINFET.

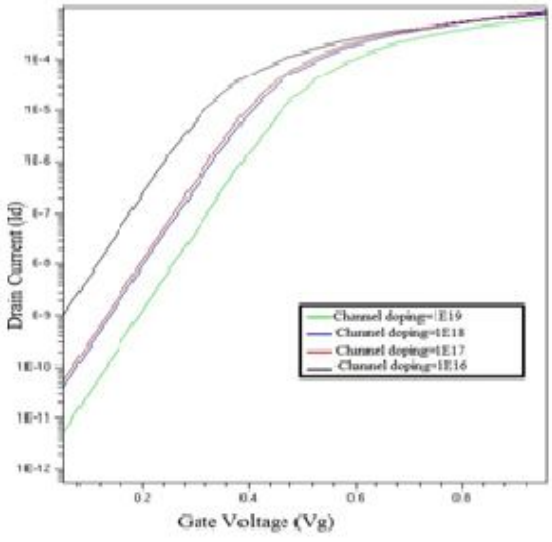

Fig. 2.4 : SOI-FinFET subthreshold characteristics

The subthreshold slope and DIBL are also plotted with the variation in channel doping. It is observed that Subthreshold characteristics is nearly independent from channel doping and DIBL reduces gradually as channel doping increases(Fig2.5&2.6).

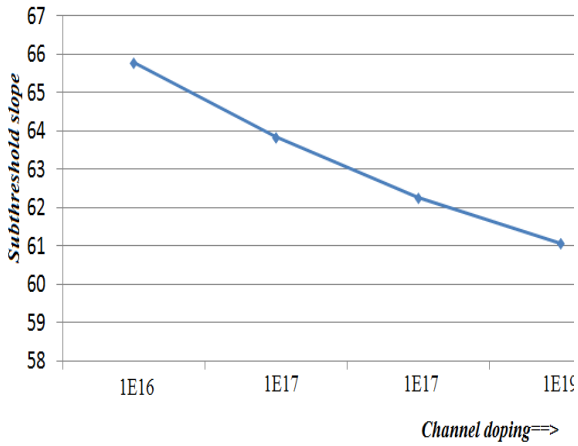

Fig. 2.5 : Subthreshold slope (in mv/decade) of SOI-FinFET under different doping conditions

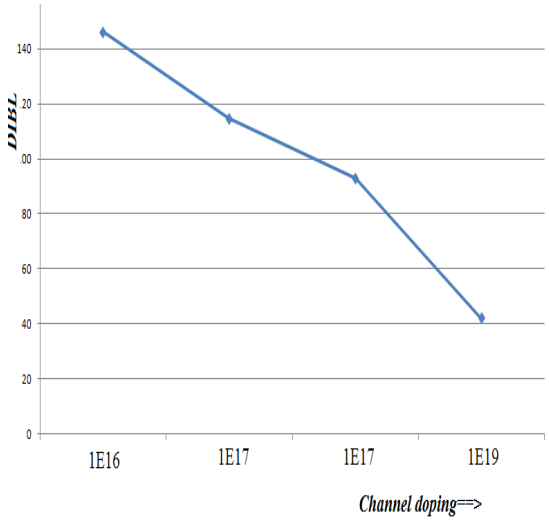

Fig. 2.6 : DIBL(in mV/V) of SOI-FinFET under different doping conditions

Bulk DG FINFET:

The bulk DG FINFET is simulated for diffrent doping profile structure for performance comparision as in Fig2.7. The transfer and subthreshold characteristics are plotted with the variation of gate voltage for different doping profile(Fig2.8&2.9).

Bulk FINFETs were compared with SOI FINFETs with nearly the same device scalability better wafer quality and characteristics regarding the body connected to substrat. In this paper the Bulk FinFET realized by using spacer technology.

Junction isolated Bulk-FINFET can potentially match SOI in terms of subthreshold(Vth) leakage control, but doping optimization can be complex.

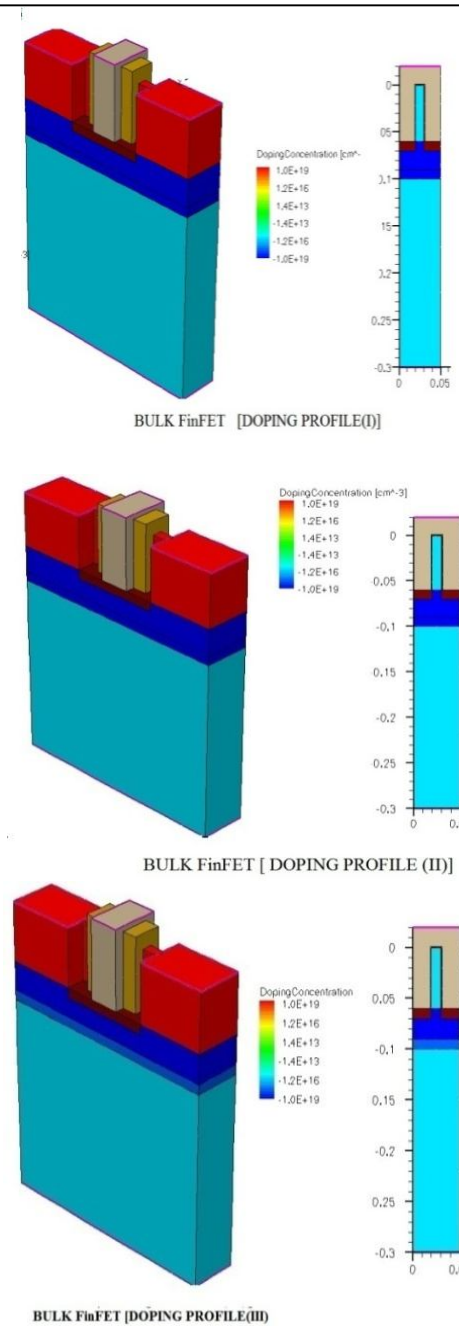

Fig. 2.7 : Device structure

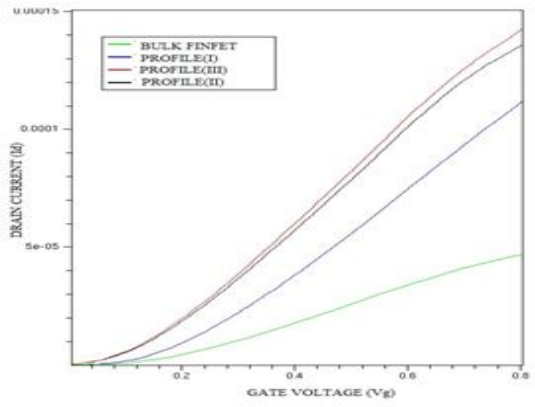

Fig. 2.8 : Transfer Characteristics Of different Bulk profile

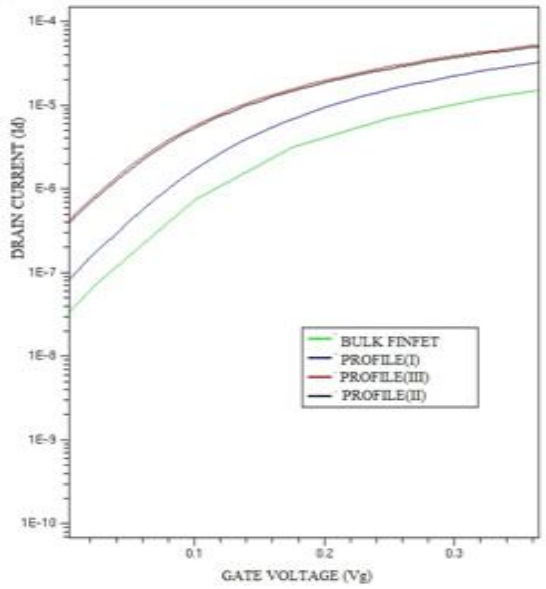

Fig. 2.9 : Subthreshold characteristics of different Bulk profile

Simulation result shows that Bulk FINFET has high value of subthreshold slope as compared to SOI FINFET but the value of SS is different for different profile structure indicating minimum value with profile(II) as shown in Table1.

Table 1: Performance comparison between SOI FINFET and Bulk FINFET of different profile

Type	SOI-FinFET	Bulk FinFET	Profile		
			I	II	III
SS	64	89.28	80.7	74.02	84

We have also obtained Bulk transfer and subthreshold characteristics for different doping level on 32nm technology.Fig2.10,2.11.

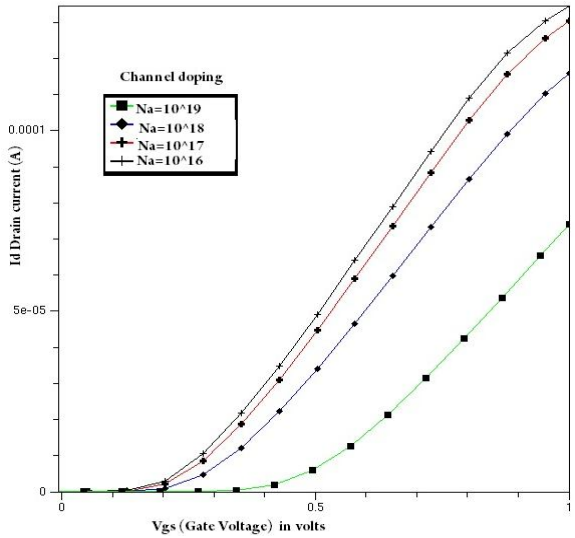

Fig. 2.10 : Bulk FINFET Transfer characteristic for 32nm channel length.

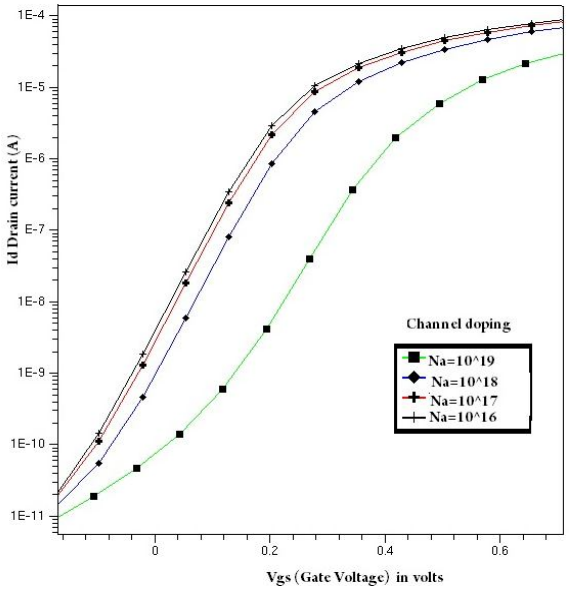

Fig. 2.11: Bulk FINFET subthreshold characteristics for 32nm channel length.

III. CONCLUSION:

The performance characteristics of DG SOI FINFET and BULK DG FINFET are compared for different gate voltages. The Bulk DG FINFET is furthure analysed with diffrent doping profile.SOI-FinFET gives superior performance over bulk FinFET. But proper designing and optimization of bulk FinFET (using profile(II)) results in better short channel effects, which makes it a strong candidate for bulk FinFET design.

REFERENCES:

[1] "Into The Nano Era" Moore's Law Beyond Planar Silicon CMOS by Howard R. Huff

[2] "SOI vs. Bulk FinFET: Body Doping and Corner Effects Influence on Device Characteristics" Mirko Poljak, Vladimir Jovanović, and Tomislav Suligoj, IEEE ,2008

[3] "Turning silicon on its edge [double gate CMOS/FinFET technology]" Circuits and device magazine IEEE ,Jan-Feb 2004, E.J.; Aller, I.; Ludwig, T.; Kim, K.; Joshi, R.V.Wong, H.-S. P.;

[4] "Beyond the conventional transistor " IBM journal of Research and development March 2002; [5] "FinFET—A self-aligned double-gate MOSFET scalable to 20 nm" IEEE Trans. Electron. Devices, ,Dec. 2000. D. Hisamoto, W. C. Lee, J. Kedzierski, J. Bokor, and C. Hu

[6] "Fin-Array-FET on bulk silicon for sub-100nm trench capacitor DRAM," VLSI Tech. Digest, Jun 2003. R. Katsumata, N. Tsuda, J. Idebuchi, M. Kondo, N. Aoki, S. Ito, K.Yahashi, T. Sanotaka, M. Morikado, M. Kito, M. Kido, T. Tanaka, H.Aochi, and T. Hamamoto

[7] "Device Design and Optimization Considerations for Bulk FinFETs" IEEE TRANSACTIONS ON ELECTRON DEVICES, FEBRUARY 2008. C. R. Manoj, Meenakshi Nagpal, Dhanya Varghese, and V. Ramgopal Rao

[8] "Sentaurus Structure Editor User's Manual", Synopsys International.