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IMPLEMENTATION OF ROBUST ARCHITECTURE FOR ERROR DETECTION AND DATA RECOVERY IN MOTION ESTIMATION ON FPGA

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Abstract- Video compression is necessary in a wide range of applications to reduce the total data amount required for transmitting or storing video data. Among the coding systems, Motion Estimation is of priority concern in exploiting the temporal redundancy between successive frames, yet also the most time consuming aspect of coding. This paper presents an error detection and data recovery (EDDR) design, based on the residue-and quotient (RQ) code that is embed into ME for video coding testing applications. Based on the Concurrent Error Detection (CED) concept, this work develops a robust EDDR architecture based on the RQ code to detect errors and recovery data in PEs of a ME and, in doing so, further guarantee the excellent reliability for video coding applications. We synthesized this design using Xilinx tool.

Keywords: *Concurrent Error Detection, Motion Estimation, Residue quotient code generation.*

I. INTRODUCTION

At its most basic level, compression is performed when an input video stream is analyzed and information that is indiscernible to the viewer is discarded. Each event is then assigned a code – commonly occurring events are assigned few bits and rare events will have more bits. These steps are commonly called signal analysis, quantization and variable length encoding respectively. There are four methods for compression; discrete cosine transforms (DCT), vector quantization (VQ), fractal compression, and discrete wavelet transform (DWT). Discrete cosine transform is a lossy compression algorithm that samples an image at regular intervals, analyzes the frequency components present in the sample, and discards those frequencies which do not affect the image as the human eye perceives it. DCT is the basis of standards such as JPEG, MPEG, H.261, and H.263.

Advance Video Coding is widely regarded as the next generation video compression standard. So, video compression is necessary to reduce the total data amount required for transmitting or storing video data. Among the coding systems, a ME is of priority concern in exploiting the temporal redundancy between successive frames, yet also the most time consuming aspect of coding. Additionally, while performing up to 60%–90% of the computations encountered in the entire coding system, a ME is widely regarded as the most computationally intensive of a video coding system. To explore the feasibility of a BIST to detect errors and recover data of a ME is of worthwhile interest. Additionally, the reliability issue of numerous PE's in a ME can be improved by enhancing the capabilities of concurrent error detection (CED). CED can also test the circuit at full operating speed without interrupting a system. - Based on the CED concept, this work develops a robust EDDR architecture based on the RQ code, to detect errors and recovery data in PEs of a ME. This guarantees the excellent reliability for video coding testing applications.

II. SYSTEM MODEL

The proposed EDDR architecture is as shown in Fig.1. Which comprises two major circuit designs, i.e. data recovery circuit (DRC),to detect errors and recover the corresponding data in a specific PE and error detection circuit (EDC).

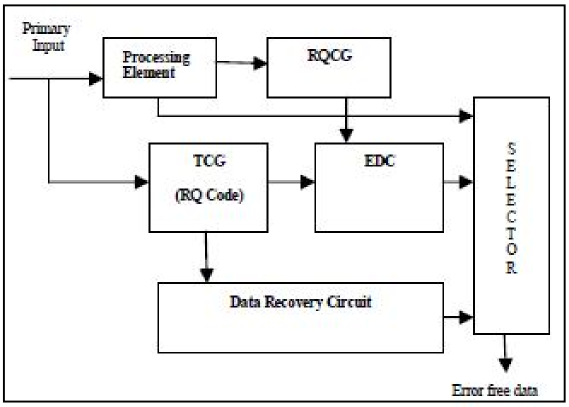


Fig.1. Conceptual View of the Proposed EDDR architecture

The test code generator (TCG) utilizes the concepts of RQ code to generate the corresponding test codes for errordetection and data recovery. In other words, the test codes from TCG and the primary output from CUT are delivered to EDC to determine whether the CUT has errors. DRC is in charge of recovering data from TCG. Additionally, a selector is enabled to export error-free data or data-recovery results.

Importantly, an array-based computing structure, such as ME, discrete cosinetransform (DCT), iterative logic array (ILA), and finite impulse filter (FIR), is feasible for the proposed EDDR scheme to detect errors and recover the corresponding data.

III. SYSTEM DESIGN

A. PROCESSING ELEMENT

A ME consists of many PE's incorporated in a 1-D or 2-D array for video encoding applications. It consists of PEs with a size of 4X4.Fig.2. shows the internal structure of PE. A PE generally consists of two ADDs (i.e. an 8-bit ADD and a 12-bit ADD) and an accumulator (ACC). Next, the 8-bit ADD (a pixel has 8-bit data) is used to estimate the addition of the current pixel (Cur_pixel) and reference pixel (Ref_pixel). Additionally, a 12-b ADD and an ACC are required to accumulate the results from the 8-b ADD in order to determine the sum of absolute difference (SAD) value for video encoding applications.

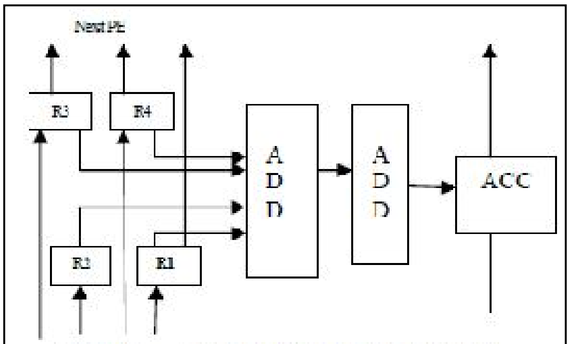


Fig 2. Internal Structure of Processing Element

Notably, some registers and latches exist in ME to complete the data shift and storage applications. The PEs is essential building blocks and are connected regularly to construct a ME. Generally, PE's issurrounded by sets of ADDs and accumulators that determine how data flows through them. Additionally, the visual quality and peak signal-to-noise ratio (PSNR) at a given bit rate are influenced if an error occurred in ME process. A testable design is thus increasingly important to ensure the reliability of numerous PEs in a ME.PEs can thus be considered the class of circuits called ILAs, whose testing assignment can be easily achieved by using the fault model, cell fault model (CFM). Using CFM has received considerable interest due to accelerated growth in the use of high-level synthesis, as well as the parallel increase in complexity and density of integration circuits.

B. RQ CODE GENERATION

To detect circuit errors in design applications coding approaches such as parity code, Berger code, and residue code have been considered. Residue code is generally separable arithmetic codes by estimating a residue for data and appending it to data. Error detection logic for operations is typically derived by a separate residue code, making the detection logic is simple and easily implemented. However, only a bit error can be detected using residue code.

Therefore a quotient code which is derived from the residue code, to help the residue code in detecting errors and recovering the data. If the input data is represented as X bits, the binary data is expressed as

$$X = \{b_{n-1}b_{n-2}\dots\dots\dots\dots\dots\dots b_2b_1b_0\} = \sum_{i=0}^{n-1} b_i\, 2^i \quad (1)$$

To accelerate the circuit design of RQCG, the binary data in (1) can generally be divided into two parts:

$$\begin{aligned} X &= \sum_{i=0}^{n-1} b_i\, 2^i \\ &= \left(\sum_{i=0}^{k-1} b_i 2^i\right) + \left(\sum_{i=k}^{n-1} b_i 2^{i-k}\right) 2^k \\ &= Y_0 + Y_1 2^k \end{aligned} \quad (2)$$

Significantly, the value of k is equal to $n/2$. The modulus value i.e. $m = 2^k - 1$. The residue code is given by

$$R = |X|m \quad (3)$$

$$Q = \left\lfloor \frac{X}{m} \right\rfloor \quad (4)$$

Based on the equations, the corresponding circuit design of RQCG is easily realized. The basic architecture of RQ code is in Fig.3.

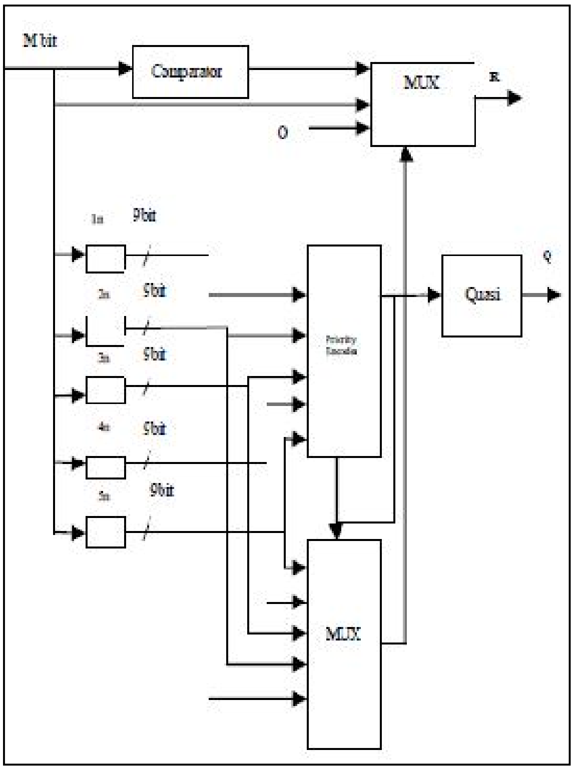
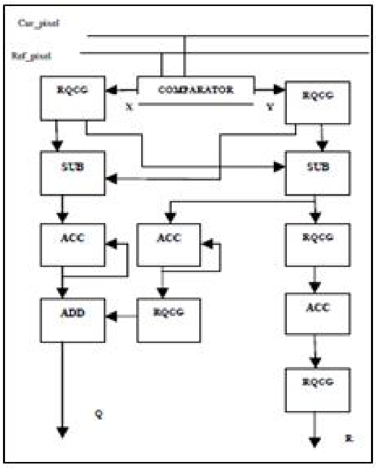


Fig.3. Residue Quotient Code Generator

The main elements of RQCG are the priority encoder and the multiplexer. These elements generate the quotient value by passing through a Quasi. The residue value is obtained directly by the comparator.

C. TEST CODE GENERATION

The important component of the TCG design is the RQCG circuit.TCG design is based on the ability of the RQCG circuit to generate corresponding test codes in order to detect errors and recover data. The specific PE estimates the absolute difference between the Cur_pixel of the search area and the Ref_pixel of the current macro block. The absolute difference is obtained based on SAD (Sum of Absolute Difference). The TCG consists of 5 RQCG block and comparator, accumulators and subtractors.



D. SAD TREE

The SAD of a macro block with the size NXNcan be compute as follows:

$$\mathrm{SAD} = \sum_{i=0}^{N-1}\sum_{j=0}^{N-1}|X_{ij} - Y_{ij}| = \sum_{i=0}^{N-1}\sum_{j=0}^{N-1}|(q_{xij}.m + r_{xij}) - (q_{yij}.m + r_{yij})| \quad (5)$$

The 2-D intra-level architecture called the Propagate Partial SAD is better suited for the absolute difference evaluation. The architecture of SAD is shown in Fig.5. The SAD is composed of PE arrays with a 1-D adder tree in the vertical direction. Current pixels are stored in each PE, and two sets of continuous reference pixels in a row are broadcasted to PE arrays at the same time.

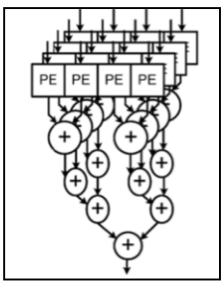


Fig.5. Propagate Partial SAD

In each PEarray with a 1-D adder tree, distortions are computed and summed by a 1-D adder tree to generate one-row SAD. The row SADs are accumulated and propagated with propagation registers in the vertical direction. The reference data of searching candidates in the even and odd columns are inputted by Ref_pixel 0 and Ref_pixel 1, respectively. After initial cycles, the SAD of the first searching candidate in zero columns is generated, and the SADs of the other searching candidates are sequentially generated in the following cycles. When computing the last searching candidates in each column, the reference data of searching candidates in the next columns begin to be inputted through another reference input.

In Propagate Partial SAD, by broadcasting reference pixel rows and propagating partial-row SADs in the vertical direction, it provides the advantages of fewer reference pixel registers and a shorter critical path. Since Rt(Qt) is equal to RPEi (QPEi) EDC is enabled and a signal “0” is generated to describe a situation in which the specific PEi is error-free. Conversely, if SA1 and SA0 errors occur in bits 1 and 12 of a specific PE i.e. the SAD value of PEi= 2124. Distortion is the difference between the current pixel and the reference pixel, and SAD is the total distortion of this searching candidate. The row column) SAD is the summation of distortions in a row (column). After all searching candidates are examined; the searching candidate that has the smallest SAD is selected as the motion vector of the current macro block.

E. CONCURRENT ERROR DETECTION (CED)

Thevisual quality and peak signal-to-noise ratio (PSNR) at a given bit rate are influenced if an error occurred in ME process. While the extended BIST schemes generally focus on memory circuit, testing-related issues of video coding. Thus, exploring the feasibility of an embedded testing approach to detect errors and recover data of a ME is of worthwhile interest. So, the reliability issue of numerous PE’s in a ME can be improved by enhancing the capabilities of concurrent error detection (CED).

The CED approach can detect errors through conflicting and undesired results generated from operations on the same operands. This scheme can also test the circuit at full operating speed without interrupting a system. Hence, based on this concept, a robust EDDR architecture can be achieved based on the RQ code to detect errors and recovery data in PEs of a ME.

This further guarantees the excellent reliability for video coding testing applications. However, only a bit error can be detected based on the residue code. Additionally, an error can’t be recovered effectively by using the residue codes. Therefore, a quotient code which is derived from the residue code to assist the residue code in detecting multiple errors and recovering errors. The corresponding circuit architecture of the RQCG is easily realized and the RQ code can be generated with a low complexity and little hardware cost. Concurrent test methods enable integrated circuits to verify the correctness of their results during normal operation. Quality assessment of concurrent test methods relies on several parameters, including the model of detectable faults or errors, the worst-case detection latency, and the incurred area overhead. Several low-cost, non-intrusive, concurrent fault detection (CFD) methods have been proposed for stuck-at faults in combinational circuits.

In the R-CBIST method, the requirement for input combinations is relaxed at the cost of a small RAM. Alternatively, latency is reduced.

IV. ERROR DETECTION AND DATA RECOVERYPROCESS.

To detect errors and recover the corresponding data in a specific ME our EDDR architecture, which comprises two major circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC) is sufficient. The test code generator utilizes the RQ code to generate the corresponding test codes for error detection and data recovery.

The test codes from TCG and the primary output are delivered to EDC to determine whether the input has errors. DRC is in charge of recovering data from TCG. A selector is enabled to export error-free data or data-recovery results. Inorder todetermine whether errors have occurred,the outputs between TCG and RQCG is compared. The errors in a specific PE can be detected when the values of $R_{PE} \neq R_T$ and similarly the quotient values. 0/1 signal is generated by error detecting circuit to indicate the error. The lost data can be recovered by DRC.

This plays an important role in recovering RQ code from TCG. The mathematical model for data recovery is

$$\mathrm{SAD} = m \times Q_T + R_T$$

$$= (2^i - 1) \times Q_T + R_T$$

The Barrel shift and Corrector circuits are necessary to achieve the functions $2^i \times Q_T$ and $-Q_T + R_T$ respectively for data recovery.

V. RESULTS

Extensive verification of the circuit design is performed using the Verilog and then synthesized by the Xilinx9.2 to demonstrate the feasibility of the proposed EDDR architecture design for ME testing applications.

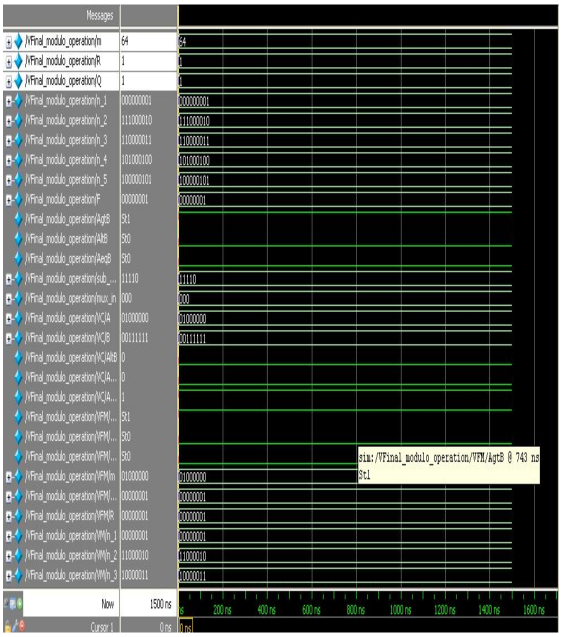


Fig. 6.1 Simulation results of RQCG

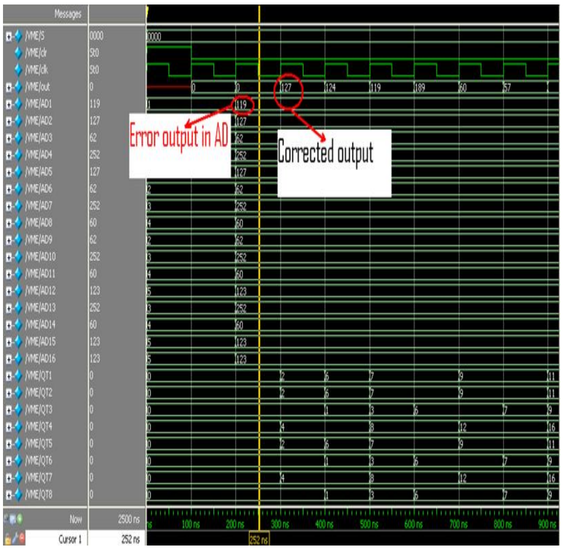


Fig. 6.2 Simulation results of EDDR

VI. CONCLUSION

We presented an efficient RQCG architecture for a error detection and data recovery in MEfor video coding testing applications.Simulation results shows that the proposed design detects the errors and recovers the data. An error in processing elements key components of a ME can be detectedand recovered effectively by using the proposed EDDR design.

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