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Shobhanjana Kalita
Department of Electronics and communication Engineering, Tezpur University, Tezpur-784028, Assam, shashi1@tezu.ernet.in

S. BABU
Department of Electronics and communication Engineering, Tezpur University, Tezpur-784028, Assam, s.babu@gmail.com

P.P. SAHU
Department of Electronics and communication Engineering, Tezpur University, Tezpur-784028, Assam, pps@tezu.ernet.in

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S.KALITA, S.BABU, P.P.SAHU

[1,2&3]Department of Electronics and communication Engineering, Tezpur University, Tezpur-784028, Assam
E-mail: shashi1@tezu.ernet.in

Abstract- This paper presents the design of a clock and data recovery circuit having a high data rate of 9.95328 Gb/s by using delay locked loop with Switched Capacitor (SC) filter to improve the jitter transfer function and jitter tolerance as it has high Q and low center frequency. From the results it is seen that the besides the conventional DLL circuit , the circuit using SC filter of f_c= 311.04 MHz and Q=500 provides very low cut off frequency.

Keywords- *Switched Capacitor filter; Delay locked loop; VCDL.*

I. INTRODUCTION

The clock synchronization and bit synchronization problem is an important issue for design of a wireless communication system as well as wired communication system, which can be solved by using a data recovery circuit. The circuit uses either phase locked loop (PLL) or delay locked loop (DLL). The DLL's [1] are considered more stable than PLL's since they employ a first order loop filter than a second order one in PLLs [2,3,4] Also noise is not accumulated over cycles in the voltage controlled delay lines (VCDL) whereas it is re-cycled in an oscillator in PLLs . In modern wireless and optical communication, SAW filters are generally used. To solve the problem of limited phase capture and uncontrollable loss of lock and self correcting circuit [1] , Kiyoshi Ishii and Keiji Kishine used SAW filter for design of a 2.48832 gb/s clock and data recovery circuit [2] as a jitter suppression technique. Further the improvement in jitter transfer characteristics was shown by P.P.Sahu using Saw filter [5]. This filters offers high Q factor and high selectivity but the problems with these filters are high insertion losses, off chip and is not tunable over wide range of frequencies and also their costs are more[6].

In this paper we have designed and simulated a fully integrated high-Q band pass filter for clock recovery circuit by filtering harmonic components for 9.95328 Gb/s non return zero (NRZ) data transmission using Microsim EDA software release 8. Using this SC filter the jitter transfer function can be improved.

II. ARCHITECTURE

Figure 1. shows the block diagram of a proposed data recovery circuit. The main blocks of this circuit includes delay locked loop, frequency divider, SC filter, frequency multiplier and decision or sample and hold circuit. The synchronized clock signal is extracted from the reference clock and input NRZ data by the delay locked loop. The frequency divider converts the clock signal to the centered frequency (f_c) of the switched capacitor filter. The high Q factor SC filter works at low frequency to achieve better performance. The low frequency clock signal converted to original clock signal frequency by frequency multiplier which triggered the decision circuit to recover the data with low jitter.

A. Delay locked loop

The block diagram of a conventional DLL as shown in Figure 1 consists of a voltage controlled delay line (VCDL), a phase detector , a charge pump and a low pass filter (LPF).DLLs have been used to generate on chip clocks in microprocessor, memory interfaces, and communication integrated circuits. The phase detector detects the phase error between the output data signal of the delay line and input reference clock which generates an up and down signal which are integrated by charge pump and low pass filter to generate a control voltage (V_{ctrl}) for voltage control delay line. To solve the problem of harmonic locking or false locking over operating range the delay (T_d) of VCDL should have maximum and minimum limits. When control voltage (V_{ctrl}) is minimum T_{dmax} must locate between T_{clk} and (3/2)T_{clk} and when V_{ctrl} is maximum T_{dmin} must be located between (½) T_{clk} and T_{clk} [7].

To see the transfer function of DLL we assume a reference clock available exactly at the correct frequency and the input data is delayed through variable voltage delay line (VVDL) a time T_d until it is synchronized with the reference clock.

The transfer function of VVDL $\emptyset_{clock}/\emptyset_{out}$ is zero and so the phase of reference clock is taken as the reference for other signals ie. Φ_{clock}=0.
The phase of input data is related to the phase of output by $\emptyset_{out}=\emptyset_{in}+T_d.2\pi f.clock$ (1)

$\emptyset_{out}=\emptyset_{in}+T_d.2\pi/(T_{clock})$ (2)

Or $\emptyset_{out}=\emptyset_{in}+T_d.\omega clock$ (3)

Where $\emptyset_{in}$ = phase of input data, $\emptyset_{out}$ = phase of output data, $\emptyset_{clock}$= phase of reference clock and T_{clock}= period of reference clock or half of the period of the data in for a string of alternate ones and zeros.

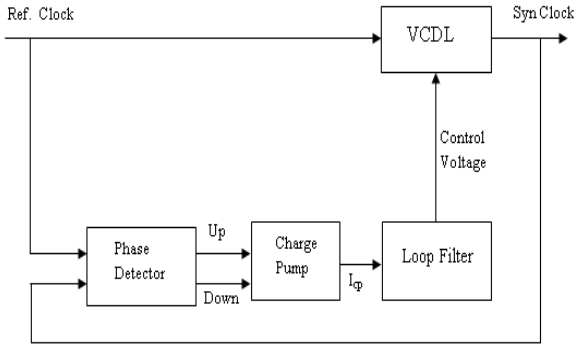

Figure 1. Block diagram of conventational DLL

The gain of VCDL can be expressed in term of delay T_d as

$$T_d=K\nu.V_{ctrl} \quad (4)$$

Where V_{ctrl} = control voltage input to VCDL from loop filt $=\emptyset_{out}.K_d.K_f$ (5)
and $K\nu$ = gain of VCDL and has the units of seconds/v, K_d = gain of phase detector, K_f = gain of loop filter.

So the overall transfer function of VCDl can be expressed as

$$\emptyset_{out}=\emptyset_{in}+T_d.\omega clock$$
$$\emptyset_{out}=\emptyset_{in}+Kv.V_{ctrl}.\omega clock$$
$$= \emptyset_{in}+Kv.\emptyset_{out}.K_d.K_f.\omega clock$$
$$\emptyset_{out}/\emptyset_{in} = 1/(1-Kv.K_d.K_f.\omega clock) \quad (6)$$

Now the gain (K_d) of self correcting phase detector if up signal (UP) and down signal (DN) occurs at the same time then

$$K_d= -I_{pump}/\pi \quad (amp/rad) \quad (7)$$

And the gain (K_f) of first order loop filter is,

$$K_f=1/sC \quad (8)$$

The transfer function of DLL can now be written as

$$\emptyset_{out}/\emptyset_{in} = 1/(s+Kv.(2.I_{pump})/(C.T_{clock})) \quad (9)$$

The frequency of the reference clock must be exactly related to the frequency of the input data by $\Delta\emptyset_{in}/s$ then the change in output voltage is given by

$$\Delta\emptyset_{out}=\nabla\emptyset_{in}/(s+Kv.(2I_{pump})/(C.T_{clock})) \quad (10)$$

Where s=jω=complex frequency

The time taken by DLL to respond to an input step in phase is given by

$$T_r=2.2*(C.T_{clock})/(Kv.2I_{pump})$$
$$= \text{no of clock cycles} * T_{clock} \quad (11)$$

The time taken by DLL to respond to an input step in phase can be decreased by making C/I_{pump} small and with the reduction of this the jitter increases. Variation of V_{ctrl} with C/I_{pump} is shown in Figure 2. Which shows that with lower values of C/I_{pump} , V_{ctrl} decreases non linearly and with higher values of C/I_{pump} , V_{ctrl} decreases slowly and linearly. Since a given ripple on the control voltage of the VCDL will have a lager effect on the delay, jitter will increases by increasing the gain Kv.

VCDL is an important part of delay locked loop which does not amplify or generate a signal but delays the clock/data signals using the adjustable delay inverters and the for proper operation VCDL should must satisfy the following conditions[7,8]:

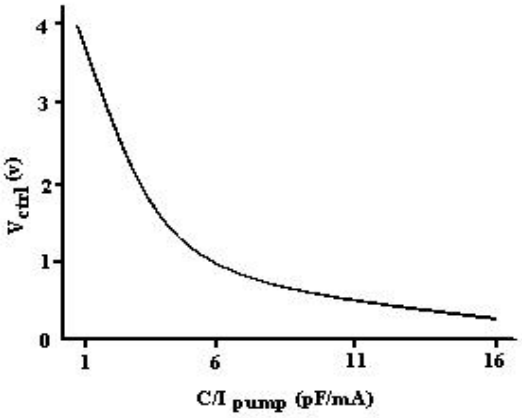

Figure 2. Design and Implementation of a High Speed Clock and Data Recovery Delay locked loop using SC filter

$$½\ T_{clock}<T_{d\ min})<T_{clock} \quad (12)$$
$$T_{clock}<T_{d\ max}\ <3/2\ T_{clock} \quad (13)$$

Where T_{clock} is the period of reference clock. Now in terms of T_{clock} the above equations can be written as,

$$\text{Max}\ (T_{dmin}\ ,\ (2/3)\ T_{dmax}\ ) <T_{clock} < \text{Min}\ (2.T_{dmin}, T_{dmax}\ ) \quad (14)$$

when $T_{dmax}= 2.T_{dmin}$ then the above inequality will becomes

$$(2/3)\ T_{dmax}\ <T_{clock}<T_{dmax}$$

We have implemented VCDL using shunt capacitor delay stage where each delay element comprises of inverter with variable load which are controlled by control voltage (V_{ctrl}) which is generated by charge pump. Now if the phase of the sync clock has large time period compared to the reference clock, the control voltage (V_{ctrl}) increases which increases the current through delay cell and decreases the delay of each delay element and thus the overall time period of output clock phases decreases to match the reference clock period. Once the loop is locked, control voltage remains stable. So the delay given by each cell can be expressed as,

$$T_{delay}=Kv.V_{ctrl} \quad (15)$$

Where Kv is the gain of VCDL and has the units of seconds/V and V_{ctrl} is voltage input to VCDL from loop filter.

Figure 4. shows the variation of delay of voltage control delay line with control voltage (V_{ctrl}) at different N, where N is the no of inverters. For the data rate of 9.95318 gb/s, the delay should be in between from 0.05ns to 0.15ns to avoid any false lock[7].

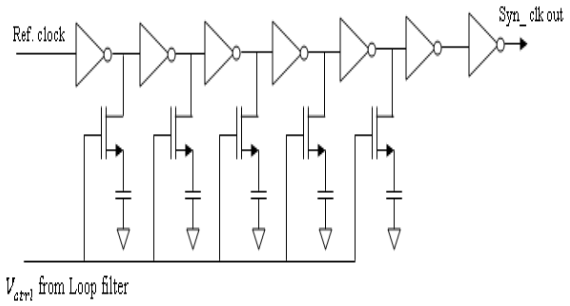

Figure 3. Shunt capacitor inverter delay

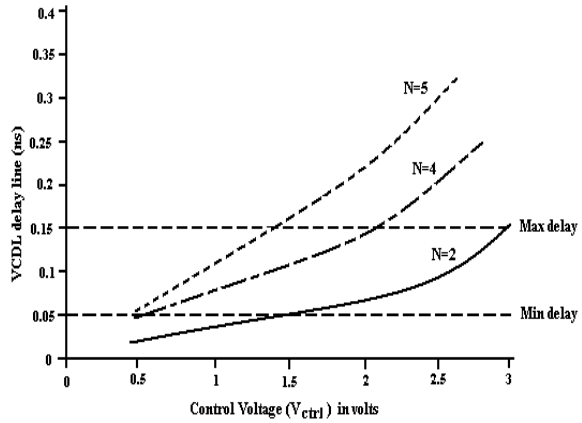

Figure 4. Variation of VCDL delay with control voltage (V_{ctrl}) in volts

III. JITTER TRANSFER FUNCTION

The jitter transfer function depends on the characteristics of SC filter as we are using SC filter here as a band pass filter whose transfer function can be expressed as [2],

$$H(f)=1/(1+j(f/B)) \quad (16)$$

where $B=f_c/2Q$, f= cut off frequency, f_c= center frequency, B = half band width of filter, $Q=\pi NRCf_c$ (in first approximation) for SC filter and N= number of delay cell.

The Q factor of SC filter depends upon the number of branches, value of R and C and the center frequency. For achieving Q factor ≈ 500, we have kept value of R= 1KΩ, C= 50pF for 8 braches. Figure 5. Shows the variation of cutoff frequency with Q factor at different center frequencies of SC filter and is evident from the figure that as the Q increases, cutoff frequency decreases. Jitter cut off frequency around 300 kHz has been achieved at Q= 500 and fc = 311.04MHz. By keeping multiplication factor as 32, the center frequency of the filter can be kept at 311.04MHz and the data rate of our proposed circuit is 9.95328MHz. Calculated jitter function of with SC filter and without SC filter considering Q factor at 1000 is shown in Figure 6. From the Figure it is evident that as the center frequency of the filter decreases the jitter cut off frequency also decreases and the lowest jitter cutoff frequency is given by the center frequency of f= 311.04 MHz at data rate of 9.95328 MHz. Figure 6. Shows the jitter transfer function for the proposed CDR system which is compared with the existing CDR using SAW filter (Q=1000). We have seen that the the jitter cut off frequency for our proposed CDR is 300KHZ compared to that of exisiting which is about 600KHz.

IV. FREQUENCY MULTIPLIER

The purpose of frequency multiplier in the proposed clock and data recovery circuit is to convert the output signal of SAW or SC filter into the high frequency clock signal.the proposed frequency multiplier uses simple exclusive-or (XOR) gates, delay elements and phase blending technique for frequency multiplication[7].

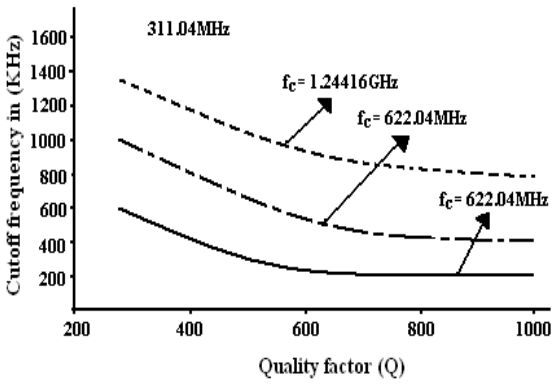

Figure 5. Variation of cutoff frequency with Q factor at different f_c of S-C filter

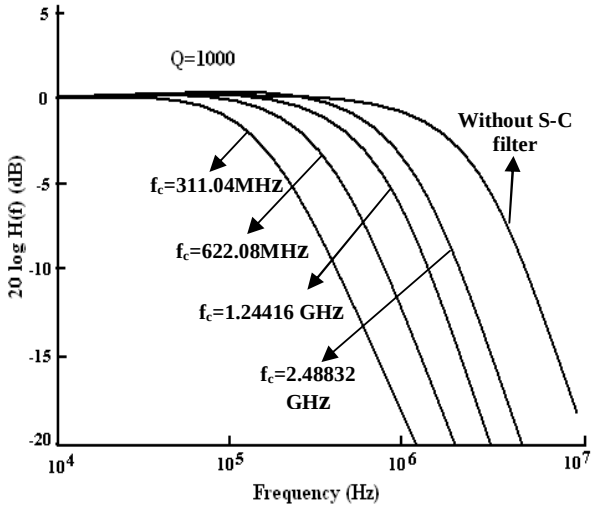

Figure 6. Calculated jitter transfer function with and without S-C filter at different center frequencies when quality factor (Q) of filter is 1000

V. USING THE TEMPLATE

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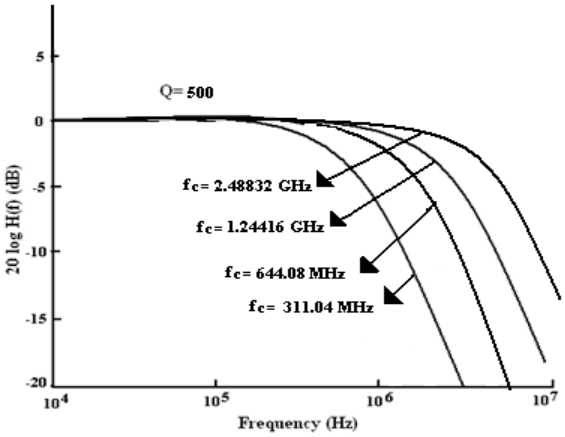
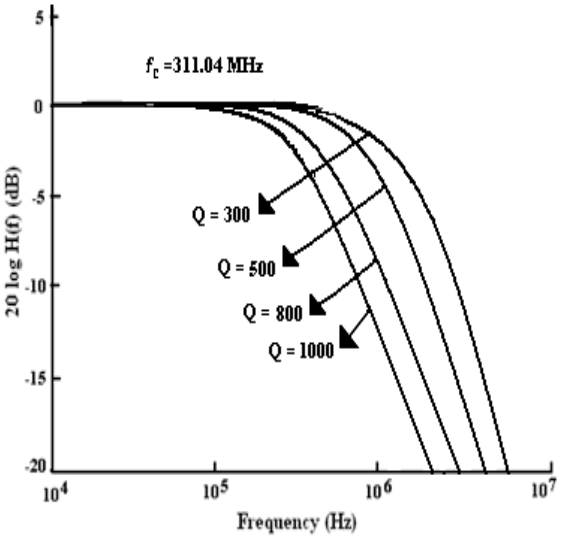


(a)



(b)

Figure 7. Calculated jitter transfer function (a) when Q factor of filter is at 500 (b) Center frequency (f_c)of filter is 311.04 MHz [5]

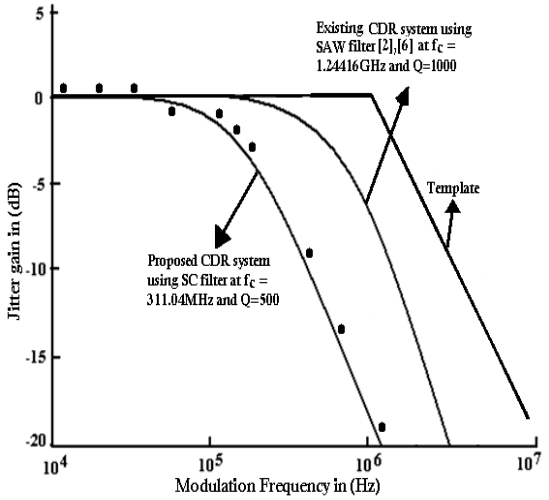


Figure 8. Jitter gain vs modulation frequency curve for existing and proposed CDR system. Black dots in the graph indicates the experimental values

The frequency multiplier can generate an output frequency that is N times of input frequency. The N is the number of phases of the input clock which is an even and N≥2. The output clock (OUT_{clock}) can be expressed as, OUT_{clock} = Nx REF_{clk} , where the REF_{clk} is the reference input clock and the OUT_{clk} is the multiplied output clock. The frequency multiplier generates four sets of 2x REF_{clk} , two sets of 4xREF_{clk}, two sets 8xREF_{clk} and one set of 16xREF_{clk} .

VI. DECISION CIRCUIT

Decision circuit recovers the distorted binary data by retiming the noisy input data signal using the recovered/synchronized clock signal from the output of frequency multiplier. The decision circuit in the clock and data recovery circuit is built by D-latch circuit which is implemented by 4 static logic NAND gate. The D port of the D-flip flop is connected with the input NRZ signal and clock port of the D-Flip flop is connected with synchronized (syn) clock signal. When clock is high the data signal propagates directly through the circuit from the input D to the output Q. the rising edge of the synchronized clock coincides with the mid point of each data bit which allows the optimum sampling of data bits by clock. This optimum sampling reduces the jitter propagation. Now the output of decision circuit is retimed data with reasonable jitter.

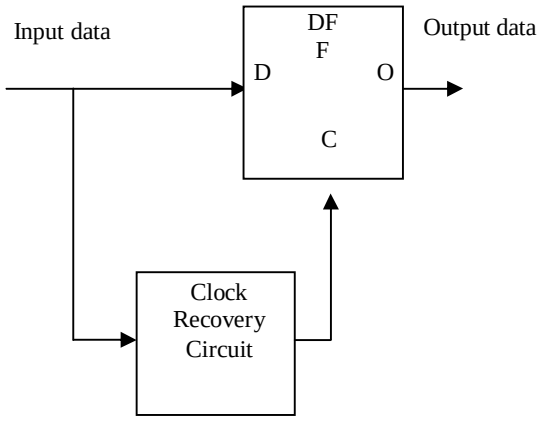


Figure 9. Schematic diagram of decision circuit

VII. CONCLUSION

In this paper, we have designed, implemented and simulated high speed (9.95328Gb/s) data recovery DLL with switched capacitor filter using Microsim EDA software. This design is simulated for four different center frequencies of SC filter by keeping multiplication as 4,8,16 and 32. For the data of 9.95338 Gb/s we have taken f_c of SC filter 2.48832 GHz, 1.24416 GHz, 622.08MHz and 311.04MHz. From the results it is clear that the jitter cut off frequency 311.04MHz has been selected as the center frequency of SC filter for optimum performance of the circuit.

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