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Power Efficient VLSI Inverter Design using Adiabatic Logic and Estimation of Power dissipation using VLSI-EDA Tool

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Abstract--**Power dissipation becoming a limiting factor in VLSI circuits and systems. Due to relatively high complexity of VLSI systems used in various applications, the power dissipation in CMOS inverter, arises from it's switching activity, which is mainly influenced by the supply voltage and effective capacitance.[1,2,3] To optimize power dissipation, the researches show various techniques like appropriate coding, appropriate design architectures, appropriate manipulation algorithms.**

In this paper we have applied adiabatic logic design approach to design COMS inverter. Adiabatic switching techniques based on energy recovery principle are one of the innovative solutions at a circuit and logic level achieve reduction in power [12]

Various adiabatic logic based inverters are shown. Mainly our aim is to design and simulate PFAL inverters. Finally we have calculated dissipated power of static CMOS inverter and compare it with that of PFAL based inverter. [4, 6]

INTRODUCTION:

Demands for low power circuits have motivated VLSI designers to explore new approaches to the design of VLSI circuits. Adiabatic logic means energy recovery logic[3,4,5]. Adiabatic circuits achiever low energy dissipation by restricting current flow across devices with lower voltage drop and by recycling the energy stored on their capacitors. Adiabatic logic also generates low switching noise. In mixed signal analog and digital IC design switching noise is an important problem. In adiabatic circuits switching occurs with the minimum voltage drop across devices and node's voltages changes slowly.

Younis and *Knight* have proposed adiabatic logic families with less dissipation but each gate requires 16 times the number of devices compared to conventional logic.

Koller and *Athnus* have decided a scheme based on transmission gates with limited cascadability. In this paper we have used PFAL adiabatic logic family.

DESIGN:

In this paper our aim is to concentrate in Positive feedback adiabatic logic but the circuits of other adiabatic inverters are also given. The differences in various adiabatic logic families can be clearly understood from the circuit representations.

To recover and to reuse the supplied energy, an AC power supply is used for ECRL inverter. As usual in adiabatic logic Circuit the supply voltage also acts as a clock. Both out and out are generated so that the power clock generator can always drive a constant Load capacitance independent of i/p signal. The differences with respect to ECRL, in PFAL Latch is made by two PMOSFETS and two n MOSFETS and functional blocks are in parallel with transmission PMOS. So equivalent resistance needs to be charged. [4,5] 2N-2N2P logic reduces coupling effect. The primary advantage of 2N-2N2P over ECRL is that the cross coupled n MOSFET snitches result in no floating o/p.

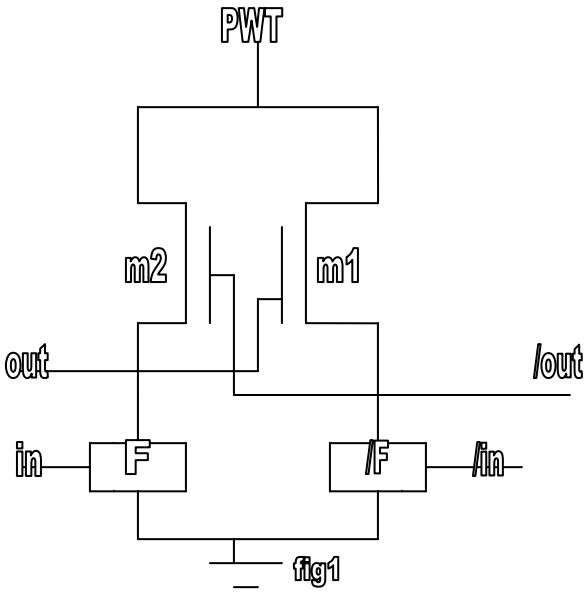


fig1

The circuit of ECRL can be shown in fig 1.

Fig 2. shows adiabatic inverter design using PFAL architecture.

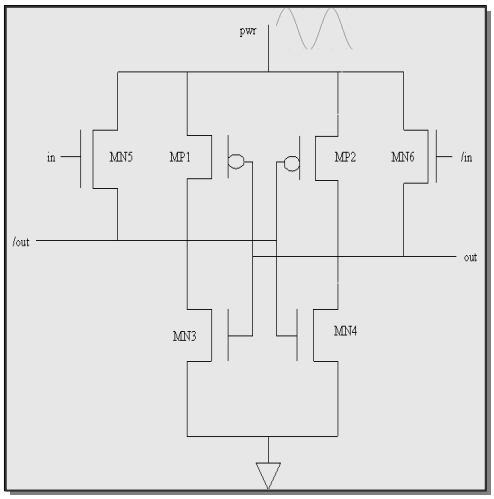


Fig. 2

Positive Feedback Adiabatic Logic (PFAL)shows the lowest energy consumption if compared to other similar families .The main part of all the PFAL gates is an adiabatic amplifier, a latch made by the two

PMOS and two NMOS. The two n-trees realize the logic functions. The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions. [4, 6, 7]

2N-2N 2P is a modification to ECRL logic . Here the coupling effect is reduced.It has cross coupled latch of two PMOSFET and two NMOSFET.

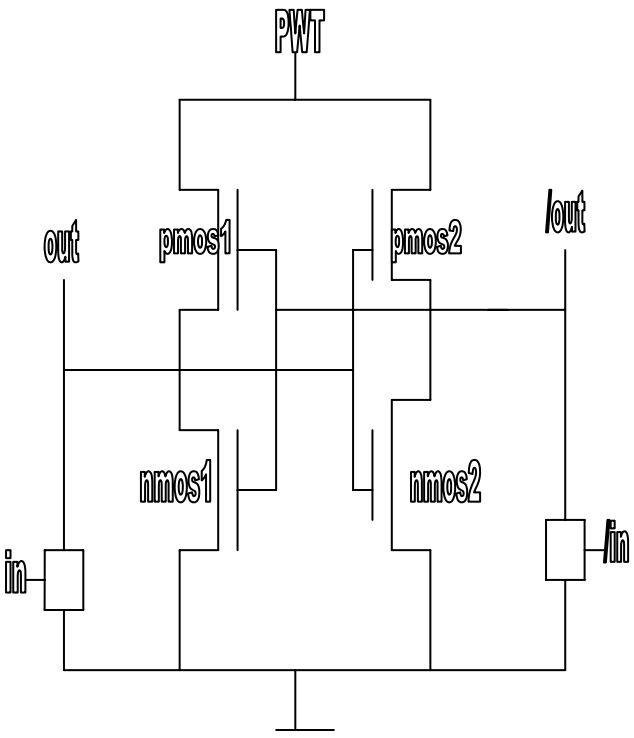


Fig. 3

Fig 3 shows CMOS inverter design using 2N-2N 2P adiabatic logic.

SIMULATION RESULTS:

We have simulated the following PFAL circuit. Standard TSMC 0.35 µm technology is used here. The circuit that is used in simulation is shown in fig 4. The simulation results are shown in fig 5.
Fig 6 shows normal CMOS inverter. It contains one PMOS and one NMOS.
We have also shown the gate level representation of CMOS inverter. In fig 6 the simulation results of CMOS inverter are shown.

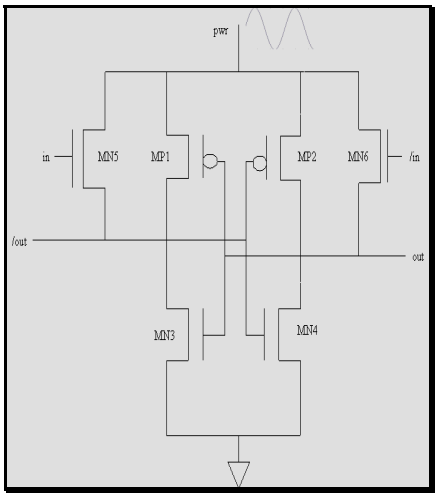


Fig. 4

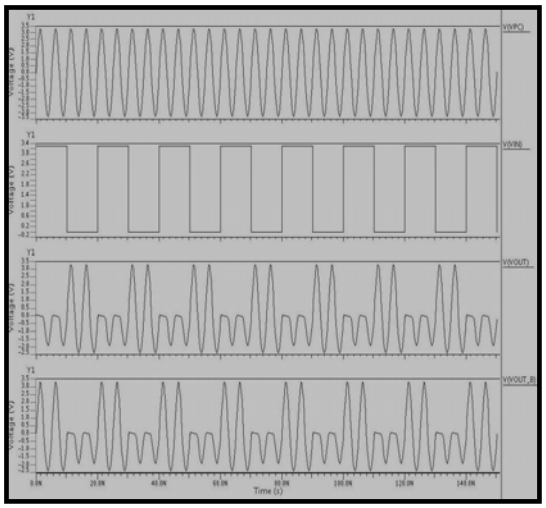


Fig. 5

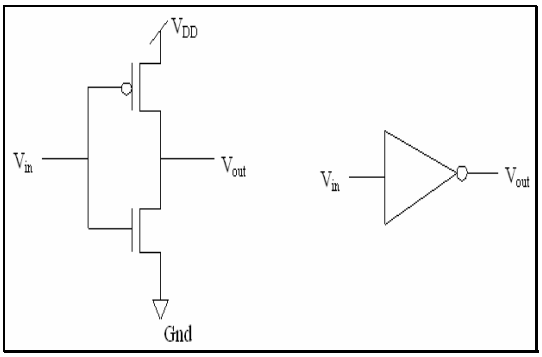


Fig. 6

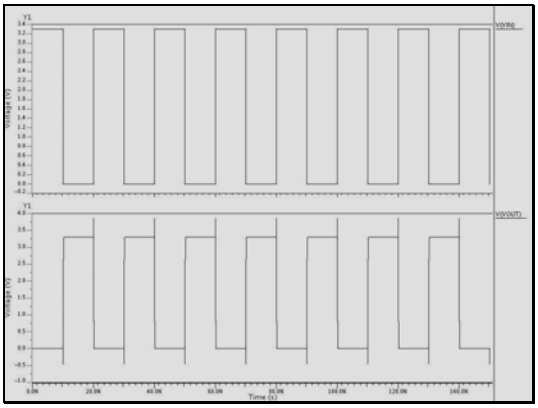


Fig .7

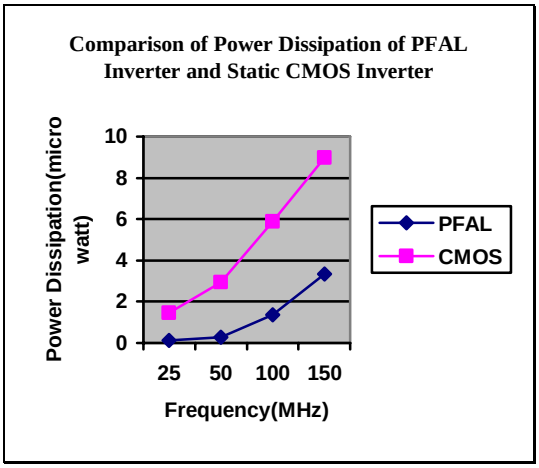
POWER DISSIPATION:

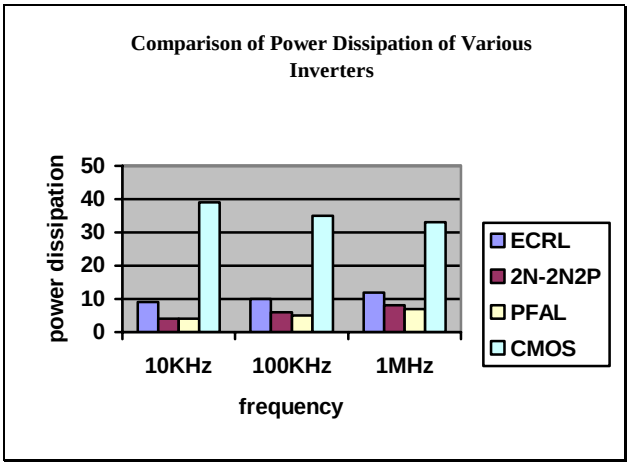
We have calculated the variation of power dissipation with the change in frequency. The power is measured in micro-watt and frequency is measured in MHz.

TABLE 1

Frequency	**PFAL CMOS**	**Static CMOS**
20MHz	0.10µW	1.40µW
50MHz	0.28µW	2.94µW
100MHz	1.37µW	5.88µW
150MHz	3.33µW	8.99µW
200MHz	5.13 µW	10.01 µW

We have taken frequency range of 20 MHz to 200 MHz.
It is clearly seen that PFAL inverters have less power dissipation than that of static CMOS.





In the chart the difference in power dissipation in PFAL inverter and Static CMOS inverter is also clearly reflected.

We have also calculated Power dissipation of other adiabatic inverters like ECRL inverter, 2N-2N2P logic based inverter and compare the results with static CMOS inverter and PFAL based inverter.

TABLE 2

Type of Inverter	Frequency		
	10KHz	100 KHz	1MHz
ECRL	9 µW	10 µW	12 µW
2N-2N2P	4 µW	6 µW	8 µW
PFAL	4 µW	5 µW	7 µW
CMOS	39 µW	35 µW	33 µW

(We have taken approx. values of power dissipations)

We have plotted the result that is power dissipations of ECRL, 2N-2N2P,PFAL and static CMOS inverters.

It is clearly seen that PFAL inverters have lowest power dissipation compare to other inverters.

Here we have taken a frequency range of 10KHz to 1MHz. The result is also suitable for higher frequency ranges.

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