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Abstract: A 1.2-V 40-mA capacitor-free CMOS low-dropout regulator (LDO) for system-on-chip applications to reduce board space and external pins is presented. By utilizing damping-factor control frequency compensation on the advanced LDO structure, the proposed LDO provides high stability, as well as fast line and load transient responses, even in capacitor-free operation. The proposed LDO has been implemented in a tsmc65nm CMOS technology, and the total error of the output voltage due to line and load variations is less. Moreover, the output voltage can recover with ≈2.3μs for full load current changes. The power-supply rejection ratio at 1 MHz is 26 dB.

Keywords: *loop-gain stability, capacitor-free low-dropout regulator (LDO)*

1. INTRODUCTION

INDUSTRY is pushing towards complete system-on-chip (SoC) design solutions that include power management. The study of power management techniques has increased spectacularly within the last few years corresponding to a vast increase in the use of portable, handheld battery operated devices. Power management seeks to improve the device's power efficiency resulting in prolonged battery life and operating time for the device. A power management system contains several subsystems including linear regulators, switching regulators, and control logic. The control logic changes the attributes of each subsystem; turning the outputs on and off as well as changing the output voltage levels, to optimize the power consumption of the device.

Due to the emerging need of high-performance low-voltage LDOs for low-voltage mixed-signal systems, many researchers have recently proposed many advanced methods to improve the performance of LDOs. Rincon-Mora *et al.* proposed current-efficient voltage buffer, forward-biased power transistor, pole-zero doublets for load-regulation enhancement, and capacitance multiplication [2]. Heisley *et al.* proposed using a DMOS power transistor. Chevalerias *et al.* proposed using an nMOS power transistor with charge-pumped gate drive. The main aims of all the proposed methods are: 1) to enable low voltage regulation; 2) to reduce slew-rate limit at the gate drive; and 3) to improve load regulation and transient response. However, the precision of. the above reveals the fact that there are limitations on the structure and frequency compensation scheme of classical

LDOs, especially for the low-voltage LDO designs. Moreover, the off-chip capacitor, which is the key for stability and high LDO performance, cannot be eliminated. This off-chip capacitor is the main obstacle to fully integrating LDOs in system-on-chip designs.

As a result, low-voltage high-stability and fast-transient LDOs with, preferably, capacitor-free operation should be developed. Solving the correlated tradeoffs on stability, precision, and recovery speed is the main challenge of capacitor-free LDO design [4]. In this paper, a CMOS LDO that is targeted for CMOS system-on-chip designs is presented. The circuit architecture is based on a three-stage amplifier design [5], and it provides a capacitor-free feature to eliminate the need of bulky off-chip capacitor. Both fast load transient response and high power-supply rejection ratio (PSRR) are achieved due to the fast and stable loop gain provided by the proposed LDO Structure and damping-factor-control (DFC) compensation Scheme. The power pMOS transistor in the proposed LDO operates in linear region at dropout, and hence, the required transistor size can be reduced significantly for the ease of integration and cost reduction. In addition, a novel CMOS voltage reference based on weighted difference of gate–source voltages enables full-CMOS implementation.

This paper focuses on low-dropout (LDO) voltage regulators. LDO regulators are an essential part of the power management system that provides constant voltage supply rails. They fall into a class of linear voltage regulators with improved power efficiency. Efficiency is improved over conventional linear regulators by replacing the common-drain pass element with a common-source pass element to reduce the minimum required voltage drop across the control device. Smaller voltage headroom in the pass element results in less power dissipation, making LDO regulators more suitable for low-voltage, on-chip, power management solutions.

2. CONVENTIONAL LDO

The conventional LDO voltage regulator, for stability requirements, requires a relatively large output capacitor in the single microfarad range. Large microfarad capacitors cannot be realized in current design technologies, thus each LDO regulator needs an external pin for a board mounted output capacitor. To overcome this issue, a capacitorless LDO has been proposed in that topology is, however, unstable at low currents making it unattractive for real applications(figure.1).

This paper poses to remove the large external capacitor, while guaranteeing stability under all operating conditions. Removing the large off-chip output capacitor also reduces the board real estate and the overall cost of the design and makes it suitable for SoC designs.

Most of the conventional LDO performances are greatly affected when the external capacitor is reduced by several orders of magnitude. The absence of a large external output capacitor presents several design challenges both for ac stability and load transient response. Conventional LDO regulators use a large external capacitor to create the dominant pole and to provide an instantaneous charge source during fast load transients. Thus, a capacitorless LDO requires an internal fast transient path to compensate for the absence of the large external capacitor [6]. To realize the task at hand, the basic capacitorless LDO regulator, is revisited in the following section.

One of the most significant side effects in LDOs is stability degradation due to the several poles embedded in the loop. As shown in Fig. 2(a), the uncompensated capacitorless LDO has two major poles: the error amplifier output pole and the load dependent output pole. Moreover, the power pMOS transistor in classical LDO must operate in saturation region due to the stability problem at different input voltages.

The change in voltage gain due to different drain–source voltage is not substantial when the transistor operates in saturation region. However, if the transistor operates in linear region at dropout, the transistor will operate in saturation region instead as the input voltage increases.

As mentioned previously, when the loop gain increases, the classical LDO based on dominant-pole compensation may be unstable. Therefore, the power pMOS transistor needs to operate in saturation region throughout the entire range of input voltage, so a large transistor size is require to provide a small saturation voltage at the maximum output current.

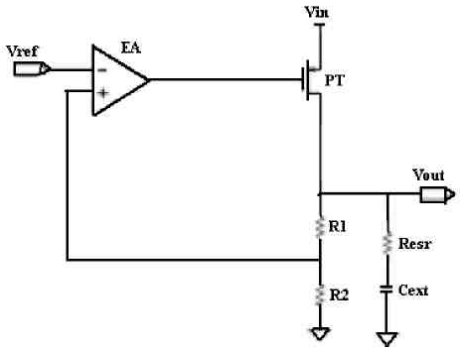

Fig 1 Conventional LDO voltage regulator

The specifications of the LDO can be classified into three classes: 1) static-state specification; 2) dynamic-state specification; and 3) high-frequency specification. Line and load regulations, as well as temperature coefficient, are regarded as static-state specifications, while line and load transient responses, as well as ripple rejection ratio, are dynamic-state specifications. The high-frequency specifications are PSRR and output noise. All specifications are correlated, and they have tradeoffs with the LDO stability when dominant-pole compensation with pole-zero cancellation is used. Line and load regulations are two important specifications that relate to the output-voltage accuracy. PSRR depends highly on both loop-gain bandwidth and ESR. An LDO with a good PSRR and line transient response results in a good ripple rejection ratio.

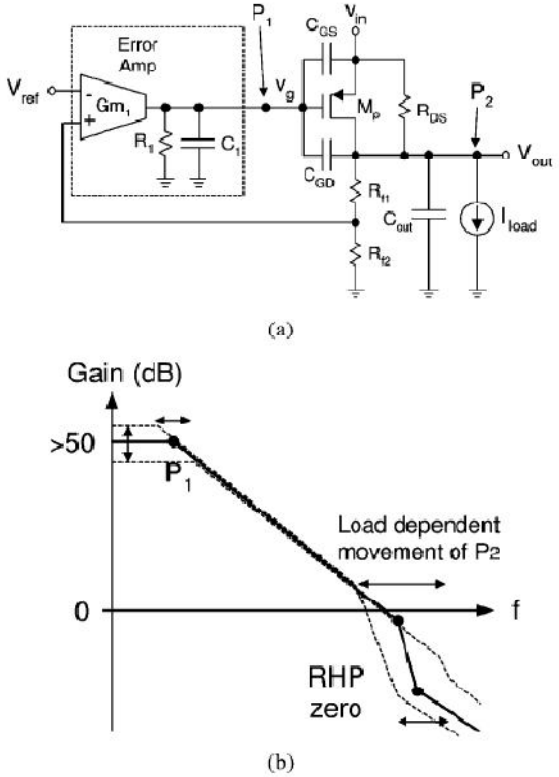

Fig. 2. (a) Equivalent circuit of LDO voltage regulator and (b) pole locations for uncompensated capacitorless LDO voltage regulator; C_{out}t around 100 pF.

From the above discussions on classical LDO using dominant- pole compensation, a high loop gain and a wide loop bandwidth are critical for the improvement of LDO performance, but static power consumption and stability are tradeoffs. It is further illustrated that classical LDOs cannot be applied effectively to system-on-chip designs due to the required large output capacitor for stability. Therefore, an advanced LDO structure with advanced frequency compensation, which solves the tradeoff problems of classical LDOs, is presented in next section.

3. PROPOSED LDO STRUCTURE WITH DFC COMPENSATION

From the previous discussion, the classical LDO suffers from a stability problem. This problem is due to the low-frequency poles, and hence, large off-chip capacitance and ESR are needed for closed-loop stability. In fact, this problem can be solved by pole splitting. However, classical two-stage-amplifier topology is not optimum since the power transistor cannot function as a high-gain stage in dropout condition. The pole-splitting effect is thus not effective and the output precision is also degraded. Instead, an LDO can be viewed as a three-stage amplifier with the power transistor as the last stage. When using this approach, as will be discussed later, the positions of the nondominant poles depend on the transconductance of the power transistor and the output capacitance. The larger transconductance and smaller output capacitance results in higher frequencies of the nondominant poles. Therefore, the worst case stability occurs at zero load-current condition as the transconductance is minimum (about 5–10 mA/V, typically) when only a current equaled to V_{out} / (R_{F1}+R_{F2}) ≈ 1–5μA drains from the power transistor. Advanced frequency compensation techniques are required to generate a more effective pole-splitting effect incorporated with pole-zero cancellation. The pushed nondominant poles can be cancelled more effectively by extra zeros at higher frequencies. The required passive components to generate the zeros can be much smaller, and the coupling noise is, hence, reduced significantly. A stable and fast-response LDO can, therefore, be achieved. In this section, the LDO with DFC frequency compensation based on this DFC idea is discussed. The structure of the proposed LDO with DFC frequency compensation and a first-order high-pass feedback network is shown in Fig. 3. It is composed of a high-gain error amplifier which is 1st stage , a high-gain high-output-swing second stage, a power pMOS transistor operating in linear region at dropout, a feedback resistive network with first-order high-pass characteristic, a CMOS voltage reference, and a DFC block with compensation capacitors C_{m1} and C_{m2} . The utilized circuit structure is a cascade architecture, which is suitable for low-voltage operation.

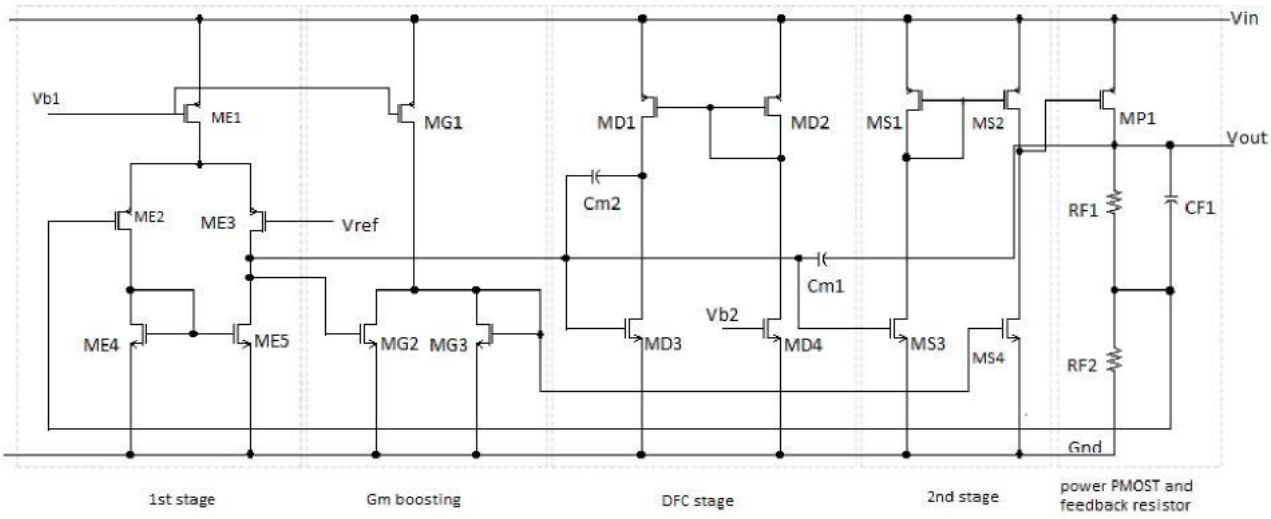

Fig. 3. Structure of the proposed LDO with capacitor-free feature.

The resulting structure can be viewed as a three-stage amplifier driving a large capacitive load, where the capacitive load is due to the power line in capacitor-free condition or due to the off-chip capacitor. This structure can be stabilized using DFC frequency compensation, which is a pole-splitting compensation especially designed for compensating amplifier with From the feedback analysis, it is shown that one pole (p_f) and one zero (z_f) are created, p_f and z_f and are, respectively, given by large-capacitive load. The DFC block is composed of a negative gain stage with a compensation capacitor C_{m2}, and the DFC block is connected at output of the first stage. Another compensation capacitor C_{m1} is required to achieve pole-splitting effect. The feedback-resistive network creates a medium frequency zero for improving the LDO stability

$$P_f = \frac{1}{CF1(RF1||RF2)} \quad (1)$$

$$Z_f = \frac{1}{CF1RF1} \quad (2)$$

The zero frequency is lower than the pole frequency, and this zero, as will be discussed later, can be used to cancel the effect of nondominant poles created in the proposed LDO. In order to have $z_f << p_f$, R_{F1} should be much smaller than R_{F2}. This implies that the required reference voltage should be much smaller than LDO output voltage.

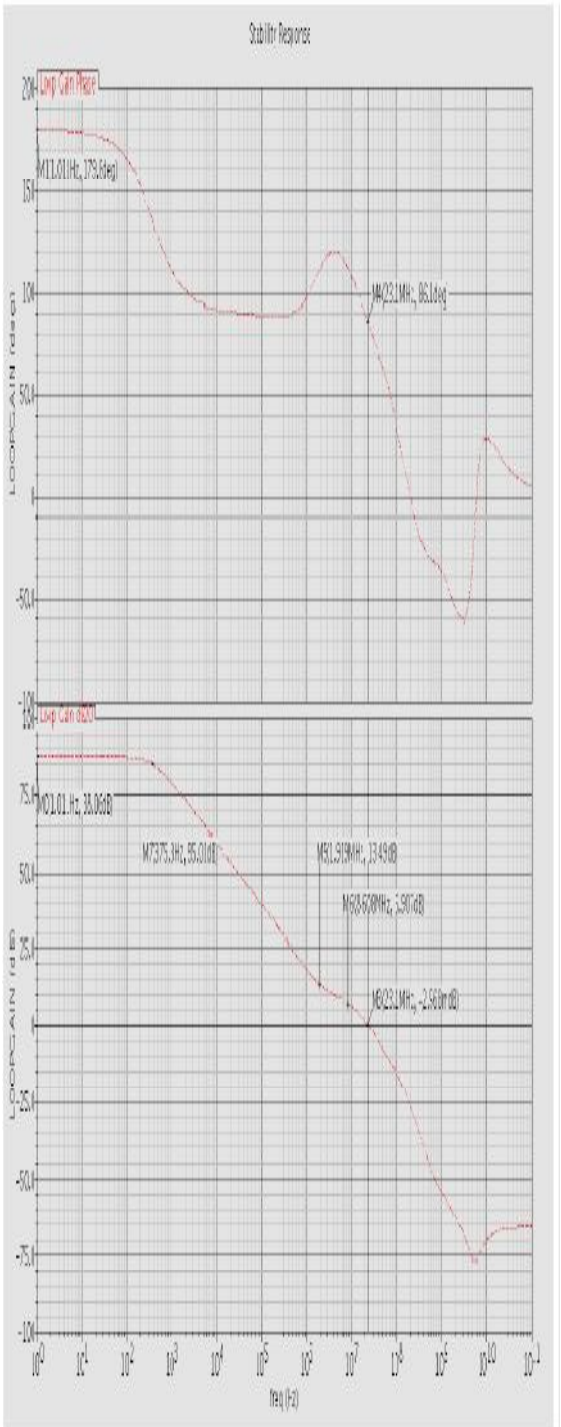

Fig.4. Simulated loop gain of the proposed LDO without an output capacitor

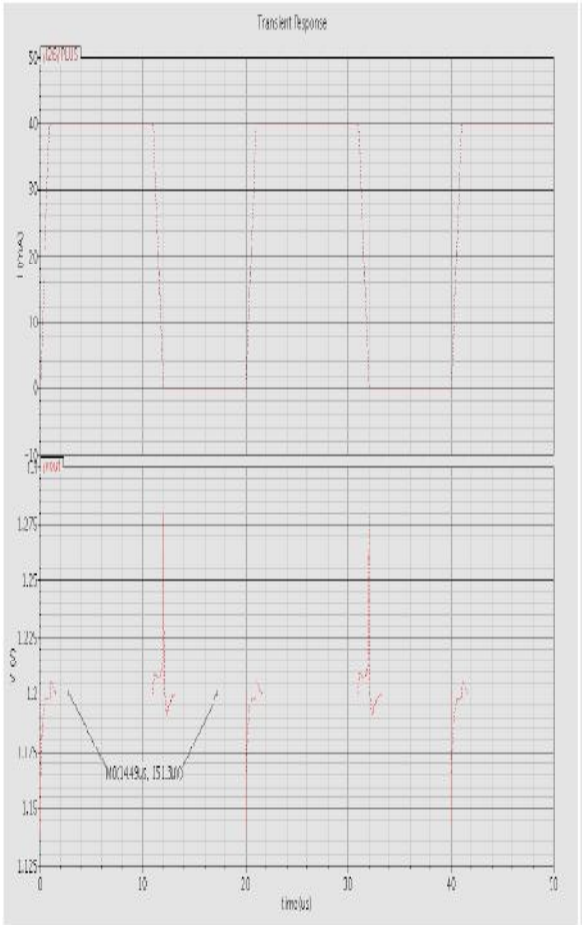

Fig.5. Load transient responses at V_{IN} = 2.5V, Iload of 0.1mA to 40mA with 1µsec of raise and fall time

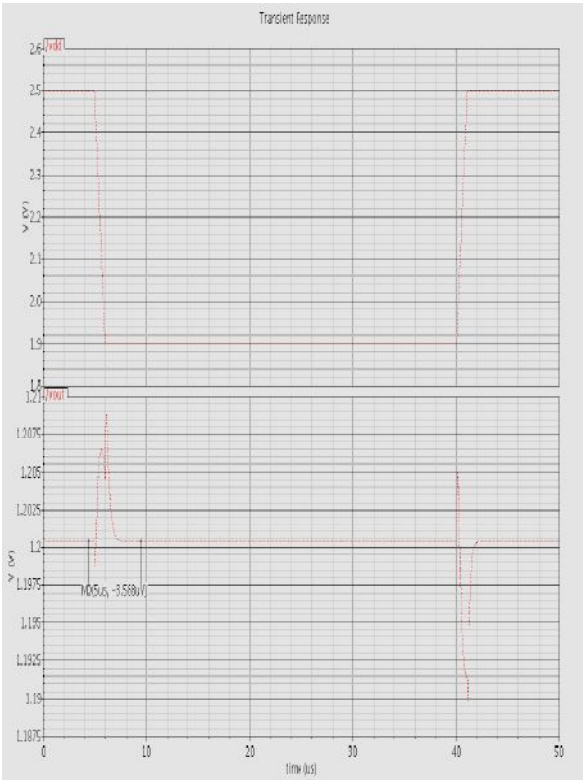

Fig.6. Measured line transient response with V_{IN} = 1.9 to 2.5V

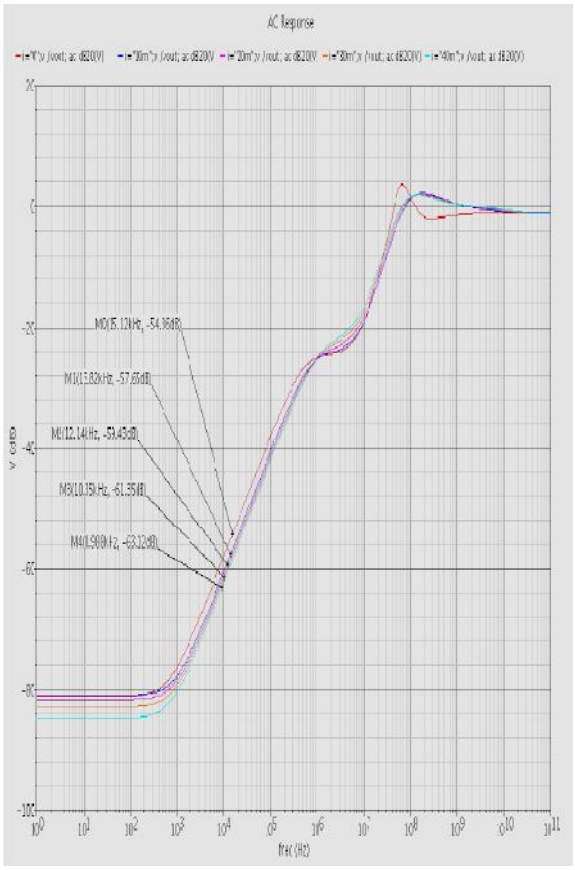

Fig.7. Measured PSRR at V_{IN} = 2.5V, Iload from 0mA to 40mA.

Due to the effective pole-splitting effect by DFC compensation, the nondominant-pole frequencies are high, and so the required C_{F1} is small and is about 5 pF in the current design. This capacitance can be easily integrated in CMOS technologies. In addition, the transient response will not be slowed down by C_{F1} because it is small and is connected at the LDO output.

Due to the advanced LDO structure and compensation scheme, the proposed LDO is stable in the full range of load current when an off-chip capacitor is connected at the LDO output. Better yet, it is also stable without a load capacitor from full load to a finite small output current. For different modes of operation, the proposed LDO has different loop-gain transfer functions, and the details of stability are discussed in the following

When the proposed LDO is used in system-on-chip designs without an off-chip capacitor, the LDO is also stable. There is a minimum load current (about 0.1mA to 40 mA depending on design) such that the LDO is still stable. The output capacitance comes from the power line, and the required minimum load current is larger for a larger load capacitance. Under capacitor, ESR does not exist. Moreover, the second and third poles are pushed to frequencies that are higher than the unity-gain frequency of loop gain due to a large. The transfer function is given by

$$L_{o(capfree)(s)} \approx \frac{Lo(1+\frac{s}{zf})}{(1+\frac{s}{p1})(1+\frac{s}{pf})} \qquad (3)$$

The pole-zero cancellation is automatically achieved by zf and pf, and thus, the phase margin is 900. However, parasitic poles and zeros will degrade the phase margin

The simulated loop gain is shown in Figs. 4. From the results, the proposed LDO is absolutely stable under any operational condition without an off-chip with a minimum load current.

From the above discussion on stability, the proposed LDO structure with the associated compensation scheme is completely different from the classical LDO. In classical LDO, the power loss in the power transistor does not provide any benefit to performance. However, in the proposed scheme, the power used in the power transistor can further improve the LDO stability and the loop-gain bandwidth. This, in turn, enhances the transient responses and PSRR, simultaneously. The power transistor in the proposed LDO is much smaller since it operates in linear region at dropout. The smaller size results in a smaller gate capacitance. This helps to increase the frequencies of the nondominant poles and hence a better stability can be achieved. Moreover, the smaller gate capacitance improves the slew rate at gate drive and a faster transient response can be obtained.

The stability of the proposed LDO is not affected when the supply voltage increases from dropout. When the input voltage increases, the operation region of the power transistor change from linear to saturation region. The voltage gain ($g_{mp}r_{op}$) contributed by the power transistor increases and the whole loop gain increases. Since the first pole of the loop gain is given by P1 = !, the first pole will shift to a lower frequency automatically and the LDO stability can be maintained.

The PSRR is effectively improved due to the wide loop-gain bandwidth. When an off-chip capacitance is used, the required ESR is much smaller than that in classical LDO. This, as mentioned before, also enhances the PSRR at high frequencies.

4. EXPERIMENTAL RESULTS

The proposed LDO shown in Fig. 3 and has been done in tsmc65nm CMOS technology.

The measured load and line regulations are shown in Fig. 5 and 6 respectively. The total error of the output voltage due to load and line variations is just 0.375%and 0.5% respectively.

The proposed LDO provides good performance on PSRR at high frequencies. As shown in Fig. 7, the LDO has at least 26 dB rejection ability at 1 MHz

TABLE I : Summary of the performance of the proposed CMOS LDO

Description	Simulated Values	Units
Vin	1.9 - 2.5	V
Technology	Tsmc65nm	-
Iq	100	µA
Iout_max	40	mA
Vout	1.2	V
Vdrop_out at Iload = 40mA	700	mV
Load regulation	0.00375	mV/mA
Line regulation	0.005	mV/V
PSRR at Iload = 40mA @f = 1kHz	80.36	dB
@f = 10kHz	61.95	dB
@f = 1MHz	24.98	dB
Ron	32.1	Ω
Transient ΔVo for Iload step	90	mV
Settling Time	2.3	µSec

TABLE 2 Comparison of the performance of the proposed work with the reference paper

Description	Reference paper[4]	This paper
Vin	1.5-4.5V	1.9 - 2.5V
Technology	0.6µm CMOS	Tsmc65nm
Iq	38 µA	100 µA
Iout_max	100 mA	40 mA
Vout	1.3 V	1.2 V
Vdrop_out at Iload max	200 mV	700 mV
Load regulation	±0.25%	±0.375%
Line regulation	±0.25%	±0.5%
PSRR at max load current @ f = 1kHz	60 dB	80.36 dB
@f = 10kHz	45 dB	61.95 dB
@f = 1MHz	30 dB	24.98 dB
Settling Time	2µSec	2.3 µSec

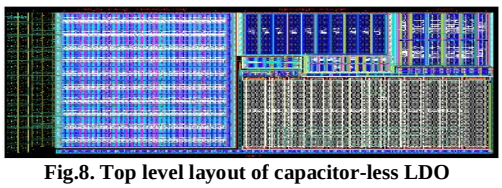

Fig.8. Top level layout of capacitor-less LDO

Figure 8 shows the top-level layout of capacitor-less LDO [8], Which is done in Virtuoso tool from cadence using tsmc65nm.

5. CONCLUSION

A CMOS LDO, which has the capacitor-free feature, based on the DFC frequency compensation, has been presented. The advanced structure and the experimental results have been provided. The performance of the proposed LDO is proven to be much better than the counter parts based on dominant- pole compensation with pole- zero cancellation.The proposed LDO structure is beneficial for system-on-chip designs since it helps to eliminate many off-chip capacitors while preserving high static-state, frequency, and transient performances. The simple structure and small chip area are additional advantages for on-chip local voltage regulators of integrated systems.

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