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# A NEW REDUCED CLOCK POWER FLIP-FLOP FOR FUTURE SOC APPLICATIONS

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**Abstract:** In this paper a novel technique is proposed based on the comparison between Conventional Conditional Data Mapping Flip-flop and Clock Pair Shared D flip flop(CPSFF) here we are checking the working of CDMFF and the conventional D Flip-flop. Due to the immense growth in nanometer technology the SOC is became the future concept of the modern electronics the number of clock transistors are also considerably increased. In this paper we propose a new system which will considerably reduce the number of transistor which will lead to the reduction in clocking power which will improve the overall power consumption. Our proposed which is designed using Pass Transistor Logic (LCPTFF) Low Power Clocked Pass Transistor Flip-Flop system is showing much better output than all other designs as mentioned in the tabulation. The simulations are done using Microwind & DSCH analysis software tools and the result between all those types are listed below.

**Keywords:** Flip-flop, Low Power Clocking System, Sequential Elements, DSCH, Microwind.

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## I. INTRODUCTION

Sequential logic elements perform as many different functions as combinational logic elements; however, they do carry out certain well-defined functions, which have been given names.

We now introduce a new type of circuit that is constructed from devices that remember their previous inputs. The logic circuits in previously were all built with combinational elements whose outputs are functions of their inputs only. Given knowledge of a combinational circuit's inputs and its Boolean function, we can always calculate the state of its outputs. The output of a sequential circuit depends not only on its current inputs, but also on its previous inputs. Even if we know a sequential circuit's Boolean equations, we can't determine its output state without knowing its past history (i.e. its previous internal states). The basic building blocks of sequential circuits are the flip-flop, bistable, and latch just as the basic building block of the combinational circuit is the gate. It's not our intention to deal with sequential circuits at anything other than an introductory level, as their full treatment forms an entire branch of digital engineering. Sequential circuits can't be omitted from introductory texts on computer hardware because they are needed to implement registers, counters, and shifters, all of which are fundamental to the operation of the central processing unit. The conceptual organization of a sequential circuit is explained one by one in the below section. An input is applied to a combinational circuit using AND, OR, and NOT gates to generate an output that is fed to a memory circuit that holds the value of the output. The information held in this memory is called the internal state of the circuit. The sequential circuit uses its previous output together with its current input to generate the next output. This statement contains a very important implicit concept, the idea of a next state. Sequential circuits have a clock input, which triggers the transition from the current state to the next state. The counter is a good example of a sequential machine because

it stores the current count that is updated to become the next count. We ourselves is state machines because our future behavior depends on our past inputs—if you burn yourself getting something out of the oven, you approach the oven with more care next time.

Just as semiconductor manufacturers have provided combinational logic elements in single packages, they have done the same with sequential logic elements. Indeed, there are more special-purpose sequential logic elements than combinational logic elements. Practical flip-flops are more complex than those presented hitherto in this chapter. Real circuits have to cater for real-world problems. We have already said that the output of a flip-flop is a function of its current inputs and its previous output. What happens when a flip-flop is first switched on? The answer is quite simple. The Q output takes on a random state, assuming no input is being applied that will force Q into a 0 or 1 state.

A clocked flip-flop captures a digital value and holds it constant. There are, however, three ways of clocking a flip-flop.

1. Whenever the clock is asserted (i.e. a level-sensitive flip-flop).
2. Whenever the clock is changing state (i.e. an edge-sensitive flip-flop).
3. Capture data on one edge of the clock and transfer it to the output on the following edge (i.e. a master-slave flip-flop).

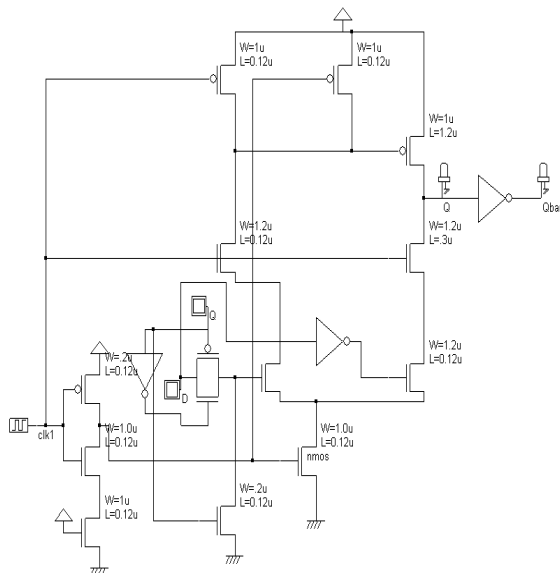
A *level-sensitive* clock triggers a flip-flop whenever the clock is in a particular logical state (some flip-flops are clocked by a logical 1 and some by a logical 0). The clocked RS flip-flop of Fig. 3.11 is level sensitive because the RS flip-flop responds to its R and S inputs whenever the clock input is high. A level-sensitive clock is unsuitable for certain applications. Consider the system of Fig. 3.24 in which the output of a D flip-flop is fed through a logic network and then back to the flip-flop's D input. If we call the output of the flip-flop the *current Q*, then the current Q is fed through the logic

network to generate a *new* input D. When the flip-flops clocked, the value of D is transferred to the output to generate  $Q$ . If the clock is level sensitive, the new  $Q$  can rush through the logic network and change D and hence the output. This chain of events continues in an oscillatory fashion with the *dog chasing its tail*. To avoid such unstable or unpredictable behavior, we need an infinitesimally short clock pulse to capture the output and hold it constant. As such a short pulse can't easily be created; the edge-sensitive clock has been introduced to solve the feedback problem. Level-sensitive clocked D flip-flops are often perfectly satisfactory in applications such as registers connected to data buses, because the duration of the clock is usually small compared to the time for which the data is valid.

**II. CONVENTIONAL CONDITIONAL DATA MAPPING D FLIP-FLOP**

Flip-Flops are the basic elements for storing information and they are the fundamental building blocks for all sequential circuits. Flip-flops have their content change only either at the rising or falling edge of the enable signal. But, after the rising or falling edge of the enable signal, the flip-flop's content remains constant even if the input changes. In a conventional D Flip Flop shown in Figure 2, the clock signal always flows into the D flip-flop irrespective of whether the input changes or not. Part of the clock energy is consumed by the internal clock buffer to control the transmission gates unnecessarily. Hence, if the input of the flip-flop is identical to its output, the switching of the clock can be suppressed to conserve power.

A large part of the on-chip power is consumed by the clock drivers. It is desirable to have less clocked load in the system. CDMFF and CCFF in Section II both have many clocked transistors. For example, CCFF used 14 clocked transistors, and CDMFF used 15 clocked transistors.



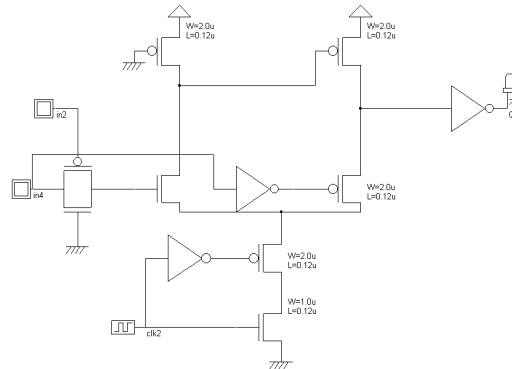
**Figure 1: Conventional Conditional Data Mapping Flip-flop Design**

In contrast, conditional data mapping flip-flop (CDMFF) used only seven clocked transistors, resulting in about 50% reduction in the number of clocked transistors, hence CDMFF used less port than CCFF and CDMFF. (Note

that CDMFF used double edge clocking. For simplicity purposes, we did not include the power savings by double edge triggering on the clock distribution network.) This shows the effectiveness of reducing clocked transistor numbers to achieve low power. Since CDMFF outperforms CCFF and CDMFF in view of power consumption, we do not discuss CCFF or CDMFF further in this paper.

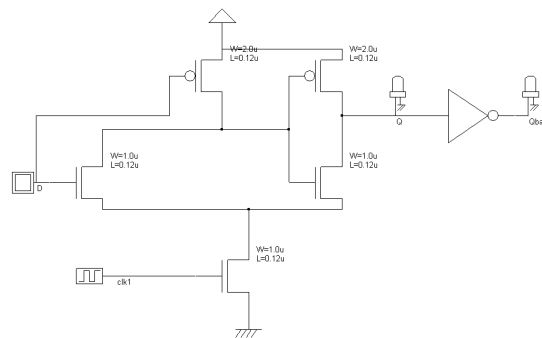
**III. CLOCK PAIR SHARED FLIP-FLOP DESIGN**

CDMFF and CCFF use many clocked transistors. CDMFF reduces the number of clocked transistors but it has redundant clocking as well as Fig. 2. Clocked-pair shared flip-flop, a floating node. To ensure efficient and robust implementation of low power sequential element, we propose Clocked Pair Shared flip-flop (CPSFF, Fig. 2) to use less clocked transistor than CDMFF and to overcome the floating node problem in CDMFF.



**Figure 2: Clock Pair Shared Flip-Flop Design**

**IV. OUR PROPOSED LOW POWER CLOCKED PASS TRANSISTOR FLIP-FLOP DESIGN**



**Figure 3: Our Proposed Low Power Clocked Pass Transistor flip-flop**

By using the Pass Transistor Logic family idea we are designing this circuit as well as by using the pass transistor logic we are using only one clocking transistor so it will be consuming only less power in the clock network of the Flip flop when compared to all other circuits. As well as we are having only 6 Transistors excluding the not gates also. So we will be having much reduced power and area when compared to the other two designs. At the same time due to the reduced no of transistor count we can reduce the delay oriented things also. Thus we are reducing the overall switching delay and power, area consumption. So this circuit will be acting as good sequential elements when compared to other flip-flop design

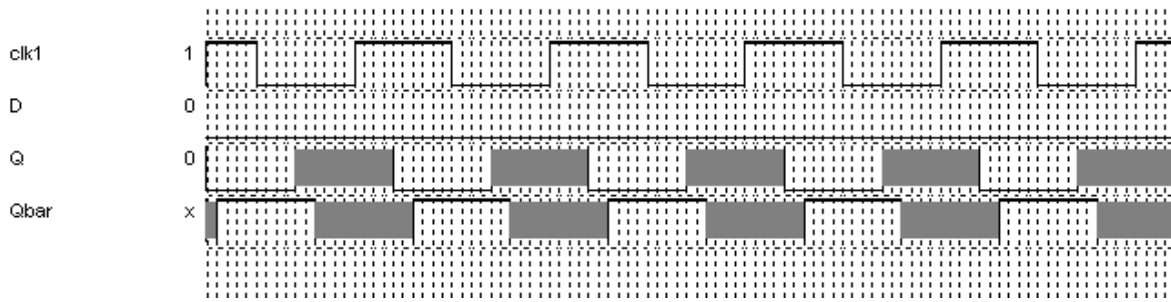


Figure4: Waveform Output of the Proposed Low Power Clocked Pass Transistor flip-flop

The graph represents the input & output characteristics of our proposed system from that we can clearly understand how it works as negative edge triggered flip-flop. There is some nano seconds delay is there even though it's a negligible amount only. Those delays can be further reduced by reducing the sizes of the transistor we are using in this circuit. Or by reducing the nano meter technology also we can reduce the constraints. The Layout design of the proposed new flip-flop is shown in the figure6 the area of that is mentioned at the downside of the layout. The Power consumption characteristics also mentioned below in figure5.

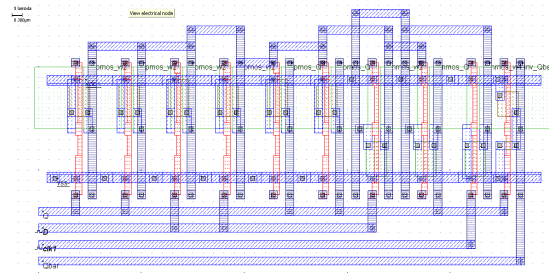


Figure5: Layout of theLCPTFF Proposed Design

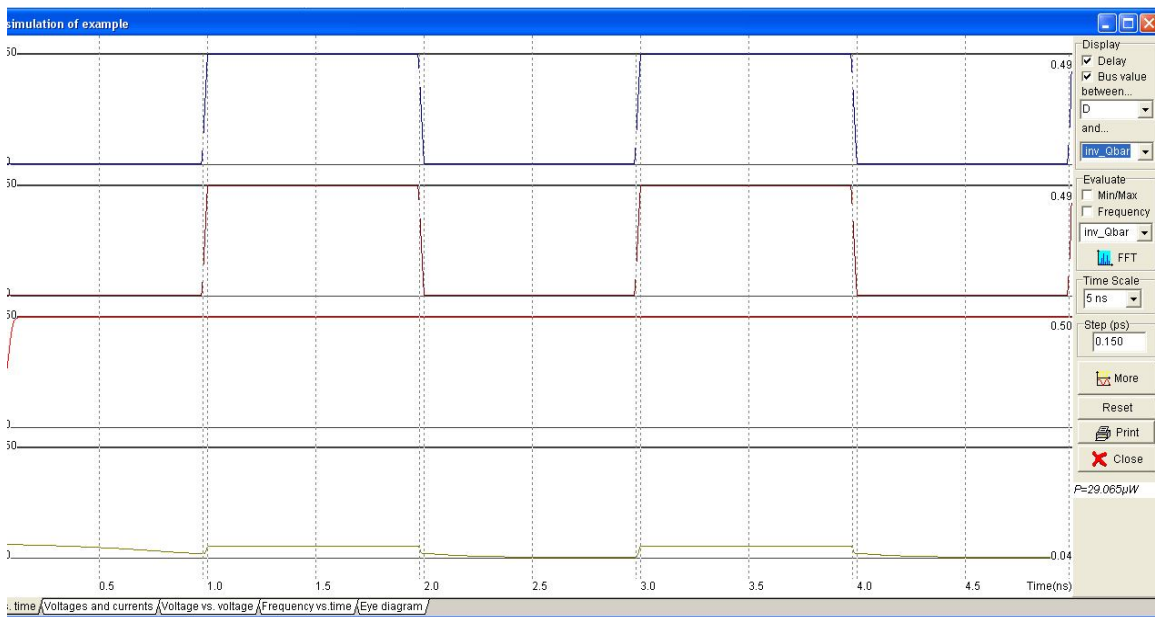


Figure6: Power Characteristic of the LCPTFF Proposed Design

V. TABULATION

Power & Area Comparison Table using CMOS12 um

Type	Power Consumption	Area Consumption
Conventional CDMFF Design	0.454mW	270um <sup>2</sup>
Clock Pair Share Flipflop (CPSFF)	15.232uW	225um <sup>2</sup>
Our Proposed Design (LCPTFF)	9.581uW	84um <sup>2</sup>

Thus the **Our Proposed Low Power Clocked Pass Transistor flip-flop** design shows much less power & Area constraints than the Existing two Flip-Flop designs. As well as the Proposed design will be having very less clock delay when compared to all other circuits. So it can be used in all the future sequential elements for high speed low SOC's manufacturing.

## VI. CONCLUSION:

In this Paper we proposed a new clocking System based D flip flop design which is named as **Low Power Clocked Pass Transistor flip-flop** Design. The Proposed system shows 59.25% Power improvement than the Existing Clock Pair Shared D Flip-Flop and it shows an improvement of 37.5% in area constraints. Thus our proposed system is having very less power and area constraints as well as it is having a very low power clocking system which will lead to improvement in the case implementation in future mobile devices. In future it can be very suitable for System On Chip SOC applications which will lead us to a brighter tomorrow with low power consumption. This can be much suitable for application of battery oriented operation for less power and area. In future we can add some other leakage reduction techniques and the power can be further reduced.

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