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Design and Simulation of Hybrid SET CMOS Based Sequential Circuit

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Abstract - Single Electron Transistor is a hot cake in the present research area of VLSI design and Microelectronics technology. It operates through one-by-one tunnelling of electrons through the channel, utilizing the Coulomb blockade Phenomenon. Due to nanoscale feature size, ultralow power dissipation, and unique Coulomb blockade oscillation characteristics it may replace Field Effect Transistor FET). SET is very much advantageous than CMOS in few points. And in few points CMOS is advantageous than SET. So it has been seen that Combination of SET and CMOS is very much effective in the nanoscale, low power VLSI circuits. This paper has given a idea to make different sequential circuits using the Hybrid SET-CMOS. The MIB model for SET and BSIM4 model for CMOS are used. The operations of the proposed circuits are verified in Tanner environment. The performances of CMOS and Hybrid SET-CMOS based circuits are compared. The hybrid SET-CMOS circuit is found to consume lesser power than the CMOS based circuit. Further it is established that hybrid SET-CMOS based circuit is much faster compared to CMOS based circuit.

Key words - *Single Electron Transistor, CMOS, Hybrid CMOS-SET Circuits, MIB, T-Spice.*

I. INTRODUCTION

For the improvement of the VLSI devices a new strategy was taken, that is the downscaling of the devices. However, there have been reports suggesting that the MOS transistor cannot shrink beyond certain limits said by its operating principle [1]. Over recent years this realization has led to exploration of possible successor technologies with greater scaling potential such as single electron device technology. Single Electron Device (SED) Technology is the most promising future technology to meet the demand for increase in density, performance and decrease in power dissipation in future VLSI circuits. The Single Electron devices have potential to manipulate electrons on the level of elementary charge, are thus considered to be the devices that will allow such a charge. In addition to their low- power nature, the operation of SED is more guaranteed even when device size is reduced to the molecular level. It is also mentionable that the performance of the SED improves as its size reduces more. These properties are quite beneficial for large scale devices. The most important three-terminal SED is single-electron transistor. The schematic structure of SET is shown in Fig. 1. As shown in the figure, the structure of SET is almost same as that of a MOSFET. The SET has one Coulomb blocked island. It has another voltage source and tunnel capacitor. The electrode with the normal capacitor is gate and other two electrodes are drain and source.

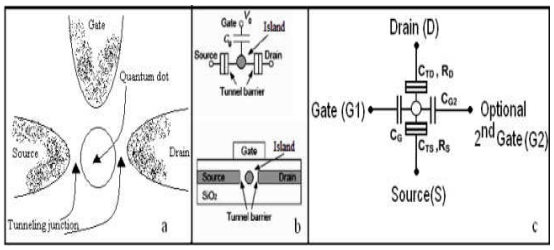

Fig. 1 : Schematic structure of SET and its equivalent circuit

SET has attracted attention as a candidate for future VLSI mainly due to its three virtues: nanoscale feature size, ultralow power dissipation, and unique Coulomb blockade oscillation characteristics. In spite of such interesting properties, the practical implementation of the SET is questionable because of its low current drive and lack of mature room temperature operable technology. A comparison between the advantages and limitations of CMOS and SET technologies is presented in Table 1.

Table1: Comparison between Advantages and Limitations of SET and CMOS Technologies

	SET	*CMOS*
Advantages	**Nanoscale feature size** Unique Coulomb blockade **Oscillation characteristic** Ultralow power dissipation	**High gain and current drive.** High speed. **Very matured fabrication technology.**
Limitations	**Low current drive** Lack of room temperature operable technology **Background charge effect.**	Sub 10 nm physical limits. **Power density.**

From this table it is seen that SET has much more advantages than CMOS. But it has its limitations too. However, Table 1 also suggests that CMOS and SET are rather complementary. SET advocates low power consumption and new functionality (related to the Coulomb blockade oscillations), while CMOS has advantages such as high-speed driving and voltage gain that can compensate for the intrinsic drawbacks of SET. Though a complete replacement of CMOS by SET is not easy, but simultaneously it is also true that the combination of SET and CMOS can bring a new era in VLSI technology. Already these thoughts have drawn the attentions in academia and industry. Toshiba has recently demonstrated the performance of a hybrid MOS-SET inverter (see Figure 1) on a SOI wafer [2, 3]. The unique periodic Coulomb blockade oscillation feature of the SET can be exploited to engender several novel analog functionalities, which are very difficult to realize in a pure CMOS approach. In this paper we have discussed how we can make Sequential circuits using Hybrid SET CMOS and how it is more advantageous than the same circuit built by CMOS only. In this paper we have designed a Master slave J-K flip-flop, and using that we have designed D flip-flop, T flip-flop, 2 bit ring counter. All the circuits are verified by means of T-Spice simulation software. The MIB compact model for SET devices and BSIM4.6.1 model for CMOS are used. This paper is been done according to our concept, you may follow some better one if you want.

II. HYBRID CMOS SET SEQUENTIAL CIRCUIT.

An SET can be made to function as a switch by pushing into the Coulomb blockade state (OFF condition) or allowing it to conduct current (ON condition), it is possible to mimic MOSFET logic architecture in order to develop a hybrid CMOS-SET logic family. It is formed by a PMOS transistor as the load resistance of an SET. It may also be noted that in the gates in these design, PMOS transistor has the SET as its load. Although these resemble CMOS inverter, there are two differences:

(a) The pull transistor is an SET and

(b) V_{DD} is defined by the SET device parameters

Here we have implemented sequential circuits. First we have implemented a master slave J-K flip-flop, and using that we have implemented D flip-flop, T flip-flop and 2 bit ring counter.

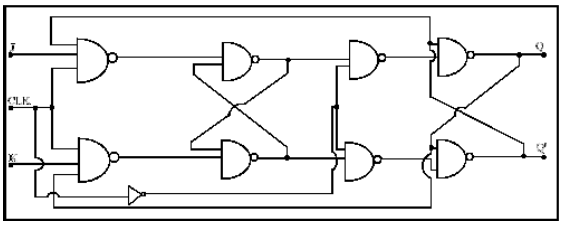

Fig. 4: Master Slave J-K Flip Flop

In Fig.5, there is a JK master slave flip-flop circuit. In this paper every gates are replaced using hybrid CMOS-SET. The total circuit is made of hybrid SET-CMOS NAND gate. In fig. 5 , 3 input NAND and 2 input NAND gates are shown.

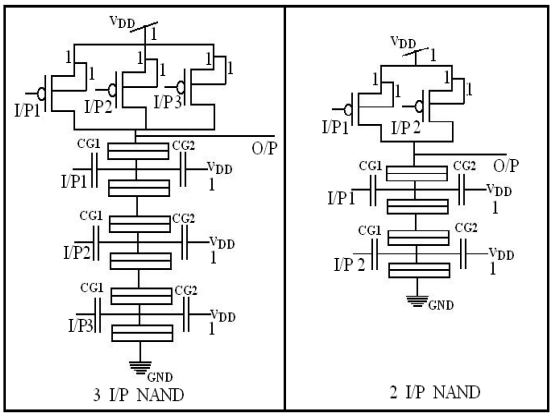

Fig. 5 : 3 Input NAND and 2 input NAND gate

Using these hybrid NAND gates and hybrid NOT gate(fig: 6) we have replaced all the gates of the circuit

The operation of the gates are discussed below:

Operation of a 2 i/p NAND gate

A. When I/P1=0 and I/P2=0

V_{gs} of M1 will be -0.8V (0V-0.8V) and also Vgs of M2 will be -0.8V (0V-0.8V). Since the gate voltages are negative with respect to sources, both M1 and M2 are ON. Since the gate voltages of SET1 and SET2 are equal to 0V, both SETs are OFF.

With SET1 &n SET2 OFF, V_{out} is connected to V_{dd} via M1/M2 and the Output is high.

B. When I/P1=0 and I/P2=1

V_{gs} of M1 will be -0.8V (0V-0.8V) and also V_{gs} of M2 will be 0V (0.8V-V_{dd}). Therefore M1 is ON and M2 is OFF. Since the gate voltage of SET1 is equal to 0V and SET2 is equal to 0.8 V, SET1 is OFF and SET2 is ON.

V_{out} is connected to V_{dd} via M1 and the Output is high.

C. When I/P1=1 and I/P2=0

V_{gs} of M1 will be 0V and Vgs of M2 will be -0.8V. Therefore M1 is OFF and M2 is ON. Since the gate voltage of SET1 is equal to 0.8V and SET2 is equal to 0 V, SET1 is ON and SET2 is OFF.

V_{out} is connected to V_{dd} via M2 and the Output is high.

D. When I/P1=1 and I/P2=1

V_{gs} of M1 will be 0V and Vgs of M2 will be also 0V. Therefore M1 is OFF and M2 is also OFF. Since the gate voltages of SET1 & SET2 are both equal to 0.8V, both SETs are ON. With SET1 and SET2 ON, Vout is connected to ground via SET1 & SET2 and the Output is low.

Thus 3 input NAND gate also operate.

III. RESULTS AND DISCUSSION

The proposed circuits are simulated using the MIB compact model described by Analog Hardware Description Language (AHDL) for SET and BSIM4.6.1 model for MOSFET in Tanner environment. The values of the parameters used for our simulation are given in Table 2.

Table 2. Values of Parameters used for the simulation

Device	***Parameters***	***Voltage Level***
SET	$R_{TD} = R_{TS} = 1M\Omega$, $C_{TD} = C_{TS} = 0.1aF$, $C_{G1} = 0.27aF$, $C_{G2} = 0.125aF$	Logic 0 = 0V Logic 1= 0.8V V_{DD}=0.8V
PMOS	V_{TH} = -220mV, W/L = 100nm/65nm and default values of BSIM4.6.1 model for other parameters	

The logic operations of the circuits were first examined by simulation using T-Spice simulation software. The simulated input-output waveform is depicted in Figures. The logic operation is found to be correct. For Master Slave JK flip-flop the simulation waveform is shown in the figure 6.

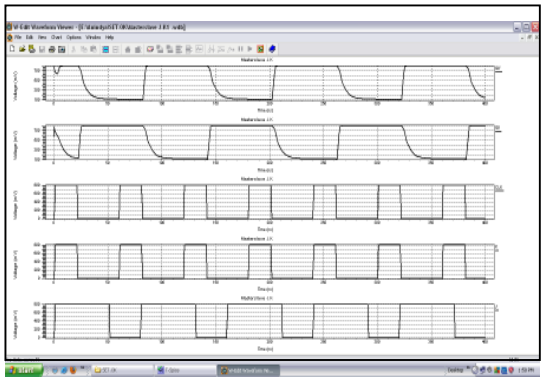

Fig. 6: Master Slave J K F/F

III. POWER AND DELAY CALCULATION

For designing in CMOS technology, a master slave J-K F/F needs 2 nos of 3 input NAND gate & 7 nos of 2 input NAND gate. As per the parameters given above in Table1,the power consumption of CMOS FET is 1000nW & delay is 40ps.The power consumption of each 3 input NAND gate and 2 input NAND gate are 6000nW and 4000nW successively. So, the total power consumption of the circuit is 40000nW. In each 3 input NAND gate 3 nos of MOSFET in the PULLUP circuit are in parallel and 3 nos MOSFET in the PULLDOWN circuit are in series. So, the delay for one 3 input NAND gate is 160ps. Similarly for 2 input NAND gate, 2 nos of MOSFET in the PULLUP circuit are in parallel and 2 nos MOSFET in the PULLDOWN circuit are in series. So, the delay for one2 input NAND gate is 120ps. In the Master slave J K flip flop 2 nos of 3 input NAND gates are in parallel connection, but the other 6 nos 2 input NAND gates are in 3X2 series connection. So, the total delay will be 1 time delay of 3 input NAND gate and 3 times delay of 2 input NAND gate. The total delay for Master Slave J K flip flop will be 520ps.

For designing in Hybrid CMOS-SET technology, each 3 input NAND gate consists of 3 nos of CMOS Transistor in PULLUP network and 3 nos of SET in PULLDOWN network. As per the parameters given

above in Table1,the power consumption of SET is 50nW & delay is 1ps. Power consumption of each 3 input NAND gate is 3150nW.

Power consumption of each 2 input NAND gate is 2150nW. So, the total power consumption of Master slave J K flip flop in Hybrid CMOS-SET technology is 21000nW. Similar to the CMOS design, in each 3 input NAND gate, 3 nos MOSFET in the PULLUP circuit are in parallel connection and 3 nos of SET in the PULLDOWN circuit are in series connection. So, the delay for one 3 input NAND gate is 43ps. Similarly for 2 input NAND gate, 2 nos MOSFET in the PULLUP circuit are in parallel connection and 2 nos SET in the PULLDOWN circuit are in series connection. So, the delay for one2 input NAND gate is 42ps. So the total delay for Master slave J K flip flop in Hybrid CMOS-SET design is 169ps.

From the above calculation, we can show that Power Consumptions & delay are quite less in Hybrid CMOS-SET technology compared to CMOS technology. In the similar way we can calculate the power consumption & delay for other sequential circuits also.

IV. CONCLUSION

The design and simulation of hybrid CMOS-SET sequential circuits are presented here. The output voltage gain is estimated to be about 4.8 as determined from the slope of the transitional region. Since the SET and CMOS are placed in series, the hybridization is found to improve the gain of the inverter while the delay remains the same. Based on the hybrid CMOS-SET inverter, the circuits are designed and implemented. The performances of the proposed circuits are verified by simulation using T-Spice. The simulation results show that the performances of the circuit presented in this paper are satisfactory thereby establishing the feasibility of using the proposed hybrid circuits in future low power ultra-dense VLSI/ULSI circuits.

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REFERENCES

[1] Y.Tau, D.A.Buchanan, W.Chen, D.Frank, K.Ismail, S.Lo, G.Sai-Halasz, R.Viswanathan, H.Wann, S.Wind, and H.Wong, "CMOS Scaling into the Nanometer Regime," Proceeding of the IEEE, vol.85, pp. 486–504, 1997.

[2] Uchida, K., et al., "Programmable Single-Electron Transistor Logic for Low-Power Intelligent Si LSI," *Proc. of. ISSCC* 2002, Vol. 2, pp. 162–453.

[3] Uchida, K., et al., "Programmable Single-Electron Transistor Logic for Future Low-Power Intelligent LSI: Proposal and Room-Temperature Operation," *IEEE Trans. Elec. Dev.*, Vol. 50, No. 7, pp. 1623–1630, 2003.

[4] "Design and Implementation of a Hybrid SET-CMOS based Hi-speed and power efficient Pulse Divider Circuit" Anindya Jana, N Basanta Singh, Anup Sarkar, J.K.Sing and Subir Kumar Sarkar Chennai and Dr.MGR University Second International Conference on Sustainable Energy and Intelligent System (SEISCON 2011), Dr. M.G.R. University, Maduravoyal, Chennai, Tamil Nadu, India. July. 20-22, 2011.

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