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STUDIES ON GE-ON-INSULATOR MOSFETS USING METAL SOURCE/DRAIN CONTACTS FOR ANALOG/ MIXED SIGNAL APPLICATIONS

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Abstract- In this paper, we report the effect of source/drain metal contacts on the electrical behavior of GeOI MOSFETs. The band diagram and current-voltage characteristics of the MOSFET are obtained using SILVACOATLAS, a 2D numerical device simulator, for various metals having a range of work function values. Our investigation reveals that the device using metals having a work function value more than 5 eV exhibits enhanced ON current, transconductance, intrinsic voltage gain, and also reduced subthreshold slope and OFF current.

Keywords- *Analog performance; GeOI MOSFETs; metal source/drain; Schottky barrier*

I. INTRODUCTION

Germanium channel MOSFETs show promise for future high-speed CMOS performance beyond Si capabilities due primary to enhanced carrier mobilities [1-3]. Moreover, because of the advantages inherent to thin-body structures, such as low parasitic capacitance and immunity to short channel effects thin-body Ge-on-insulator (GeOI) MOSFETs can provide further high-speed operation. However, the low dopant solubility in Ge and the fast dopant diffusion during impurity activations [4] make it difficult to realize conventional p-n junction source/drain with low resistance in thin-body structures. The resistance associated with the source/drain (S/D) extensions is one of the pressing challenges to preserve high ON current. One solution to alleviate the problem of resistance associated with the S/D is to replace the ohmic contacts on highly doped junctions by metallic extensions [5-10].

This approach readily takes advantage of the reduced sheet resistance of metal compared to heavily doped junctions and also benefits from atomically sharpened metal/semiconductor junctions. Series resistance can be reduced further using Schottky diodes on highly doped Ge [11-13]. In our study a GeOI device is considered with metal source/drain. Gate to S/D underlap of 5 nm is used to reduce the reverse drain tunneling leakage current density and hence to suppress the ambipolar effect.

In this paper, the impact of different metal S/D Schottky contacts on various electrical parameters of GeOI MOSFETs is intensively investigated. It is found that a higher S/D metal work function increases the I_{ON}-I_{OFF} ratio significantly. An I_{ON}-I_{OFF} ratio of 10^5 can be obtained using S/D contacts with a metal of work function of 5.2 eV whereas the ratio is only 10^3 for work function of 4.52 eV.

II. DEVICE DESCRIPTION

The cross-section of the device considered in our analysis is shown in Fig. 1. The transistor has metal source/drain contacts with HfO_2 as the gate dielectric and a TiN gate. The device comprises a 10 nm thick Ge sitting on 400 nm SiO_2. Different material parameters and geometrical dimensions of our device are entered in Table 1.

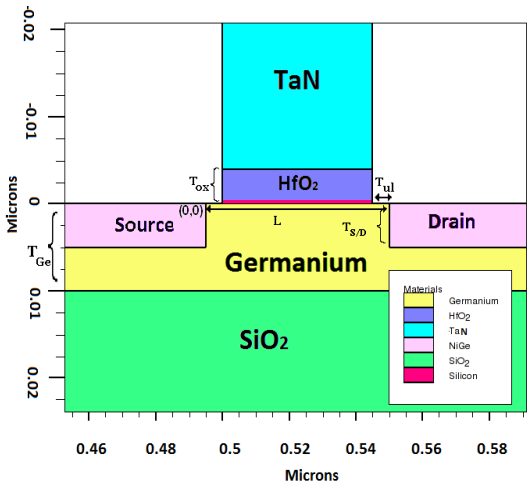

Figure 1: Schematic device structure of a GeOI MOSFET with source/drain Schottky contacts.

TABLE 1: DEVICE PARAMETERS AND THEIR VALUES USED FOR THE SIMULATION WORK

Device parameter	Value
Gate length	45 nm
Gate oxide thickness (HfO_2)	4 nm
Germanium thickness	10 nm
Channel doping (N_D)	2.9×10^{17} cm^{-3}
Gate Overlap (S/D)	5 nm
Gate work function	4.4 eV
Source/Drain work function	4.52o 5.2 eV

III. RESULTS AND DISCUSSION

The 2D numerical device simulator SILVACOATLAS [14] is employed to simulate the metal S/D MOSFET using the high-k gate dielectric and metal gate. In our simulation Universal Schottky Tunneling (UST) model, concentration and field dependent mobility model, Shockley Read Hall and Auger generation recombination models have been taken into account. We have employed our simulation technique to obtain current density versus voltage (J-V) characteristics of Ni–Ge Schottky diodes as described in [12]. Our simulation data as shown in Fig. 2 match quite well with the measured J-V data reported in [12]. In this way we have calibrated our ATLAS simulator and employed this in evaluating performance of MOSFETs with different S/D metal contacts as described below.

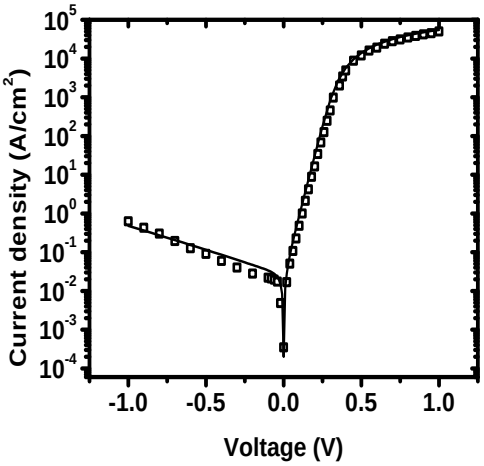

Figure 2: *J–V* characteristics of the Ni/Ge Schottky diodes. Continuous line shows the simulation results whereas the symbols show the experimental data [12].

Fig. 3 shows the valence band edge along the channel length for two different source/drain metal contacts with V_{GS}= -1 V, V_{DS}= -50 mV and V_{DS}= -1 V. The valence band edge energy is displayed for two metal contacts with the work function values 4.52 eV and 5.2 eV. For a lower work function contact material a barrier height of 140 meV is established for holes at the source-channel junction while for a higher work function metal a band offset of 540 meV is set up propelling the hole movement at the source-channel junction. This band diagram helps in-depth understanding of the hole transport within the channel. When the S/D metal work function increases, the device ON current increases while the OFF current decreases as demonstrated in Fig. 4. Since holes move from lower energy to higher energy, the S/D metal contact with a higher work function, for instance 5.2 eV, producing a negative barrier height effectively facilitates the hole movement from the source to drain through the channel for negative gate voltages. At the same

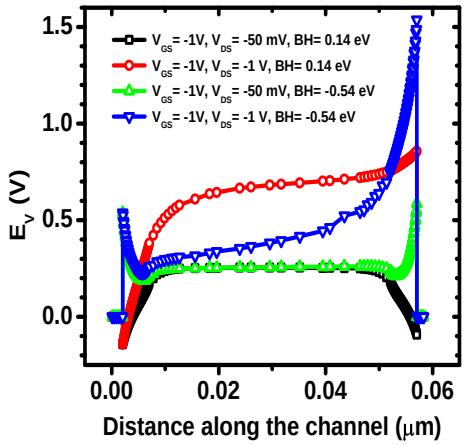

Figure 3: Dependence of valence band edge along the channel length for different drain voltages with two different source/ drain metal contacts.

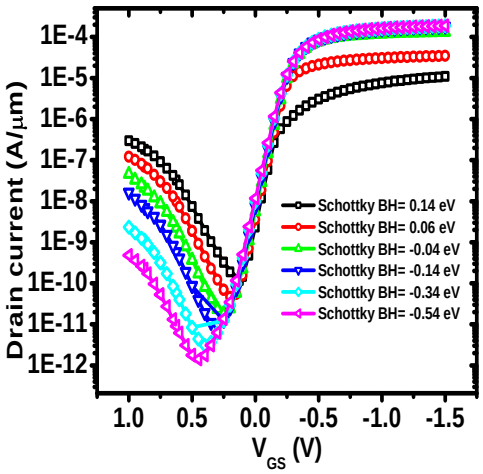

Figure 4: I_D–V_G characteristics of a GeOI based SB-FET for various metals forming source/ drain contacts at V_{DS} =50 mV.

time the electron barrier height becomes 1.2 eV restricting the flow of electrons within the channel for positive gate voltages thereby preventing the device from exhibiting ambipolar behavior as may be seen from Fig. 4. On the other hand, the S/D contact with a lower work function, for example 4.52 eV, opposes both the movement of holes and electrons in the channel for negative and positive gate voltages, respectively thereby degrading the device performance. Hence by employing a metal with a higher work function ~ 5 eV or more for source/ drain contacts it is possible to enhance the ON current and suppress the OFF current. Thus a large I_{ON}/I_{OFF} ratio can be achieved using a metal with a higher work function making S/D contacts. The variation of ON and OFF currents with the barrier height is shown in Fig. 5. It can also be observed that as the work function of the metal forming the S/D contacts increases from 5 to 5.2 eV, the ON current remains almost the same

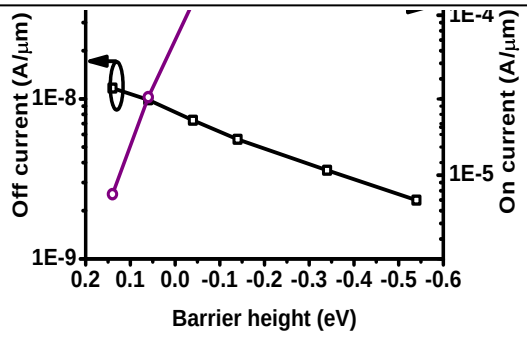

Figure 5: Dependence of ON and OFF currents in a GeOI based SB-FET having channel length of 45 nm.

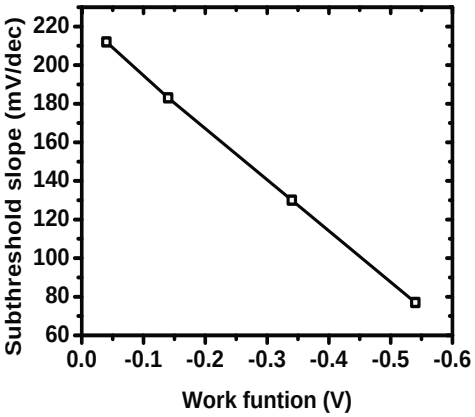

Figure 6: Variation of subthreshold slope with barrier height of a GeOI based SB-FET having channel length of 45 nm.

while the OFF current decreases significantly because of the higher Schottky barrier height encountered by electrons. Fig. 6 demonstrates the dependence of subthreshold slope (SS) with barrier height. Most interestingly, one can easily observe from Fig. 6 that the SS assumes a lower value for devices using metals with a higher work function making S/D contacts. Fig. 7 shows the variation of transconductance with gate to source voltage for different metals. Metals having a higher work function yield a larger value of g_m which may be explained using the transfer characteristic as shown in Fig. 4. Variations of output conductance and transconductance with gate to source voltage for devices with S/D metal contacts are compared in Fig. 8. Devices with Schottky S/D contacts having a barrier height of -0.54 eV exhibit higher transconductance as compared with devices having ohmic S/D contacts. In the strong inversion region of operation devices with Schottky S/D contacts yield a lower value of g_d as compared to devices with ohmic S/D contacts. The extracted value of intrinsic device gain at V_{DS} = -0.5V is plotted in Fig. 9. Higher device gain is obtained for devices with metal source/drain contacts as compared to ohmic contacts particularly in the strong inversion region of operation.

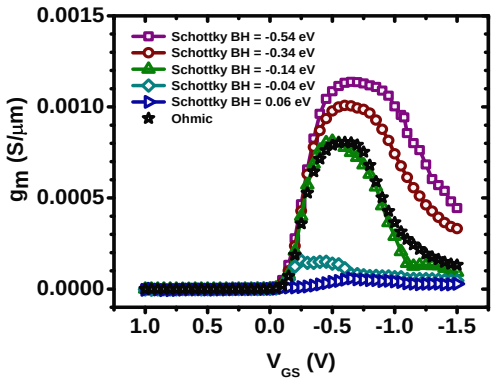

Figure 7: Variation of transconductance with gate voltage of a GeOI based SB-FET at V_{DS} = -0.5V having channel length of 45 nm.

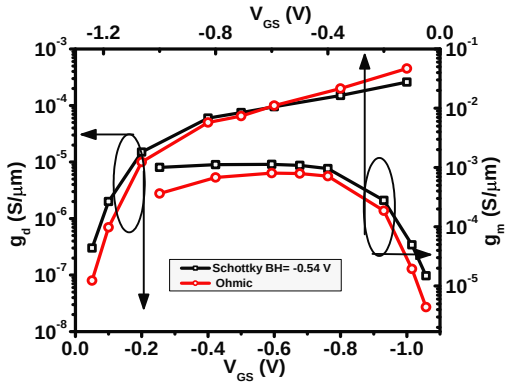

Figure 8: Variation of output conductance and transconductance with gate voltage of a GeOI based SB-FET at V_{DS} = -0.5V having channel length of 45 nm.

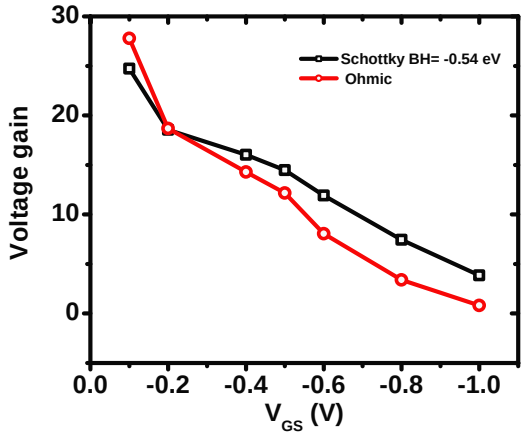

Figure 9: Dependence of intrinsic voltage gain with gate voltage of a GeOI based SB-FET at V_{DS} = -0.5V having channel length of 45 nm.

IV. CONCLUSION

Extensive studies are performed to obtain the effect of metal source/drain contacts on the electrical parameters of GeOI MOSFETs. Devices using a metal with a work function value more than 5 eV forming source/drain contacts exhibit higher values of ON current, transconductance, voltage gain and lower values of subthreshold slope and OFF current.

V. ACKNOWLEDGMENT

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REFERENCES

[1] W. V. D. Daele, C. L. Royer, E. Augendre, J. Mitard, G. Ghibaudo, and S. Cristoloveanu, "Detailed investigation of effective field, hole mobility and scattering mechanisms in GeOI and Ge pMOSFETs," Solid State Electron., vol. 59, no. 1, May 2011, pp. 25–33.

[2] C. Mondal and A. Biswas, "Studies on halo implants in controlling short-channel effects of nanoscale Ge channel pMOSFETs," IEEE Trans on Electron Devices, vol. 59, no. 9, September 2012, pp. 2338-2344.

[3] K. Saraswat, C. O. Chui, K. Donghyun, T. Krishnamohan and A. Pathe, "High mobility materials and novel device structures for high performance nanoscale MOSFETs," in Proc. IEDM. 2006, pp. 659-662.

[4] S. M. Sze, Physics of Semiconductor Devices, Wiley, New York, 1981, p. 68.

[5] D. R. Gajula, D. W. McNeill, B. E. Coss, H. Dong, S. Jandhyala, J. Kim, R. M. Wallace and B. M. Armstrong "Low temperature fabrication and characterization of nickel germanide Schottky source/drain contacts for implant-less germanium p-channel metal-oxide-semiconductor field-effect transistors," Appl. Phys. Lett., vol. 100, 2012, pp. 192101-1-4.

[6] T. Maeda, K. Ikeda, S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, S. Takagi, "Thin-body Ge-on-insulator p-channel MOSFETs with Pt germanide metal source/drain," Thin Solid Films, no. 508, 2006, pp. 346 – 350.

[7] S. Kim, S-J. Choi, M. Jang and Y-K. Choi, "Investigation of the source-side injection characteristic of a dopant segregated Schottky barrier metal-oxide-semiconductor field-effect transistor," Appl. Phys. Lett., Vol. 95, 2009, pp. 063508-1-3.

[8] J. Knoch, M. Zhang, Q. T. Zhao, St. Lenk, S. Mantl, J. Appenzeller, "Effective Schottky barrier lowering in silicon-on-insulator Schottky-barrier metal-oxide-semiconductor field-effect transistors using dopant segregation," Appl. Phys. Lett. Vol. 87, 2005, pp. 263505-1-3.

[9] R. Jhaveri, V. Nagavarapu and J. C. S. Woo, "Asymmetric Schottky tunneling source SOI MOSFET design for mixed-mode applications," IEEE Trans. on Electon Devices, vol. 56, no. 1, January 2009, pp. 93-99.

[10] R. Valentin, Emmanuel Dubois, J-P. Raskin, G. Larrieu, G. Dambrine, T. C. Lim, N. Breil and F. Danneville, "RF Small-Signal Analysis of Schottky-Barrier p-MOSFET," IEEE Trans. on Electon Devices, vol. 55, no. 5, May 2008, pp. 1192-1202.

[11] T. Nishimura, K. Kita and A. Toriumi "A significant shift of schottky barrier heights at strongly pinned metal/Germanium interface by inserting an ultra thin insulating film," Appl. Phys. Exp., vol. 1, 2008, pp. 051406-1-3.

[12] M. K. Husain, X. V. Li, and C. H. de Groot, "High-quality schottky contacts for limiting leakage currents in Ge-based schottky barrier MOSFETs," IEEE Trans. on Electon Devices, vol. 56, no. 3, March 2009, pp. 499-504.

[13] L. Hutin, C. Le Royer, C. Tabone, V. Delaye, F. Nemouchi, F. Aussenac, L. Clavelier, and M. Vinet, "Schottky barrier height extraction in ohmic regime: contacts on fully processed GeOI substrates," Journal of The Electrochemical Society, vol. 156, no. 7, 2009, pp. H522-H527.

[14] ATLAS User's Manual, *A 2D Device Simulator Software Package*, SILVACO Int. CA, (2010).