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AJIT SAMASGIKAR
Instrumentation Technology Department, B.V.B.College of Engineering & Technology Vidyanagar, Hubli, Karnataka, ajit_sam@bvb.edu

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A LOW PHASE NOISE, POWER EFFICIENT VOLTAGE CONTROLLED OSCILLATOR USING 0.18-µM CMOS TECHNOLOGY

AJIT SAMASGIKAR

Instrumentation Technology Department,
B.V.B.College of Engineering & Technology Vidyanagar, Hubli, Karnataka
Email: ajit_sam@bvb.edu

Abstract- A low phase noise, power efficient VCO using UMC 0.18µm CMOS technology has been proposed in this paper. The proposed VCO has a tuning range of 9.71GHz to 9.9GHz, with a phase noise of -79.88 dBc/Hz @ 600kHz offset. The V_{tune} ranging between 1V - 1.5V generates sustained oscillations. The maximum power consumption of the VCO is 11.9mW using a supply voltage of 1.8V with ±10% variation.

Keywords-*PLL, VCO, phase noise, tuning range, active inductor.*

I. INTRODUCTION

The most critical blocks in Phase Locked Loop (PLL) are Voltage Controlled Oscillators (VCOs). They play a vital role in tuning the frequency of the PLL with the incoming frequency. With the demand for low cost and high integration of wireless transceiver building blocks, a low power design is a great concern for RF circuit design. A great deal of research has focused on integrated VCOs using passive inductors, transformers and varactors, which was made possible with the advancement in CMOS technology. While evaluating the performance of VCOs, several parameters such as phase noise, tuning range, frequency, power consumption, area and cost need to be considered. All the simulations are performed using Cadence tool.

VCO is a circuit that outputs a signal of a certain waveform, i.e. triangular, sinusoidal etc. Basic VCO configuration consists of an LC oscillator employing both nMOS and pMOS cross-coupled pairs.

II. THE PROPOSED VCO ARCHITECTURE

The figure shows the basic architecture of VCO. It consists of an LC oscillator employing both NMOS and PMOS cross-coupled pairs. In this, the same bias current flows through both the NMOS and PMOS devices. Consequently for the same power consumption, the configuration yields a large negative resistance. In order to achieve a desirable control over the negative resistance and the oscillation amplitude, a current mirror is generally adopted to limit the supply current. The bias current that flows through current mirror is referred to as tail current and sets the total power dissipation. Implementation and optimization of the on-chip inductors generally dominate the design and turnover time of LC based VCOs.

Varactor MOS are variable capacitors that work in accumulation mode. It is used to tune the frequency of LC tanks implemented in VCO. It is not unusual to channel

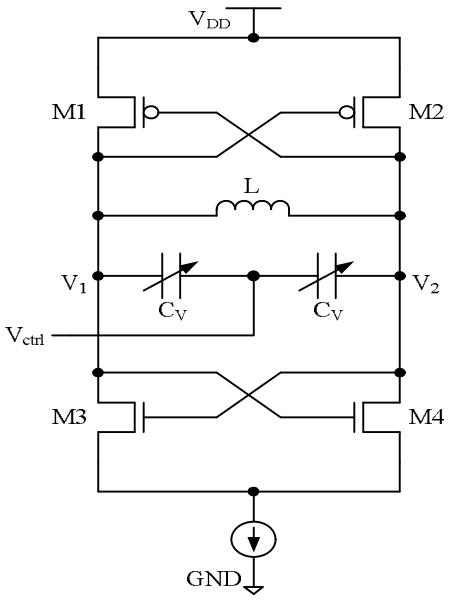

Fig.1. CMOS VCO Architecture

significant efforts into the reduction of parasitic resistances and capacitances associated with the monolithic inductor. Their heavy influence on the inductor's quality factor, as well as the quality factor of the LC tank speaks volumes in terms of performance degradation. However, it's seen that the capacitance constituting the LC tank bears a finite Q-value. In addition, a part of this capacitance is voltage controlled, or in other words implemented as a varactor. The series resistance of a varactor has an overbearing influence on the overall quality factor of the tank circuit. On-chip integrated inductors are

preferred due to ease of packaging. An on-chip inductor's performance is largely influenced by design parameters such as shape, width, thickness, diameter and equally by the material's properties used in implementation.

III. MATHEMATICAL ANALYSIS OF CMOS VCO DESIGN

A 9.82GHz voltage controlled oscillator designed in 0.18u CMOS process is presented. The simulation results have shown that the circuit has a tuning range from 9.71GHz – 9.9GHz, output swing of 1.5V while consuming 11.9 mW of power. The cross-coupled transistor topology depicted in Fig.1 is used as the design topology for several reasons. Full exploitation of differential operation mitigates undesirable common-mode effects such as extrinsic substrate and supply noise. The oscillation amplitude of this structure is a factor of two larger than that of the NMOS-only structure due to the PMOS pair, which results in a better phase noise performance for a given tail current. The rise and fall time symmetry is incorporated to further reduce the 1/f noise up-conversion. The cross-coupled MOS pair acts like a negative resistance as shown in Fig.2. The negative resistance cancels the parasitic resistance of the LC element and the circuit oscillates at frequency given by

$$\omega = 1/\sqrt{LC}$$

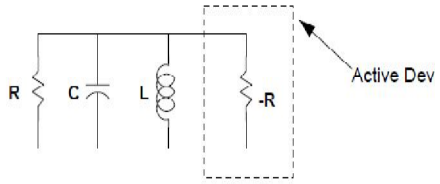

Fig 2.Model of an Oscillator

The equivalent model of an oscillator (with all the parasitic elements) is shown in Fig .3. C_{nmos} and C_{pmos} are the total parasitic capacitances of the NMOS and PMOS transistors, respectively, and g_m and g_o are the small-signal transconductance and output conductance of the transistors, respectively.

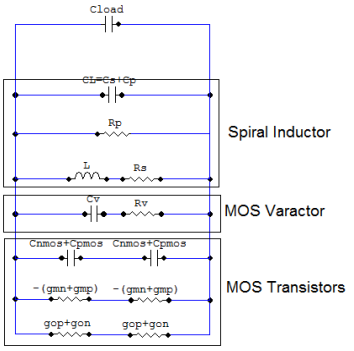

Fig. 3. Equivalent Model of Oscillator

The circuit elements in Fig.3 are defined as follows:

$$C_{nmos} = C_{gs,n} + 4C_{gd,n}$$

$$C_{pmos} = C_{gs,p} + C_{db,p} + 4C_{gd,p}$$

IV. DESIGN STEPS

1. The design process can be summed up in following steps
2. Set $g_{mn} = g_{mp}$ to improve the $1/f_3$ corner of phase noise. This equality gives the equation $Wp = 4.77*Wn$.
3. The tail current is set depending on the power consumption limit.
4. The conductance is calculated keeping in mind the voltage swing specification. $V_{swing} \le I_{\text{tank}} \cdot R_{\text{tank}}$ The value of R_{tank} is used to calculate the value of inductor used in the oscillator.
5. To ensure start-up the gm of cross-coupled devices are set 4 times more than C_{tank} . $\frac{g_m}{G_m} \ge 4$
6. The minimum and maximum capacitance value needed for the required tuning range of frequency is calculated as

$$\omega_{\min} = \frac{1}{L_{\text{tank}} \cdot C_{\text{tank}},\max}$$

$$\omega_{\max} = \frac{1}{L_{\text{tank}} \cdot C_{\text{tank}},\min}$$

The design consists of an inductor and a pair of MOS varactors which are responsible for generating the oscillations. A single inductor is used in order to minimize the area of the chip and also its bulkiness. Implementation and optimization of on-chip inductors generally dominates the design. The heavy influence on the inductor's quality factor, as well as the quality factor of the LC tank degrades the overall performance. This can be recovered by the finite Q-value of the capacitor. Part of this capacitance is voltage controlled that is a varactor. The MOS capacitor has a structure that is analogous to a parallel plate capacitor, with the drain, source and bulk (D, S, B) of a PMOS transistor connected together realizing one plate of the capacitor, while the polysilicon gate constituting the other.

A current mirror is generally adopted to limit the supply current. The bias current that flows through current mirror is referred to as the tail current and sets the total power dissipation. The substrates of the pair of varactors used in the VCO design are shorted. A control voltage called as Vtune is applied to the substrate of the varactor. This decides the tuning range of VCO. The Vtune ranging between 1V - 1.5V generates sustained oscillations. The design is implemented with the supply voltage of 1.8V with a

tolerance of +/-10%. The supply voltage determines the type of technology applied in VLSI Design.

V. SIMULATION RESULTS

The VCO architecture as shown in fig.1 is implemented using 0.18um UMC Technology. The schematic diagram is as shown in fig.4. The physical layout of VCO with on-chip inductor is as shown in fig.5. The sustained oscillations obtained are shown in fig.5. The frequency of oscillation obtained is 9.82GHz for a V_{cntl} of 1.5 V. The minimum phase noise was -79.88 dBc/hz at a 600kHz offset from 9.82GHz. This phase noise performance was maintained throughout the entire frequency range values between -79.88 to -82.4 dBc/Hz.

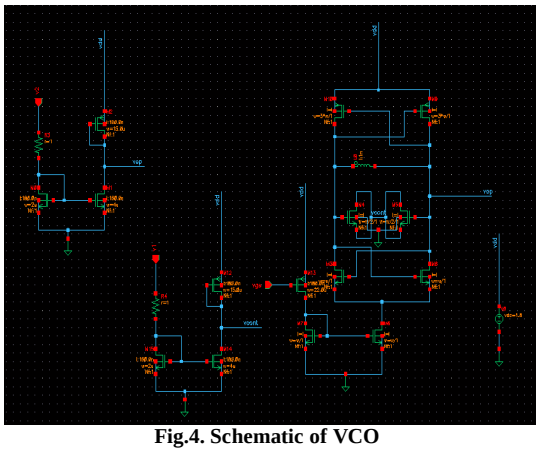

Fig.4. Schematic of VCO

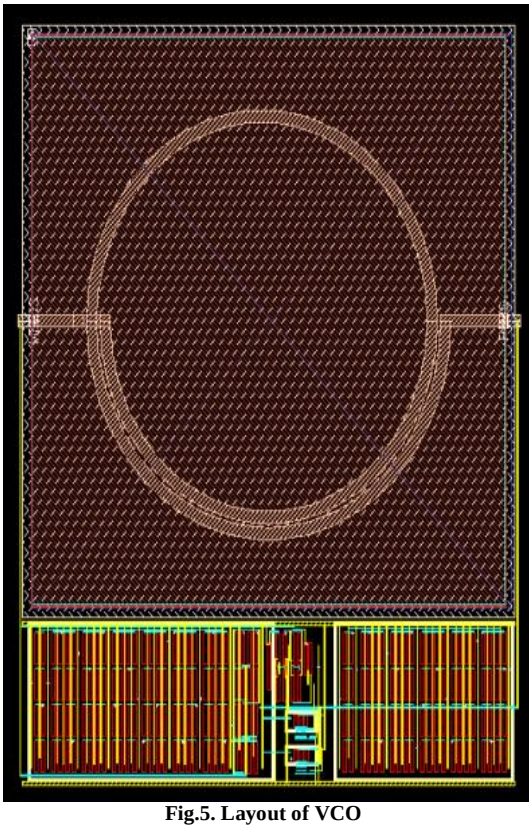

Fig.5. Layout of VCO

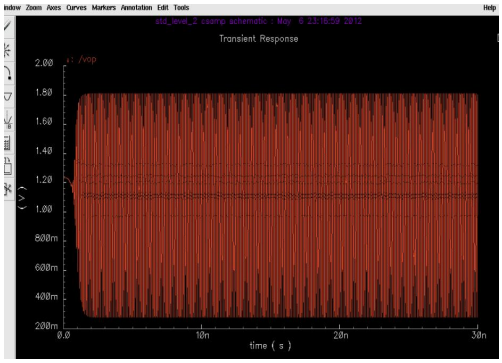

Fig.6. Sustained Oscillations

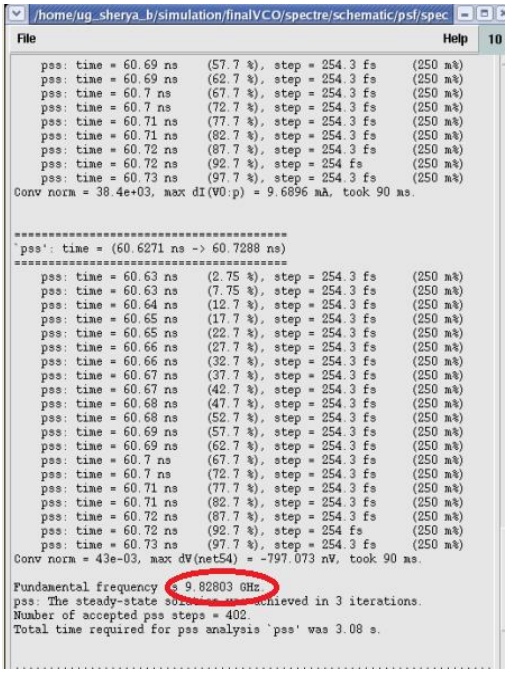

Fig.7. Simulation Result

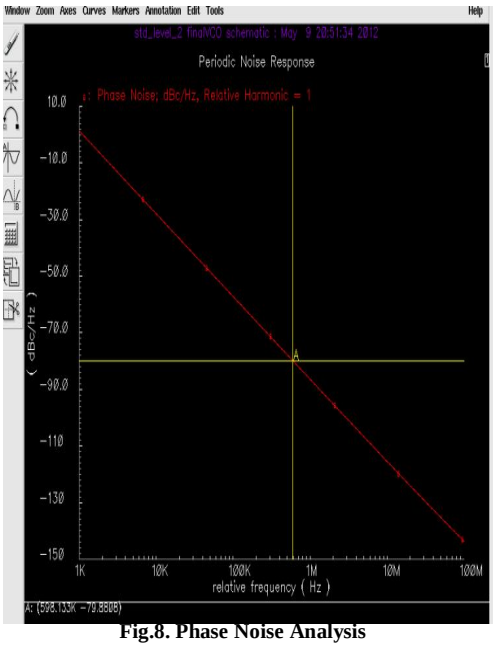

Fig.8. Phase Noise Analysis

SUMMARY OF VCO MEASUREMENTS

Technology	0.18um UMC
Supply Voltage	1.8V
Tuning Range	9.71 Hz to 9.9 GHz
Phase noise @600kHz	-79.88 dBc/Hz
Power Dissipation	9.11mW

TABLE II
COMPARISON OF VCO'S PERFORMANCE

Ref.	Technology	Freq. (GHz)	V_{DD} (V)	P_{DC} (mW)	Phase Noise (dBc/Hz)
This work	0.18um	9.82	1.8V	9.11	-79.88 @ 600kHz
[1]	0.18um	19.9	1.8	32	-111 @ 1MHz
[2]	0.25um	2.73	2.5	10	-102.5@100kHz
[3]	0.18um	2.56	0.5	600uA	-120 @1MHz
[5]	0.18um	20.7	1.8	10.8	-108.67@1MHz

VI. CONCLUSIONS

The proposed VCO has been implemented using 0.18um UMC technology and it achieves a phase noise of -79.88dBc/Hz @ 600 kHz offset. The low power is achieved by carefully designing the varactors and MOS transistors. The circuit design and layout has been done using Cadence Tools. The power dissipation of the circuit is 9.11mW. The proposed VCO has a wide tuning range from 9.71GHz to 9.9GHz.

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