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A 0.1-2 GHZ LOW POWER FOLDED RF FRONT-END WITH MERGED LNA AND MIXER FOR SOFTWARE-DEFINED RADIO APPLICATIONS

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Abstract - In this paper, A Software-Defined Radio (SDR) RF front-end is presented that contains merged LNA and mixers, VGAs, and frequency synthesizer, supporting various wireless communication standards in 0.1-2 GHz while guaranteeing a power/performance trade-off at any time. The proposed low power RF front-end uses the folded and current reuse techniques. for 0.18 um RF CMOS technology with 1.8V supply voltage. In the receive path the proposed design achieves a Noise Figure of 3.8 dB at 160 MHz and 5.5 dB at 2GHz. The Output-referred 3rd-order Intercept Point (OIP3) is high up to 21.3 dBm at 800 MHz. The voltage gain of the front- end is between 16-44 dB. The phase mismatch of LO quadrature signals is lower than 3deg.It consumes 13.8 mW at the 1.7V supply.

Key Words*: *SDR; LNA; Mixer; VGA

I. INTRODUCTION

The demand for the integration of multiple standards into a single portable terminal is growing together with the proliferation of wireless communication standards [1]-[3]. Such handsets could be implemented with multiple dedicated front-ends integrated in parallel. However, that solution is everything but optimal for cost. A Software-Defined Radio (SDR) optimizes the functionality versus area trade-off, by programming a versatile front-end to the desired standard. The boundary conditions being that for each supported standard both performance and power consumption should be comparable to dedicated solutions. The SDR front-end should be compatible with various wireless communication standards, including DRM, DAB, DVB-H, GSM and GPS.

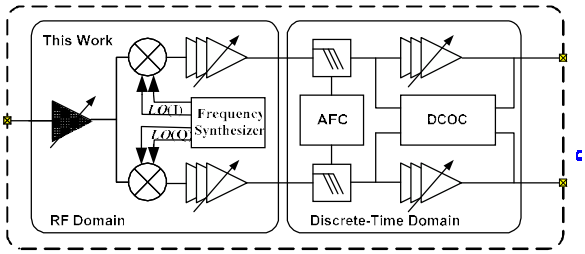

Figure 1. Simplified SDR block diagram

The system architecture is presented in Fig.1. The direct- conversion architecture is the best candidate to realize such SDR as it has the highest potential to reduce the cost, size and power. The receiver usually contains two major parts of the RF-Domain and the Discrete-Time Domain. In RF Domain, a single wideband LNA is used instead of the multi-LNA solutions. Single-ended input LNAs are preferred to save I/O pins and because antennas and RF filters usually produce single-ended signals. Compared to traditionally wireless communication applications the linearity of the proposed I/Q mixer should be high enough to prevent the receiver from being blocked by the large signals in adjacent bands. The VGAs is added to provide a moderate signal power level to the Discrete-Time Domain. In order to provide LO quadrature signals, a wideband frequency synthesizer consists of a single loop PLL and wideband high speed frequency dividers. The detail analysis and circuits design are present in section II.

II. CIRCUITS DESIGN

Referring to Fig.1, the RF front-end consists of four parts: single-ended input and differential output LNA, I/Q mixer, two VGAs and wideband frequency synthesizer. The LNA must have the lowest possible Noise Figure and high enough gain to suppress the noise contribution of the second stage. The mixer and the VGAs are designed aiming for high linearity. The VGAs should have the linear-in-dB property. Meanwhile, the frequency synthesizer should have the wide band, low phase noise and better orthogonality.

A. Low Noise Amplifier

Fig.2 shows the schematic of the proposed LNA for SDR applications. It consists of three stages. The first stage is Low Noise Stage (LNS). The LNS is a low noise amplifier exploiting a noise-canceling technology [4]. The Noise Figure is calculated as follows:

$$NF = 1 + \frac{R_s}{R_f} + \left(\frac{R_s}{R_f}\right)^2 + \frac{\gamma}{4}\cdot\frac{R_s}{R_f}\left(\frac{2R_s}{R_f}+1\right) + \frac{KR_s^3}{8kTR_f^2\cdot f} \quad (1)$$

In Eq. (1), the parameter R_S and R_f are used to quantify the source load impedance and the feedback resistance. parameter γ is noise parameter of transistors. For a deep- submicron MOSFET, the value of γ is usually between 1 and 3. K is an experiential parameter.

The second stage is a Single to Differential Converter (SDC). The compensatory capacitor C_1 is parallel to the resistor R_1 to make the mismatch of the amplitude and the phase of the output differential signal lower than 0.3 dB and 4 degrees.

The third stage is a Differential Multiple Gate Transistor (DMGTR) [5]. The M_{11} and M_{12} are Fully Differential Amplifiers (FDA), the M_{13} and M_{14} are Pseudo-Differential Amplifiers (PDA). The FDA usually suffers from low "g_m" linearity problems due to the negative "g_m". Fortunately, when bias the PDA from saturation to near threshold regime, the "g_m" of the PDA can be moved from negative to positive. From the above consideration, the negative value of "g_m" which degrades linearity of FDA can be compensated by positive value of g_m in the PDA by adjusting the bias and transistor size of PDA. This method does not require extra power consumption, but the OIP3 can be improved above 10 dB.

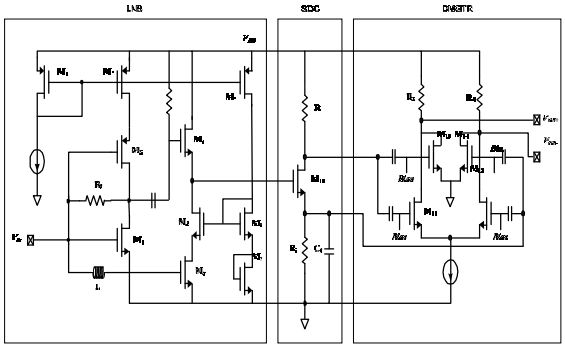

Figure 2. Schemetic of the LNA

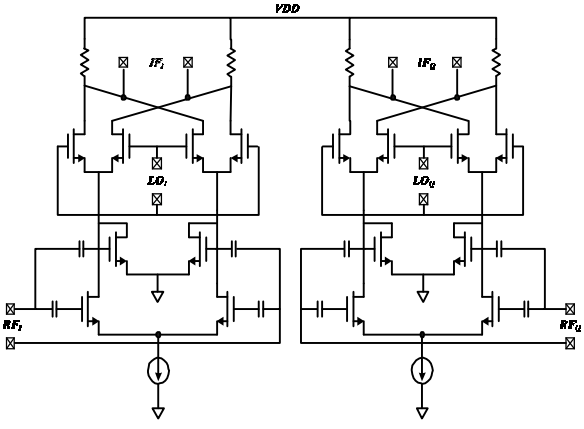

Figure 3. Schemetic of the mixer

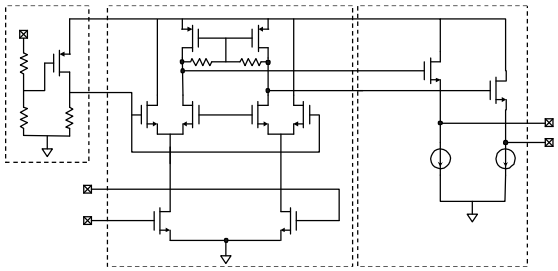

Figure 4. Schemetic of the VGA

B. Mixer

Fig.3 shows the schematic of the mixer. The mixer consists of two modified double balanced Gilbert cell. Compared to the traditional double balanced Gilbert cell, the input transconductance stage of proposed mixer uses the DMGTR topology. It can achieve high linearity but consume the same power than the FDA topology.

C. Variable Gain Amplifer

Signal-summing topology has been widely used in low- power and high-frequency VGA design. Fig. 4 shows the circuit schematic of the proposed signal-summing variable- gain stage with exponential gain control. Compared with the previous work in [6], the proposed variable-gain stage used PMOS transistors M_7 and M_8 as a load instead of a resistor resistors R_1 and R_2 are used as a common-mode feedback circuit, the tail current source is eliminated to enhance the linearity of VGA in low voltage supply process. With the same linear-in-dB gain characteristics on the control voltage, the output voltage swing is larger than the design in [6], especially at the low-gain mode when the input signal is a large signal. The reason is that the DC equivalent resistance of PMOS load in proposed VGA is large than the resistor in [6], while the AC small-signal equivalent resistance maintains the same. The DC voltage at the drain of the PMOS M_7 and M_8 is around 1.3V in low-gain mode, while the DC voltage of resistor load in [6] is 1.7V. So, the total harmonic distortion in proposed VGA is much smaller than the previous signal-summing VGA design.

The exponential gain control circuit is shown in Fig. 4. The PMOS transistor M_{11} works in linear region and in common-source configurations. By combining the variable- gain stage and the exponential gain control circuit, the logarithmic current gain of the circuit becomes linear along with the control voltage as follows.

$$Gain_1\,(dB) = 10\times\log K_1 + 10\times C\times\log e + 10\times K_2\times\log e\times V_c \quad (2)$$

Where the K_1 and K_2 can be written as

$$K_1 = \frac{W_3}{W_4\left(V_{GS4} - V_{TH4}\right)} \quad K_2 = \frac{R_4 R_5}{R_5 + R_4}\cdot \mu_P C_{ox}\cdot \frac{W_{11}}{L_{11}} \quad (3)$$

D. Frequency Synthesizerr

Fig.5 shows the schematic of the frequency synthesizer. The frequency synthesizer consists of a phase frequency detector (PFD), a charge pump (CP), loop filters (LP), a voltage controlled oscillator (VCO), a swallow pulse frequency divider (SPFD) and a multi-mode frequency divider (MMFD). Compared to the ordinary structure, the proposed frequency synthesizer with additional MMFD can achieve better orthogonality and maintain wideband property.

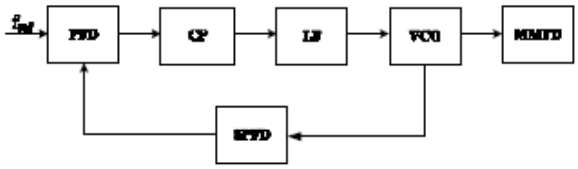

Figure 5. Schematic of the frequency synthesizer

E. Operation Principle and design of the proposed low power folded RF front end

The proposed RF front-end uses a folded mixer. Figure 6 shows the schematic of the folded Gilbert cell mixer. The use of folded technique can decrease the power consumption because the switching stage of the mixer does not need large current. High voltage headroom is also achieved. Another merit of the folded mixer is to have low flicker noise.

However, if PMOS is used at a switching stage of the mixer, flicker noise can be difference of CMOS technology is considered, the proposed RF front-end achieves the smallest power consumption and the highest gain among the other lowpower RF front-ends. The proposed folded RF front-end achieves not only the low power consumption, but also high gain compared with other RF front-ends.

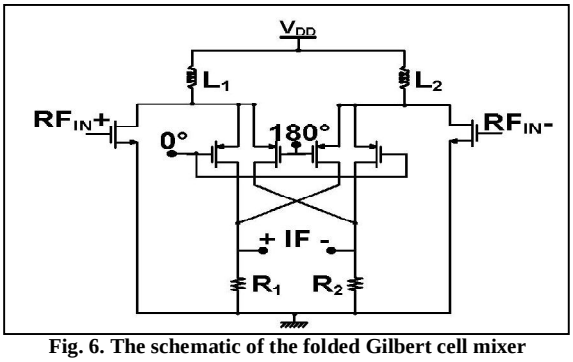

Fig. 6. The schematic of the folded Gilbert cell mixer

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Typically, two methods, folded technique and current reuse method, are used for low power operation . In folded technique, the stacked circuit is converted to a cascade circuit.

The power consumption decreases because VDD is lowered by reducing the stacks, while the chip size increases by the added inductor. This method can be applied to high gain circuits because this method increases the voltage headroom due to the reduced stacks. Current reuse method can decrease the current consumption by converting the cascade connected circuit to the stacked circuit.

By sharing current, the power consumption decreases. However, because this method can reduce the voltage headroom due to the increased stacks, its linearity is limited.

III. COMPARISON BETWEEN PROPOSED LOW POWER FOLDED RF FRONT END & GENERAL RF FRONT END

	Current(mA)	Power(mW)
Proposed Design	8.11	13.8
Conventional Design	46.35	78.8

From the above table we can summarize that the conventional design consumes six times more power than the proposed low power folded RF front end with merged LNA and Mixer The proposed RF front-end can be used in direct conversion receiver for a relatively narrow bandwidth system.

IV. EXPECTED RESULTS

A. Variable Gain Amplifier

Fig.8 shows the post-simulated voltage gain of VGA with the control voltage from 0.2 V to 1.6 V in 0.2 dB step. This VGA operates up to 700 MHz. The linear in-dB variable-gain range is from -10dB up to 18dB.

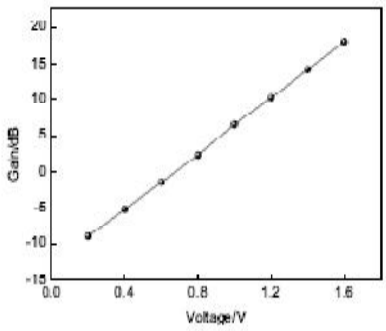

Figure 7. Post-simulated linear-in-dB characteristics of VGA

B. Frequency Synthesizer

When the control voltage is 0.9 V and the control-code is '0000', the post–simulated phase noise of VCO is shown in Fig 8.

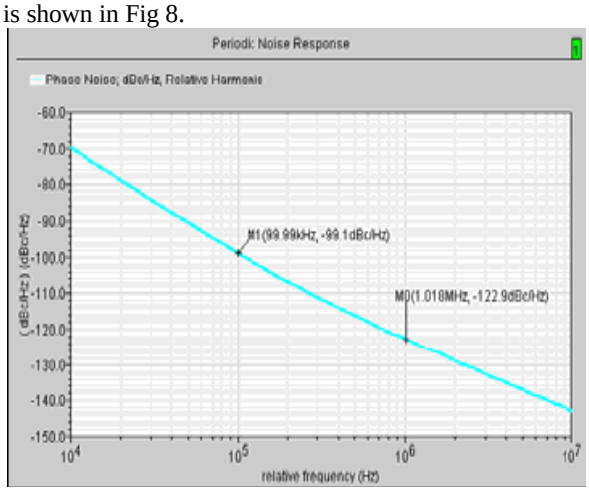

Figure 8. The post–simulated phase noise of the proposed VCO

V. CONCLUSION

In this paper, a broadband RF front-end for 0.1-2 GHz SDR radio receiver has been demonstrated in SMIC's 0.18 μm RF CMOS technology. The noise-canceling and DMGTR method breaks the trade-offs between the noise figure, source impedance matching and linearity. The proposed low power RF front-end is designed with current reuse technique and folded mixer in SIMC's 0.18 um CMOS process. The proposed RF front-end not only shows low power and high gain characteristics in comparison with those of other low power RF front-ends, The expected results of RF front-end are summarized in Table.1. Post-simulated results show that the performance of the RF front-end meets the requirement of SDR applications.

TABLE I. SUMMARY OF THE PROPOSED DESIGN

Freq. range	0.1-2 GHz
Gain. range	16-44 dB
NF (high gain)	3.8 dB@ 160MHz, 5.5 dB@2 GHz
OIP3@800 MHz	21.3 dBm
Phase noise of VCO	-122.9 @1 MHz
Phase Mismatch	<3°
Power	13.8mW@1.7V

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