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ZAHRA GHANE FASHTALI
Department of Electrical Engineering, Guilan University, Rasht City, Iran, zahra.ghane1986@gmail.com

MAHROKH MAGHSOODI
Department of Electrical Engineering, Guilan University, Rasht City, Iran, maghsoodi@guilan.ac.ir

REZA EBRAHIMI ATANI
Department of Computer Engineering , Guilan University, Rasht City, Iran, rebrahimi@guilan.ac.ir

MEHRGAN MAHDAVI
Department of Computer Engineering , Guilan University, Rasht City, Iran, mahdavi@guilan.ac.ir

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[1]ZAHRA GHANE FASHTALI, [2]MAHROKH MAGHSOODI, [3]REZA EBRAHIMI ATANI & [4]MEHRGAN MAHDAVI

[1,2]Department of Electrical Engineering, Guilan University, Rasht City, Iran
[3,4]Department of Computer Engineering , Guilan University, Rasht City, Iran
Email:[1]zahra.ghane1986@gmail.com, [2]maghsoodi@guilan.ac.ir, [3]rebrahimi@guilan.ac.ir , [4]mahdavi@guilan.ac.ir

Abstract—A fully differential low-power down-conversion mixer using a TSMC 0.18-µm CMOS process is presented in this paper. The proposed mixer is based on a folded double-balanced Gilbert cell topology that enhances conversion gain and reduces power dissipation. Though, this mixer is designed for 5.8 GHz ISM band applications, but at 0.5-7.5 GHz, the proposed mixer exhibits a maximum conversion gain of 12dB, maximum IIP3 of -2.5 dBm, maximum input 1-dB compression point of -13 dBm, the minimum DSB noise figure of 9.2 dB and a dc power consumption of 2.52 mW at 1.8 V power supply. Also, this circuit architecture increases port-to-port isolations to above 140 dB. Moreover this mixer is suitable for broadband applications.

Keywords*-braodband; ISM band; CMOS; low-power; folded ; mixer.*

I. INTRODUCTION

The industrial, scientific and medical (ISM) radio bands were originally reserved internationally for the use of RF electromagnetic fields for industrial, scientific and medical purpose other than communications. Current solutions exploit the worldwide license-free 2.4 GHz frequency band. Unfortunately, many applications nearly overcrowd this band such as high-power microwave ovens, cordless phones, Bluetooth and HomeRF applications, WLAN, game pads, etc. As a consequence, significant RF interference is present within the 2.4 GHz band [1]. Recently, wireless LAN system have been developed for the C-band (4 ~ 8 GHz) frequency. Proposals for wireless data system in the C-band range such as 5.8 GHz (wireless LAN for U.S.A) and 5.2 GHz (Hiper LAN for Europe) have been submitted [2]. The license-free 5.8 GHz frequency band provides wider spectrum frequency. Furthermore, investigations showed that 5 GHz applications in narrow surroundings can provide better performance than 2.4 GHz applications as the shorter wave length propagates farther. In addition, 5.8 GHz system nearly always be operated at higher data rates than 2.4 GHz systems in form of bandwidth [3]. There are a few mixers that work in 5.8 GHz frequency, for example a 5.8 GHz low power bulk-driven mixer is proposed in [4], that the supply voltage and the power consumption of this mixer is low well, but the noise figure of this mixer is high relatively. Another mixer with folded structure that operate in 5.8 GHz ISM band is proposed in [5], this mixer shows good performance in the case of conversion gain and noise figure at the expense of high power consumption. A 5.8 GHz mixer using SiGe HBT process is presented in [6] with the drawback of high supply voltage and high power consumption. Recently, a lot of effort has been spent on the development of low-voltage CMOS RF mixers. In [7], [8] LC tanks are used in the mixer to achieve low-voltage operation, but in CMOS technology, Q-value of the spiral inductor is relatively low, and the inductor occupies a lot of chip space. The transformer based architecture is adopted to reduce the dc power consumption in [9], but the 3-dB bandwidth is quite narrow due to the bandwidth limitation of the transformer. A low-voltage mixer using a folded Gilbert cell topology has been proposed in [10], but the noise figure of this mixer is rather high.

In this paper, a down-conversion CMOS mixer with low supply voltage is presented. In order to decrease the supply voltage and then reduce the power dissipation, folded structure is used to mixer design. Also, this work demonstrated the highest figure-of-merit (FOM) among the CMOS mixers.

The contents of this paper as follows. Section II shows the complete schematic of proposed mixer and working principle of the mixer. Section III is the conversion gain analysis of the mixer. In section IV, simulation results are presented, while the conclusion is presented in section V.

II. FOLDED MIXER CIRCUIT TOPOLOGY

The proposed low-power folded mixer was designed using the TSMC 0.18-µm CMOS technology. The circuit schematic of the down-conversion mixer is shown in Fig. 1. Compared with the conventional Gilbert cell mixer, the proposed mixer is based on a folded structure. The principle advantage of the proposed mixer is to allow the designer adjust the bias current in the transconductance (RF) stageeasily without affecting the switching (LO) stage in contrast with a conventional Gilbert-cell that have a stacked structure. The structure of the driver stage transistor closely resembles that of a simple differential pair amplifier. Input RF current is amplified and fed into the

switching quad network as in conventional Gilbert mixers. Ensuring that only AC current will flow into the switching quad, coupling capacitors C1 and C2 are used, the size of these capacitors will be limited by process restrictions and chip area.

To make mixer loads, we have to choose between resistors, LC circuit or PMOS transistors. The use of LC circuit is not an integrable solution .The use of PMOS transistors as active loads gets higher gain than resistors [11], for equivalent power consumption. Moreover, this will allow even higher gain without using up too much headroom and allows for smaller on chip space requirements as compared to a resistor. On the other hand, the linearity is worse. PMOS active loads in driver stage are implemented such that input RF current will flow up into the switching quad with sufficient gain and that transistors M1 and M2 are properly biased.

Degeneration resistor R_S will provide the overall mixer with improved linearity and stability during temperature fluctuations. Moreover, resistor degeneration was used because the circuit must operate over a broad bandwidth. In this circuit, the degeneration resistor was connected between the two current sink to improve linearity. This topology also helps headroom because there is no voltage drop across the degeneration resistor. The switching quad comprises of NMOS transistors M3, M4, M5 and M6, these transistors will oscillate (between ON and OFF states) according to the input frequency of the LO. PMOS active load also used in switching stages to convert mixed signal current into output IF voltage. The RF and LO signals are differential injected to the mixer so the IF output signal is fully differential.

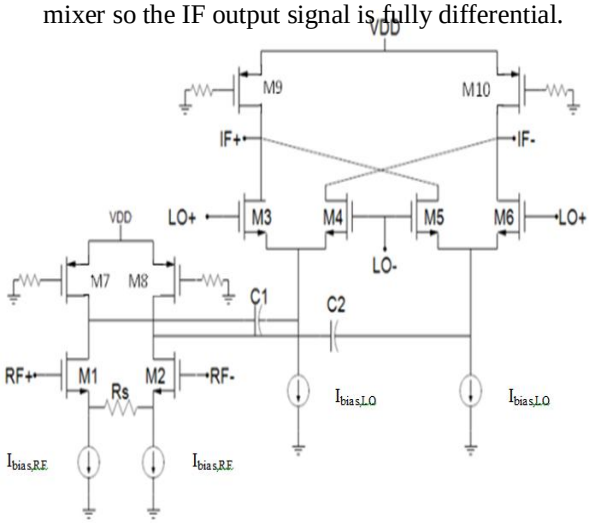

Fig. 1.Schematic of the proposed mixer.

III. CONVERSION GAIN AND PERFORMANCE ANALYSIS

According to the small signal equivalent circuit of the left hand branch, in one phase of the local oscillator when M3 is ON and M4 is OFF is shown in Fig. 2.

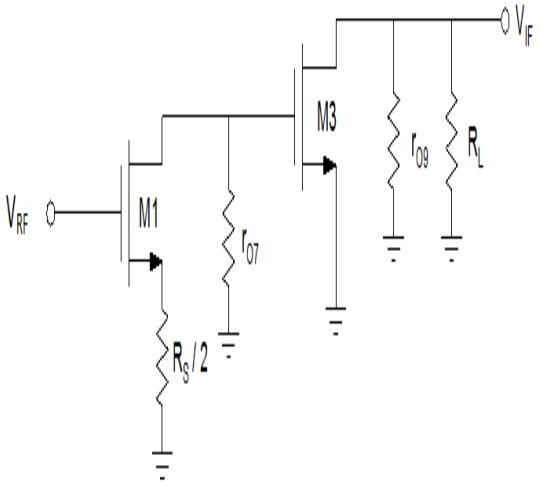

Fig. 2.Simplified small signal equivalent circuit of the left hand branch in one phase of the LO.

An approximation of the mixer gain is as follows

– ——————— (1)
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In the above expression, R_S is the source degeneration resistance that inserted to improve the linearity of the mixer. r_{O7} and r_{O9} are the output resistance of the PMOS active loads for the transconductance and switching stages, respectively. These transistors are biased in saturation region well to enhance the gain operation of the mixer.

This approximation is valid if the switching stage transistors are considered to act as perfect switches. In proposed mixer, the transconductance stage transistors are biased in strong-inversion region to achieve good gain and linearity, the switching transistors are biased in weak-inversion region to reduce power consumption, and the POMS active loads are biased in saturation to increase the conversion gain, because $r_{o\text{-}active}$ is greater than $r_{o\text{-}linear}$.

The NMOS device sizes of the driver stage (M1-M2) are 55 µm. The POMS transistors (M7-M8) of the driver stage with a total gate width of 3 µm are biased in saturation region as load resistors. The NMOS device sizes of the switching stage (M3-M6) are 23 µm, and the PMOS load transistors (M9-M10) sizes biased in saturation region, are 1.2 µm. The bypass capacitor is responsible for coupling the RF signal between two branches. The value of these capacitors are 2 pF. For this design, the optimal bias current of the driver stage is 1 mA , and the bias current of the switching stage to keep this stage in weak-inversion region is only 0.4 mA.

A summary of chosen parameters and mixer operating conditions is shown in Table I.

TABLE I . SUMMARY OF MIXER PERFORMANCE

RF Input Frequency	5.8 GHz
RF Input Power	-30 dBm
LO Input Frequency	5.7 GHz
LO Input Power	0 dBm
IF Output Frequency	100 MHz
Conversion Gain	10.5 dB
1 dB Compression Point	-17 dBm
IIP3	-2.5dBm
DSB NF	11 dB
Dc Power Consumption	2.52mW
Supply Voltage (V_{DD})	1.8 V

IV. SIMULATION RESULTS

The down-conversion mixer is designed with TSMC 0.18-µm CMOS process. The RF input power and LO input power are -30 dBm and 0 dBm, respectively for maximum conversion gain, and the IF output frequency is 100 MHz. At RF frequency of 5.8 GHz the simulated maximum conversion gain is 10.5dB. The simulated third-order intermodulation of the mixer in 5.8 GHz are plotted in Fig. 3, which features an input IP3 (IIP3) of -2.5dBm. The simulated input 1-dB compression point (IP_{1dB}) is about -17 dBm in 5.8 GHz, as shown in Fig. 4.

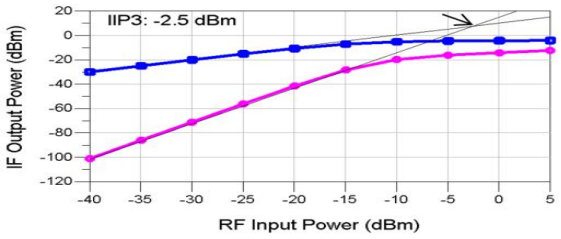

Fig.3.IIP3 of the proposed mixer in 5.8 GHz RF frequency.

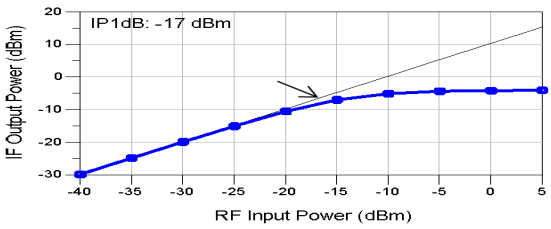

Fig.4.IP1dB of the proposed mixer in 5.8 GHzRF frequency

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The double-sideband (DSB) noise figure of the mixer with LO power sweep is shown in Fig. 5, that shown a 11dB, DSB NF at 0 dBm LO power and The double-sideband (DSB) noise figure against RF frequency from 0.5 GHz to 8 GHz are plotted in Fig. 6 where the IF frequency is fixed at 100 MHz, as can be seen from the figure, in 5.8 GHz RF frequency the DSB NF is 10.94dB. Thus, SSB NF is a about 13.94 dB in this frequency.

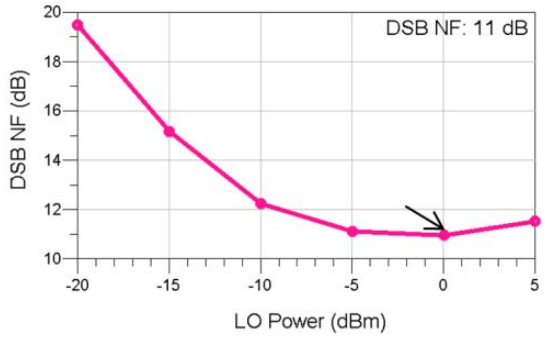

Fig.5. DSB NF against LO power.

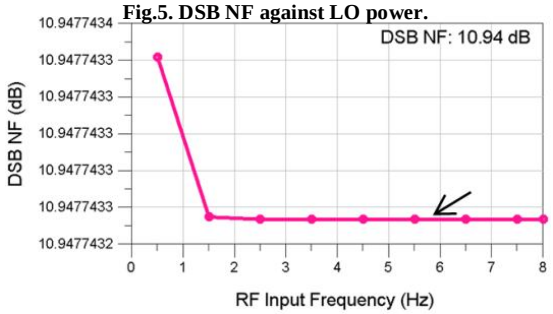

Fig.6.DSB NF against RF frequency.

The conversion gain against LO power is plotted in Fig. 7, which shows a conversion gain of 10.2 dB in 0 dBm LO power. The simulated conversion gain versus RF frequency from 0.5 GHz to 9 GHz is plotted in Fig. 8. As can be seen, the conversion gain from 0.5 to 7.5 GHz RF frequency is greater than 8 dB, in fact, the 3-dB RF bandwidth is about 7 GHz. Thus, the proposed mixer is very suitable for broadband applications. Mixer port-to-port (RF to IF, LO to IF and LO to RF) isolations are simulated and shown in Fig. 9. Isolations of more than 140 dB were achieved.

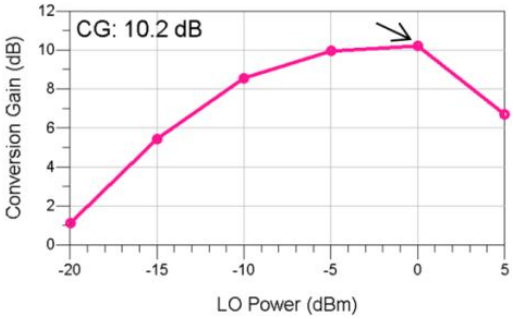

Fig. 7. Conversion gain against LO power.

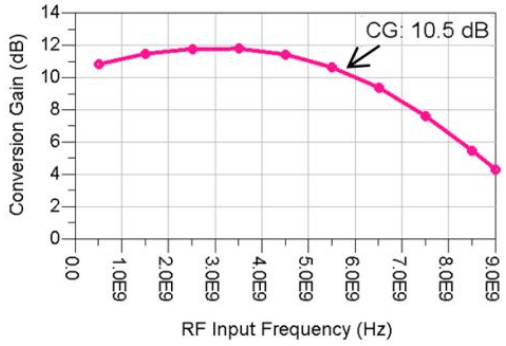

Fig. 8.Conversion gain against RF frequency.

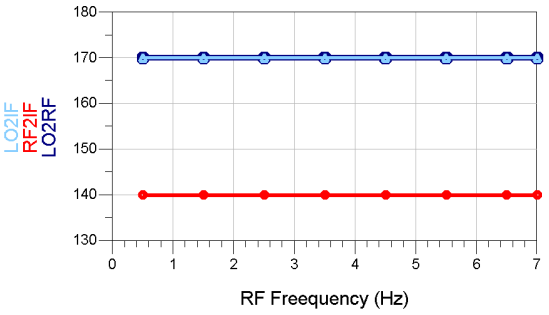

Fig. 9.Port-to-port isolations.

As can be seen, isolations are very good, that due to structure which is adopted to mixer design. The optimum DC supply voltage (V_{DD}) is 1.8 V with a total drain current of 1.4 mA, thus the mixer core dc power is 2.52 mW. However, this work is designed for 5.8 GHz ISM band applications, as can be seen from Fig. 8 the presented mixer is suitable for broadband applications.

In order to evaluate the performance of the proposed folded mixer, the performance summaries of the previously reported CMOS mixers and this work are summarized in Table II. The mixer□s figure of merit (FOM) can be expressed as [12]

(2)

where is the RF frequency in Hz, and NF represent the conversion gain and noise figure in dB, respectively. is the input referred third order intercept point in dBm, and is the power consumption in Watts. As can be seen, this work demonstrated the highest FOM of 218.5 among all the 0.18 µm CMOS circuits.

V. CONCLUSION

A CMOS down-conversion folded mixer has been presented. Which can operate at a 1.8-V supply voltage in a TSMC 0.18-µm CMOS technology. Folded structure is used to decrease supply voltage and power consumption. The 3-dB RF bandwidth of the proposed mixer is greater than 7 GHz with a IF frequency of 100 MHz. Though, this circuit is designed for 5.8 GHz ISM band applications also suitable for broadband applications. The dc power consumption of the mixer core is 2.52 mW and this mixer can achieve the good port-to-port isolations among the CMOS mixers.

TABLE II.COMPARISION OF PREVIOUSLY REPORTED MIXERS AND THIS WORK

Ref.	[4]	[5]	[9]	[10]	This work
CMOS Process (µm)	0.18	0.18	0.13	0.18	0.18
RF freq. (GHz)	5.8	5.8	2.1- 3	3.5-10	0.5-7.5
SSB NF (dB)	28	8.5	14.8	21	12.2
Gain (dB)	3.4	17	5.4	5	12
IIP3 (dBm)	11	-6	-2.8	-2.52	-2.5
P_{diss} (mW)	1	18	1.6	8	2.52
V_{DD}(V)	1	1.8	0.6	1.8	1.8
F.O.M (dB)	212	215	204	197.3	218.5

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