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A SPACE VECTOR PWM SCHEME FOR NEUTRAL POINT CLAMPED MULTILEVEL INVERTERS

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Abstract: Multilevel inverters are increasingly being used in high power medium voltage applications when compared to two level inverter due to their merits, such as lower common mode voltage, lower dv/dt, lower harmonics in output voltage and current. Among various modulation techniques for a multilevel inverter, space vector pulse width modulation is poplar due to the merits like, it directly uses the control variable given by the control system and identifies each switching vector as a point in complex space. However the implementation of the SVPWM for a multilevel inverter is complicated. The complexity is due to the difficulty in determining the location of the reference vector, the calculations of on times and the determination and selection of switching states. The multilevel SVPWM method uses the concepts of two level modulations to calculate the on times of an n-level inverter. Use of multilevel inverters has become popular for motor drive applications. Various topologies and modulation strategies will be studied from the available literature. This work is devoted to the study and simulation of a new NPC multilevel inverter system typically suitable for high-performance high-power applications. Simulation of this work will be done in MATLAB/Simulink .

Index Terms*—Multilevel inverter, neutral point clamped (NPC), space vector pulse width modulation (SVPWM), switching state, three-level inverter*

1. INTRODUCTION

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as an inverter. Two categories into which inverters can be broadly classified are two level inverters and multilevel inverters. One advantage that multilevel inverters have compared to two level inverters is minimum harmonic distortion. A multilevel inverter can be utilized for multipurpose applications, such as an active power filter, a static VAR compensator and machine drive for sinusoidal and trapezoidal current applications. Some drawbacks to the multilevel inverters are the need for isolated power supplies for each one of the stages, they are more expensive, and they are more difficult to control in software. This paper focuses on the analysis of a three-level inverter of desirable voltage and frequency has been achieved; however, harmonics distortion should be investigated during operation. The pulse width modulation (PWM) strategies are the most effective to control multilevel inverters. Even though space vector modulation (SVPWM) is complicated, it is the preferred method to reduce power losses by decreasing the power electronics devices switching frequency, which can be limited by pulse width modulation. Different aspects of the three-level NPC inverter will be discussed including the inverter topology. The operation theory will be discussed with the aspect of space vector pulse width modulation.

2. NEUTRAL POINT CLAMPED (NPC) INVERTER

In these inverters, the voltage across semiconductor Switches are limited by diodes connected to various DC levels as such it is called Diode Clamed Multilevel inverters. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors addition across source dc-bus. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology Neutral Point Clamped inverter was introduced. The functional diagram of an n-level NPC converter is shown in figure 1. Each leg contains four active switches S1 to S4 with ant parallel diodes D1 to D4. The capacitors at the DC side are used to split the DC input into two, to provide a neutral point Z. The clamping diodes can be defined as the diodes connected to the neutral point, DZ1, DZ2. When switches S2 and S3 are connected, the output terminal A can be taken to the neutral through one of the clamping diodes. The voltage applied to each of the DC capacitors is E, and it equals half of the total DC voltage V_d.

The advantages of NPC inverter are:

(i) All of the phases share a common dc bus, which minimizes the capacitance requirements of the inverter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection or an adjustable speed drive. (ii)The capacitors can be pre-charged as a group. (iii)Efficiency is high for fundamental frequency switching.

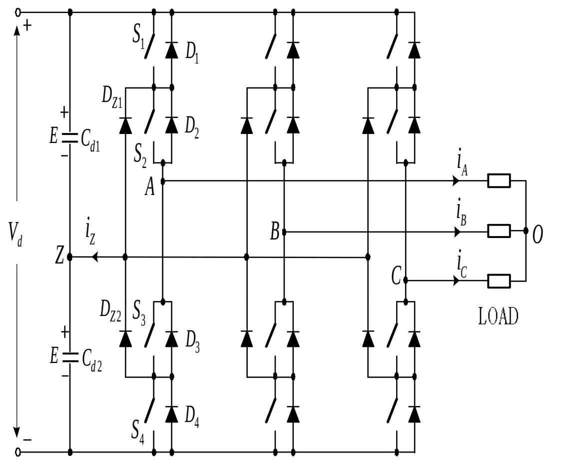

Fig.1; NPC Inverter

3. SPACE VECTOR PULSE WIDTH MODULATION FOR MULTI-LEVEL INVERTERS

Various Pulse Width Modulation (PWM) algorithms have been studied to control the multilevel inverter systems and Space Vector Modulation (SVPWM) method is a valid one. The most significant advantages of SVPWM are fast dynamic response and wide linear range of fundamental voltage compared with the conventional PWM. But when it is applied to the diode clamped inverter and flying capacitor inverter, the SVPWM strategy also has to solve the neutral-point voltage unbalance problem. There are three main steps to obtain the proper switching states during each sampling period for the SVPWM method:

1) Choose the proper basic vectors.
2) Calculate the dwelling time of each selected vectors.
3) Select the proper sequence of the pulse.

Choose the proper basic vectors: As shown in Fig.2. There are altogether **27** switching States in diode-clamped three-level inverter. They correspond to 19 voltage vectors whose Positions are fixed.

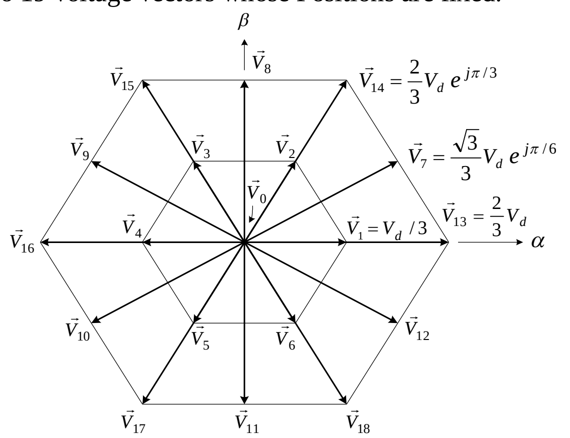

Fig.2. Space vector diagram

Space Vector		Switching State		Vector Classification	Vector Magnitude
V_0		[1 1 1] [-1 -1 -1] [0 0 0]		Zero vector	0
		P-type	N-type	Small vector	$\frac{1}{3}V_d$
V_1	V_{1P}	[1 0 0]			
	V_{1N}		[0 -1 -1]		
V_2	V_{2P}	[1 1 0]			
	V_{2N}		[0 0 -1]		
V_3	V_{3P}	[0 1 0]			
	V_{3N}		[-1 0 -1]		
V_4	V_{4P}	[0 1 1]			
	V_{4N}		[-1 0 0]		
V_5	V_{5P}	[0 0 1]			
	V_{5N}		[-1 -1 0]		
V_6	V_{6P}	[1 0 1]			
	V_{6N}		[0 1 0]		
V_7		[1 0 -1]		Medium vector	$\frac{\sqrt{3}}{3}V_d$
V_8		[0 1 -1]			
V_9		[-1 1 0]			
V_{10}		[-1 0 1]			
V_{11}		[0 1 1]			
V_{12}		[1 -1 0]			
V_{13}		[1 -1 -1]		Large vector	$\frac{2}{3}V_d$
V_{14}		[1 1 -1]			
V_{15}		[-1 1 -1]			
V_{16}		[-1 1 1]			
V_{17}		[-1 -1 1]			
V_{18}		[1 -1 1]			

Table1: voltage and switching states

These space voltage vectors can be classified into 4 groups: large voltage vector (VI,, VI, etc.), medium voltage vector, small voltage vector and zero voltage vector *(Vo).* The plane can be divided into 6 major triangular sectors (I to VI enclosed by solid lines) by large voltage vectors and zero voltage vector. Each major section represents *60'* of the fundamental cycle. Within each major sector, there are 4 regions. There are totally **24** regions in the plane. And the vertices of these regions represent the voltage vectors. Notice Table 1, each small voltage vector and zero voltage vector have **2** and **3** redundant switching states, respectively.

Calculation of duty cycles:

The space vector diagram that is shown in Fig. 2 can be used to calculate the time for each sector (I to VI). Each sector has four regions (1 to 4), as shown in fig. 3, with the switching states of all vectors. The sum of the voltage multiplied by the interval of chose space vector equals the product of the reference voltage *ref V* and sampling period T_s. To illustrate, when reference voltage is located in region of sector I then the nearest vectors to reference voltage are 1 7 2 V ,V ,and V as shown in Fig. 3, and the next equations explain the relationship between times and voltages :-

$$V_1T_a+V_7T_b+V_2T_c=V_{ref}T_s \qquad (1)$$
$$T_a+T_b+T_c=T_s$$

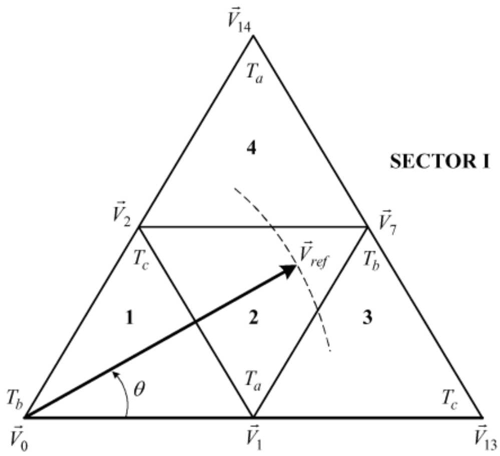

Fig.3 voltage vector 1 and their times

Now substitute V_1,V_2 and V_7 values from table.1 in equation 1. And get result

$-V_dT_a+—V_d(\cos-+j\sin-)T_b+-V_d\ (\cos-+j\sin-)T_c=V_{ref}(\cos\theta+j\sin\theta)$ (2)

From equation (2) real part and imaginary part can be determined by following equations

Re $T_a+-T_b+-T_c=3—(\cos\theta)T_s$ (3)

Im $-T_b+—T_c=3—(\sin\theta)T_s$

By solving equation (3) with the equation for total time $T_s = T_a + T_b + T_c$. then we get time expressions T_a ,T_b and T_c of region2 as shown in table2. In other regions such as 1, 3, 4 etc. the duration of each voltage vector can be calculated in similar fashion.

Region	T_a		T_b		T_c	
1	$\vec{V}_1$	$T_s\left[2m_a\sin\left(\frac{\pi}{3}-\theta\right)\right]$	$\vec{V}_0$	$T_s\left[1-2m_a\sin\left(\frac{\pi}{3}+0\right)\right]$	$\vec{V}_2$	$T_s[2m_a\sin\theta]$
2	$\vec{V}_1$	$T_s[1-2m_a\sin\theta]$	$\vec{V}_7$	$T_s\left[2m_a\sin\left(\frac{\pi}{3}+\theta\right)-1\right]$	$\vec{V}_2$	$T_s\left[1-2m_a\sin\left(\frac{\pi}{3}-\theta\right)\right]$
3	$\vec{V}_1$	$T_s\left[2-2m_a\sin\left(\frac{\pi}{3}+\theta\right)\right]$	$\vec{V}_7$	$T_s[2m_a\sin\theta]$	$\vec{V}_{13}$	$T_s\left[2m_a\sin\left(\frac{\pi}{3}-\theta\right)-1\right]$
4	$\vec{V}_{14}$	$T_s[2m_a\sin\theta-1]$	$\vec{V}_7$	$T_s\left[2m_a\sin\left(\frac{\pi}{3}-\theta\right)\right]$	$\vec{V}_2$	$T_s\left[2-2m_a\sin\left(\frac{\pi}{3}+\theta\right)\right]$

Table2. time calculation eq for sector1

The Switching States by Using Switching Sequence:

By considering the switching transition and using sequences direction, shown in Fig. 4. The direction of the switching sequences for all regions in six sectors can be derived and the switching orders are given in the tables below, which are obtained for each region located in sectors I to VI, if all switching states in each region are used. From diagram shows thirteen segments of region 1 for each sector, shows nine segments of region 2 for each sector, shows seven segments of region 3 for each sector and shows seven segments of region 4 for each sector. For example region 4 switching sequence swon in fig5

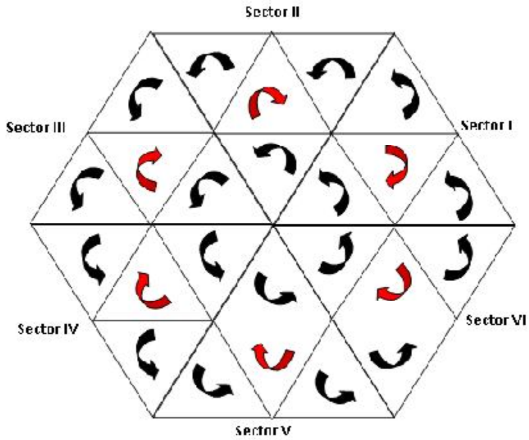

Fig.4. Switching sequence for three-level SVPWM inverter

Switching Segments							
Sector	1	2	3	4	5	6	7
I.	$\vec{V}_{2N}$	$\vec{V}_7$	$\vec{V}_{14}$	$\vec{V}_{2P}$	$\vec{V}_{14}$	$\vec{V}_7$	$\vec{V}_{2N}$
	00-1	10-1	11-1	110	11-1	10-1	00-1
II.	$\vec{V}_{3N}$	$\vec{V}_8$	$\vec{V}_{15}$	$\vec{V}_{3P}$	$\vec{V}_{15}$	$\vec{V}_8$	$\vec{V}_{3N}$
	-10-1	01-1	-11-1	010	-11-1	01-1	-10-1
III	$\vec{V}_{4N}$	$\vec{V}_9$	$\vec{V}_{16}$	$\vec{V}_{4P}$	$\vec{V}_{16}$	$\vec{V}_9$	$\vec{V}_{4N}$
	-100	-110	-111	011	-111	-110	-100
IV.	$\vec{V}_{5N}$	$\vec{V}_{10}$	$\vec{V}_{17}$	$\vec{V}_{5P}$	$\vec{V}_{17}$	$\vec{V}_{10}$	$\vec{V}_{5N}$
	-1-10	-101	-1-11	001	-1-11	-101	-1-10
V	$\vec{V}_{6N}$	$\vec{V}_{11}$	$\vec{V}_{18}$	$\vec{V}_{6P}$	$\vec{V}_{18}$	$\vec{V}_{11}$	$\vec{V}_{6N}$
	0-10	0-11	1-11	101	1-11	0-11	0-10
VI.	$\vec{V}_{1N}$	$\vec{V}_{12}$	$\vec{V}_{13}$	$\vec{V}_{1P}$	$\vec{V}_{13}$	$\vec{V}_{12}$	$\vec{V}_{1N}$
	0-1-1	1-10	1-1-1	100	1-1-1	1-10	0-1-1

Seven segments of region 4 for each sector

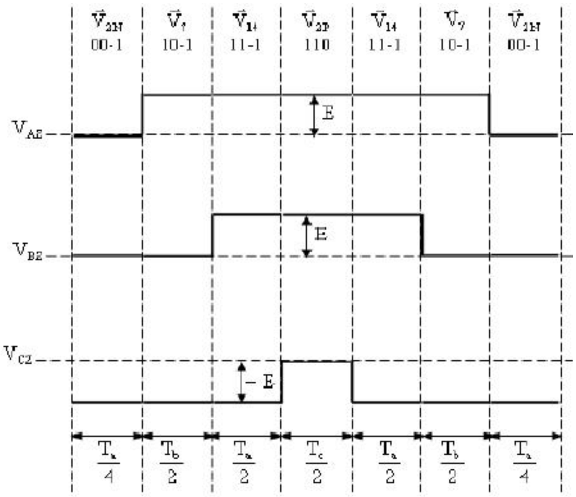

Fig5. Switching sequence of nine segments for Vref in sector I region 4

5. SIMULATION RESULTS:

Simulation of various inverters using sinusoidal pulse width modulation was carried out with the help of "MATLAB 6.5". Simulation was carried out to observe the improvement in the line voltage THD and Line Current THD as the inverter level increases from 2-level and 3-level. The fig.6 shows final simulation diagram and corresponding simulation results of line voltages, phase voltages and THD results are shown in fig.7, fig.8 and fig.9. And also fig.10 shows THD analysis of 2-level inverter. Fig.11 shows Space vector modulation output waveform of three level inverter.

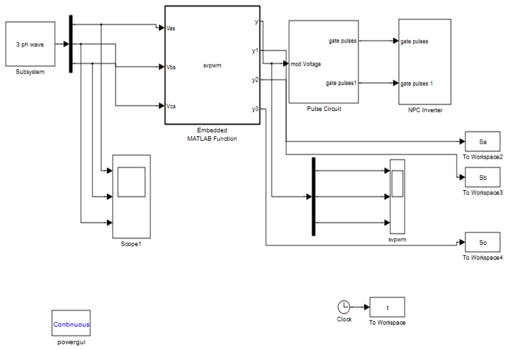

Fig.6 simulation diagram

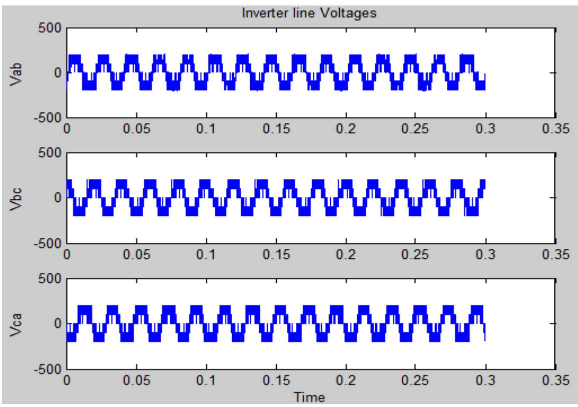

Fig.7 Inverter line voltages

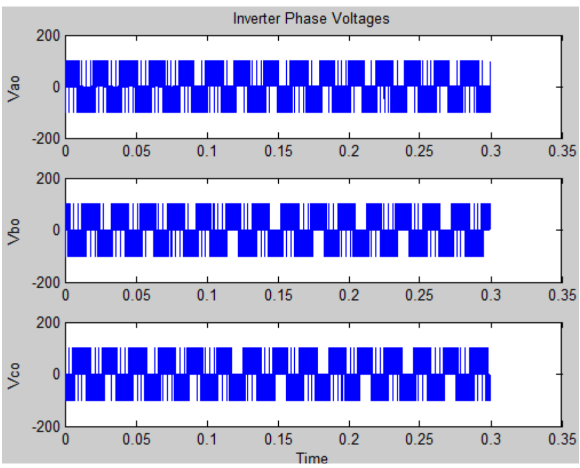

Fig.8 Inverter phase voltages

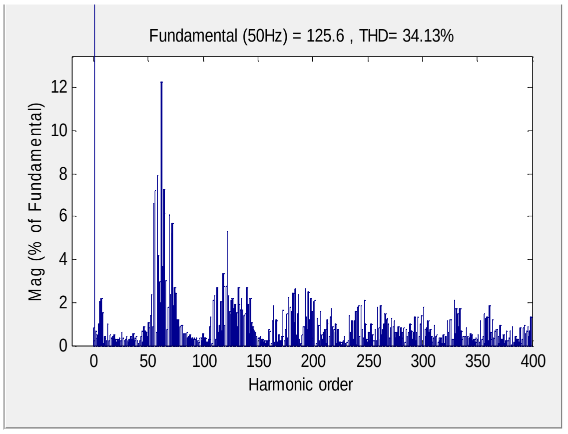

Fig.9 THD results for 3-level inverter

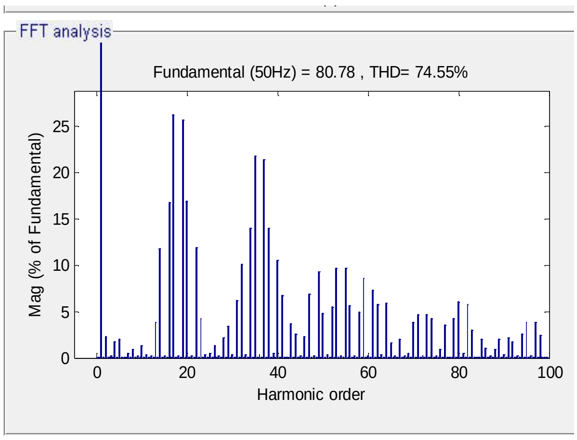

Fig.10 THD results for 2-level inverter

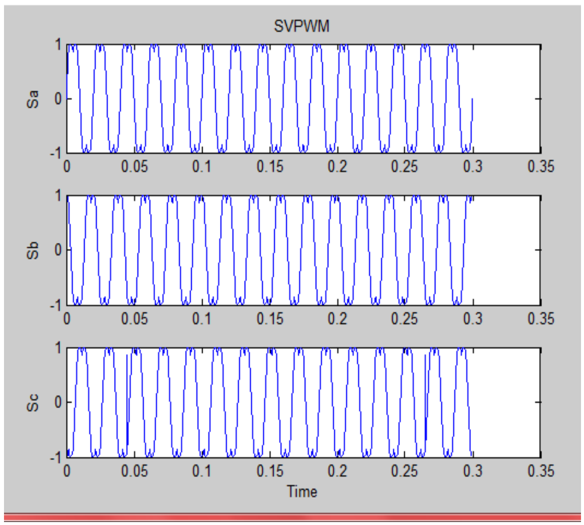

Fig.11 Space vector modulation out put waveform

6. CONCLUSION:

Space vector pulse width modulation algorithm has been described and applied to two-level, three-level inverter. Compared with conventional methods, this method has the advantage of ease implementing, especially for the inverters with more levels. From simulation results it is observed that the generated voltage spectrum is very much improved with increase the level of inverter. The total harmonic distortion (THD) is highly reduced as the level of the inverter is increases. It needs no additional reactors or transformers to reduce the harmonic components. Then, it is suitable for high voltage and high power systems.

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