DESIGN, IMPLEMENTATION AND ANALYSIS OF FLASH ADC ARCHITECTURE WITH DIFFERENTIAL AMPLIFIER AS COMPARATOR USING CUSTOM DESIGN APPROACH

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Abstract— Analog-to-Digital Converters (ADCs) are useful building blocks in many applications such as a data storage read channel and an optical receiver because they represent the interface between the real world analog signal and the digital signal processors. Many implementations have been reported in the literature in order to obtain high-speed analog-to-digital converters (ADCs). In this paper an effort is made to design 4-bit Flash Analog to Digital Converter [ADC] using 180nm cmos technology. For high-speed applications, a flash ADC is often used. Resolution, speed, and power consumption are the three key parameters for an Analog-to-Digital Converter (ADC). The integrated flash ADC is operated at 4-bit precision with analog input voltage of 0 to 1.8V. The ADC has been designed, implemented & analysed in standard gpdk180nm technology library using Cadence tool.

Keywords*— Flash ADC, Resolution, power consumption, gpdk180*
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I. INTRODUCTION

With the rapid growth of modern communications and signal processing systems, handheld wireless computers and consumer electronics are becoming increasingly popular. Mixed-signal integrated circuits have a tendency in the design of system-on-chip (SOC) in recent years. SOC designs have made possible substantial cost and form factor reductions, in part since they integrate crucial analog interface circuits, such as ADCs with digital computing and signal processing circuits on the same die. The interfaces only occupy a small fraction of the chip die and for SOC designs, the technology selection and system design choices are mainly driven by digital circuit requirements [1].

For high-speed applications, a flash ADC is often used. Resolution, speed, and power consumption are the three key parameters for an analog-to-digital converter (ADC). These parameters cannot be changed once an ADC is designed. While one can use 6-bit precision from an 8-bit ADC, it is non-optimal resulting in slower speed and extra power consumption due to full 8-bit internal operation. In this paper, a new flash ADC design is proposed that is a true variable-power and variable-resolution ADC. It can operate at higher speed and will consume less power when operating at a lower resolution. Such features are highly desirable in many wireless and mobile applications. For example, the strength of a radio frequency (RF) signal varies greatly depending on geographic location. Optimally, the ADC resolution can be reduced upon the reception of strong signal and can be increased upon the reception of weak signal. Substantial reduction in power consumption at lower resolution will prolong the battery life [1]. Low power ADC architectures are implemented with pipelined, successive approximation, and sigma-delta modulators. These are all useful for the medium speed conversion and high resolution applications. On the other hand, the flash architecture is suitable for high speed conversion and low resolution applications due to its parallel architecture.

II. BACKGROUND

The paper on "The CMOS Inverter as a Comparator in ADC Designs", spinger Analog Integrated Circuits and Signal Processing, Vol.39, pp.147-155, 2004 by Tangel A. Choi K discussed about the advancement of technology, digital signal processing has progressed dramatically in recent years.

Signal processing in digital domain provides high level of accuracy, low power consumption and small silicon area besides providing flexibility in design and programmability. The design process is also quite faster and cost effective. Furthermore, their implementation makes them suitable for integration with complex digital signal processing blocks in a compatible low-cost technology, particularly CMOS [1].

This evolution of technology provides much faster transistors with smaller sizes, making it possible to have very high clock rate in digital circuits. In the end, it leads us to design a very high speed as well as systems with small die area called System on a chip (SoC), with a smaller number of chips using increased integration level.

However, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters", 2nd Edition, 2005 by Rudy J. van de Plassche et al, deals with the evolution

of technology has not provided same level of benefit for the analog circuit design. So to extract the advantages of digital signal processing, there is a trend of shifting signal processing from analog to more efficient digital domain and dealing with the analog signals only in the input-output stages. This has resulted in the requirement of smart converters between analog and digital signals to cope up with the evolution of technology [3].

Section III discuss about the ADC architecture, in the mean while Section IV about its Implementation. Section V, VI describes the experimental results and Conclusion respectively.

III. FLASH ADC ARCHITECTURE

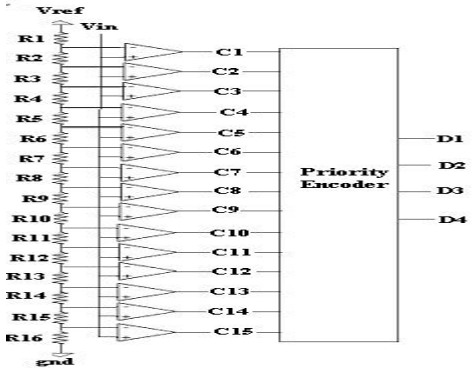

Fig.1: Flash ADC architecture

The above Fig.1., shows a typical flash ADC block diagram. For an "4" bit converter, the circuit employs 2^4-1= 15 comparators. A resistive divider with 2^4 = 16 resistors provides the reference voltage The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a "1" when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is "0". The Flash ADC consists of the following components which are given below:

***1. Resister string*:** In an 'n' bit flash ADC, 2^n resistances are necessary. The two extreme resistors are calculated to delimit the voltage input range. Each resistor divides the reference voltage to feed a comparator. The higher the resistance value is, the weaker the current is consumed in the device. That is why a high resistance will minimize power dissipation. Nevertheless, we have to put a reasonable value for this resistor string: it should stand lower than the input resistance of the comparators.

***2. Comparator*:** Here 2^n-1 differential amplifiers are used as comparators in"n" bits flash-ADC architecture. We first tried to implement a complex type of differential amplifier. But this element was not easy enough to understand and use for beginners. We consequently decided to prefer a basic design to realize our ADC. This decision made us loose several advantages as an improved gain, or power savings that would have benefit to our ADC precision and efficiency. When the input signal voltage is less than the reference voltage, the comparator output is at logic '0'.when the input signal voltage is higher than the reference voltage, the comparator output is at logic '1'. The comparators give the 2^n-1 levels of outputs in terms of reference voltage.

***3. Priority encoder*:** The output of the comparators is in the encoded form. Therefore a priority encoder has to be designed in order to convert the encoded signal into n bits data (digital) which is unipolar binary code[4][6].

VI. DESIGN AND IMPLEMENTATION

This section deals with implementation of three components as discussed in section III.

1. The resistor string

The 4 bit flash ADC, needs 2^4 resistances [fig.,1]. The two extreme resistors are calculated to delimit the voltage input range. Each resistor divides the reference voltage to feed a comparator. The higher the resistance value is, the weaker the current is consumed in the device. That is why a high resistance will minimize power dissipation. Nevertheless, we have to put a reasonable value for this resistor string: it should stand lower than the input resistance of the comparators. We expected to convert any voltage between 0 and 1.8 V.

In general, the voltage division takes place as follows:

$$V_a = (M*V_{ref})/2^n \quad \ldots\ldots\ldots\ldots\ldots (1)$$

Where,

M = No., of resistors at which voltage division occurs.

n = No., of bits.

2^n = Total No., of resistors used.

The design of resister string for proposed Flash ADC is done using schematic approach in cadence as shown in fig., 2.

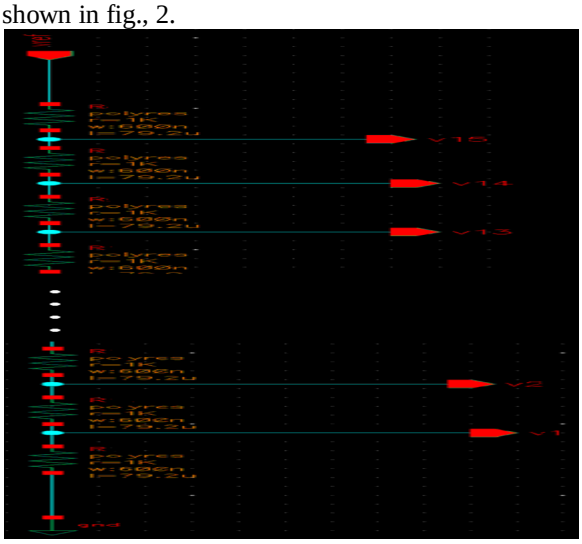

Fig. 2: Resistor string for proposed flash ADC.

The Table I show the voltage division for resistor string with reference voltage is taken to be 1.8 V.

Table I: Voltage division occurs as follows:

M *	V_a*= $(M*V_{ref})/2^n$
Tap 1	0.1125V
Tap 2	0.225V
Tap 3	0.3375V
Tap 4	0.45V
Tap 5	0.5625V
Tap 6	0.675V
Tap 7	0.7875V
Tap 8	0.9V
Tap 9	1.0125V
Tap 10	1.125V
Tap 11	1.2375V
Tap 12	1.35V
Tap 13	1.4625V
Tap 14	1.575V
Tap 15	1.6875V
Tap 16	1.8V

*M= Resistor tap Number & V_a=Voltages of each resistor tap

2. The Comparator

The proposed flash ADC consists of comparator as one of the important component, this comparator is designed in such a way that which is less immunity for noise and with high common mode rejection ratio. Hence, the Differential Amplifier is used to achieve the same.

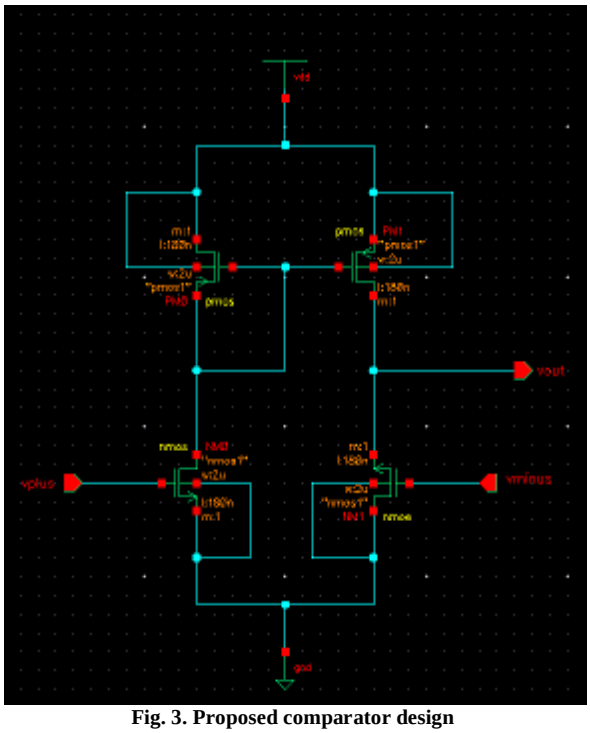

Fig. 3. Proposed comparator design

Hence forth the design of comparator is shown in fig. 3., uses 2^4-1=15 differential amplifiers are used as comparators in 4-bit flash-ADC architecture.

Working of Comparator:

When the input signal voltage is less than the reference voltage, the comparator output is at logic '0'.when the input signal voltage is higher than the reference voltage, the comparator output is at logic '1'. The comparators give the 15 levels of outputs in terms of reference voltage. In transient response, during 0 to 5ns time V1 is '0',V2 is '1',so output will be '0' because V1<V2 and during 5 to 10 ns time V1 is '1',V2 is '0', so output will be '1' because V1>V2.

3. Priority encoder stage:

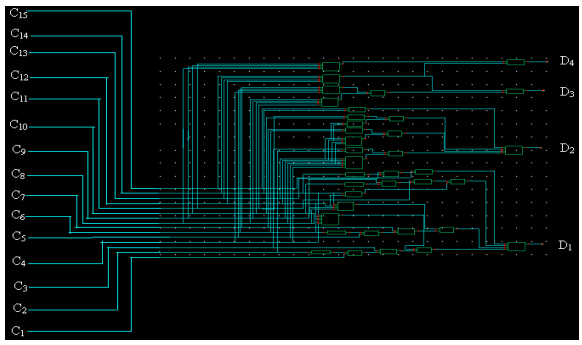

Fig. 4: Priority encoder stage

The output of the comparators is in the encoded form. Therefore a priority encoder has to be designed in order to convert the encoded signal into 4 bits data (digital) which is unipolar binary code.

The logic employed in designing the priority encoder is explained as follows,

$D1=C_1C'_2C'_4C'_6C'_8C'_{10}C'_{12}C'_{14}+C_3C'_4C'_6C'_8C'_{10}C'_{12}C'_{14}+C_5C'_6C'_8C'_{10}C'_{12}C'_{14}+C_7C'_8C'_{10}C'_{12}C'_{14}+C_9C'_{10}C'_{12}C'_{14}+C_{11}C'_{12}C'_{14}+C_{13}C'_{14}+C_{15}$.

$D2=C_2C'_4C'_5C'_8C'_9C'_{12}C'_{13}+C_3C'_4C'_5C'_8C'_9C'_{12}C'_{13}+C_6C'_8C'_9C'_{12}C'_{13}+C_7C'_8C'_9C'_{12}C'_{13}+C_{10}C'_{12}C'_{13}+C_{11}C'_{12}C'_{13}+C_{14}+C_{15}$.

$D3=C_4C'_8C'_9C'_{10}C'_{11}+C_5C'_8C'_9C'_{10}C'_{11}+C_6C'_8C'_9C'_{10}C'_{11}+C_7C'_8C'_9C'_{10}C'_{11}+C_{12}+C_{13}+C_{14}+C_{15}$.

$D4 = C_8+C_9+C_{10}+C_{11}+C_{12}+C_{13}+C_{14}+C_{15}$.

V. EXPERIMENTAL RESULTS

This Section clearly disscuss about the simulation results of above said three important components of flash ADC, the work is carried out on cadence virtuoso the simulation is done using spectre and layout using assura.

Fig.5., discuss about transient response for resistor string of voltage at resister taps. These tap voltages become inputs to comparator stage.

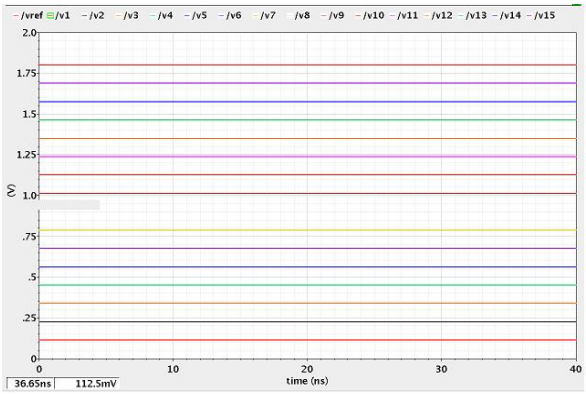

Fig. 5: Transient response for resistor string.

When the input signal voltage is less than the reference voltage, the comparator output is at logic '0',when the input signal voltage is higher than the reference voltage, the comparator output is at logic '1'. The comparators give the 15 levels of outputs in terms of reference voltage. In transient response, during 0 to 5ns time V_1 is '1',V_2 is '0', hence output will be '1' because $V_1 > V_2$ and during 5 to 10 ns time V_1 is '0',V_2 is '1', hence output will be '0' because $V_1 < V_2$ shown in Fig.6.,

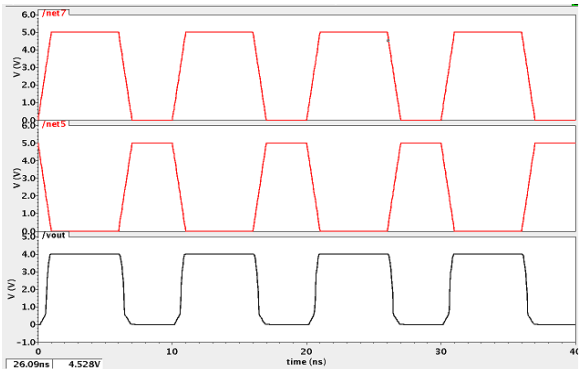

Fig.6: Transient response for comparator

The schematic simulation of 4 bit Flash ADC using Cadence tool is shown in Fig.7-11.

Fig.7., shows transient response for Vin = 0V, so here Vin will be in range between 0≤Vin≥0.112, so comparator output will be "000000000000000" and priority encoder output will be "0000".

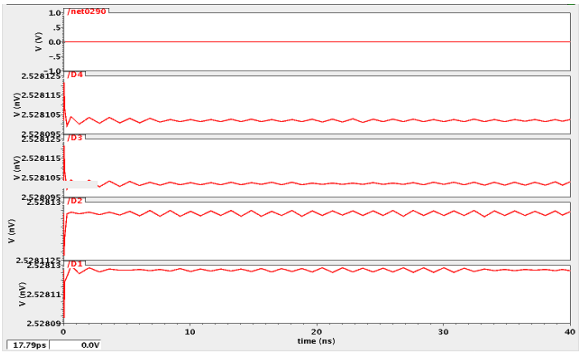

Fig.7: Transient response for V_{in}=0V, output will be 0000

Fig. 8 shows transient response for Vin = 0.8V, so here Vin will be in range between 0.7875≤Vin≥0.9, so comparator output will be "000000011111111" and priority encoder output will be "0111".

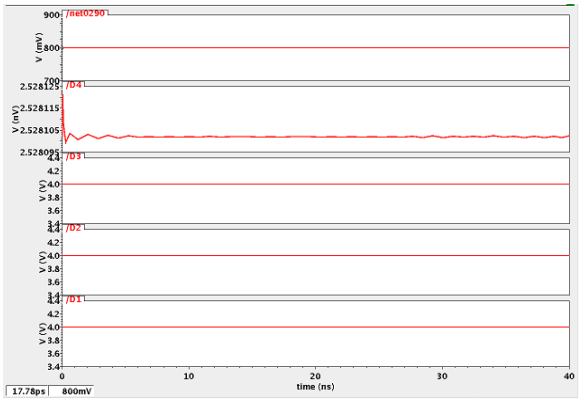

Fig 8: Transcient response for V_{in}=0.8V, output will be 0111

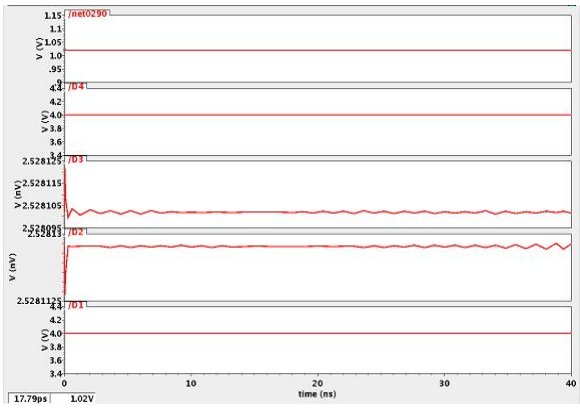

Fig.9: Transient response for V_{in} = 1.02V, output will be 1001

Fig. 9 shows transient response for Vin = 1.02V, so here Vin will be in range between 1.0125≤V_{in}≥1.125, so comparator output will be "000000111111111" and priority encoder output will be "1001".

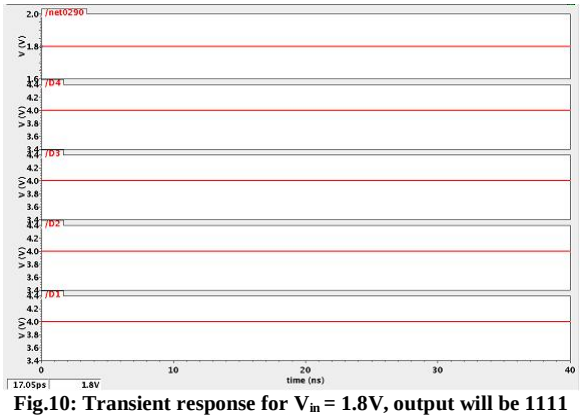

Fig.10: Transient response for V_{in} = 1.8V, output will be 1111

Fig.10. shows transient response for Vin = 1.8V, so here Vin will be in range between 1.6875≤V_{in}, so comparator output will be "111111111111111" and priority encoder output will be "1111".

Table II. Specifications Summary of ADC

Technology	180ηm
Analog voltage, V_{in}	0 to 1.8V
Reference voltage, V_{ref}	1.8V
V_{dd}	4V
Resolution	4-bits
Speed	3.8 GS/sec
Power Dissipation	49.94mW
SNR	25.84 dB
Standard Deviation	12ηs
Mean	19ηs
Calculated layout area	821634.145 $(\eta m)^2$

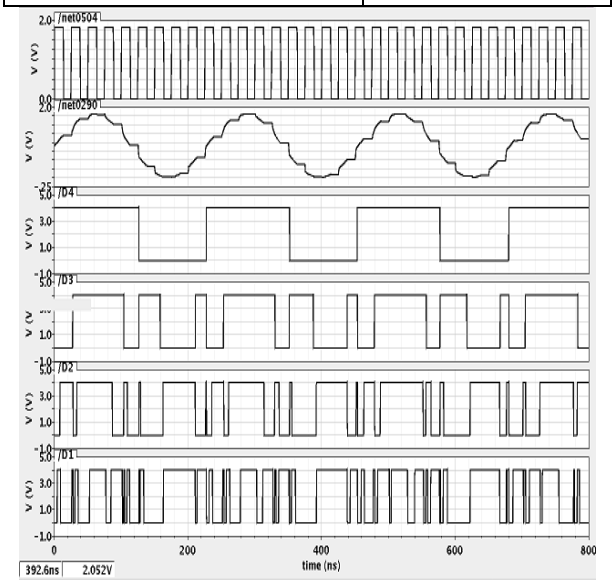

Fig. 11: Flash ADC outputs for analog input of 0 to 1.8V and 4.4M Hz Input frequency

Fig.11., shows outputs for analog input of 0 to 1.8V and 4.4M Hz input frequency using sample and hold circuit.

VI. Layout design for proposed ADC design

Layout design of resister string made up of 16 polyresisters metals, which is connected to 15 outputs with Metal1-poly, this design is made inside PR (Place and Route) boundary, each Resister is constructed from polycrystalline silicon and poly is having width of 600ηm, segment length of 79.2µm, sheet resistivity 7.5Ω, body resistance 990Ω, contact resistance 10Ω and end resistance 0Ω. Layout design of comparator, totally it contains two pmos & nmos of gpdk180 libraries, where pmos is connected with nwell & nmos with psubstrate,each comparator is constructed from 32 pcapacitor & 13 presister pmos and nmos of width 2µm and length 180ηm. Calculated layout area is 821634.1415 $(\eta m)^2$.

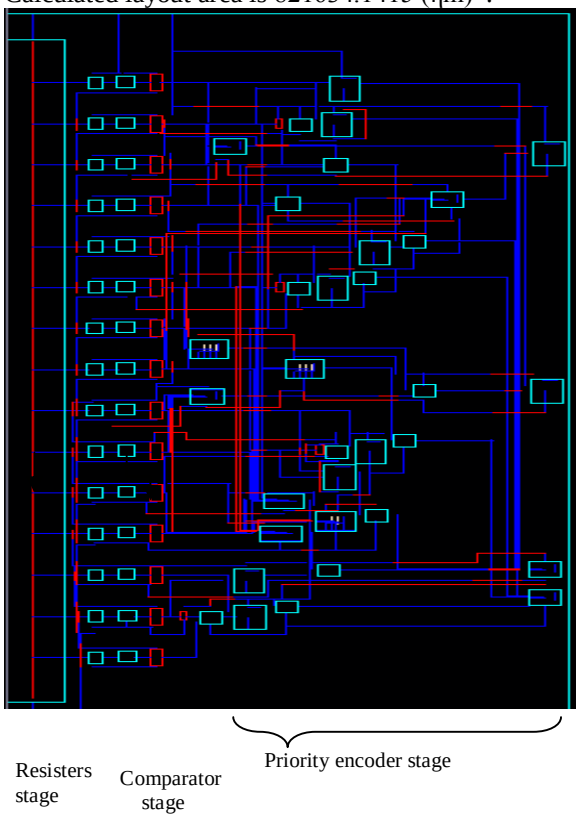

Fig. 12: Layout design of Flash ADC

VII.CONCLUSION

The schematic and layout of register stage, comparator stage, and priority encoder stage are designed and integrated. From table II Gives brief design summary of flash ADC i.e., the integrated flash ADC is operated at 4-bit precision with analog input voltage of 0 to 1.8V, supply voltage 4V, Resolution 4bits, SNR 25.84dB, consumes 49.94mW power, speed is 3.8GS/s and layout Area is $0.821634\mu m^2$. The ADC is designed and implemented in standard gpdk180nm cmos technology of version – IC 6.1 using Cadence virtuoso tool.

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