Five Level Flying-Capacitor Multilevel Converter Using Dynamic Voltage Restorer (DVR)

K. Ramakrishna Reddy & G. Koti Reddy

Narasaraopet Engineering College, Narasaraopet
E-mail : krkr97@gmail.com, gogulamoodikotireddy@gmail.com

Abstract **-** This paper deals with dynamic voltage restorer (DVR) controlled by a five-level flying-capacitor multi level converter. To decrease the power-quality disturbances in distribution system, such as voltage imbalances, harmonic voltages, and voltage sags. The organisation of this paper has been divided into three parts; the first one eliminates the modulation high-frequency harmonics using filter increase the transient response. The second one deal with the load voltage; and the third is flying capacitors charged with balanced voltages. The MATLAB simulation results effectively for five level flying capacitor multilevel converters charged with balanced voltage regulation.

Key words *- Dynamic voltage restorer (DVR), flying capacitor multilevel converter, Power quality (PQ), Voltage sags.*

I. INTRODUCTION

Dynamic Voltage Restorers (DVR) are an efficient and economic means to mitigate voltage sags and swells. The DVR is a series connected device, which primarily can protect sensitive electric consumers against voltage dips and surges in the medium and low voltage distribution grid. The main components of DVR are controller, voltage source inverter, energy source for DC link capacitor, filters and interfacing transformers. The DVR is basically a voltage source inverter which compensates the missing voltage by rapidly injecting set of three phase voltages into the lines via booster transformer. The voltages can be controlled both in magnitude as well as phase. The generated voltages are rapidly injected into the line via booster transformer without any time delay. This significantly improves the dynamic response of DVR.

The balancing of FC voltages is quite important and dictates both the safe and efficient operation of the converter. If voltage imbalance occurs, the quality of the output voltages will deteriorate and blocking voltages imposed on certain devices may increase beyond the rated values. Thus, the safe operation of power devices cannot be guaranteed.

Therefore, it is necessary to take into account the balance of FC voltages when designing the control schemes for the FC converters. There are three types of multilevel converter topologies namely, the neutral-point-clamped (NPC) converter, the flying capacitor (FC) converter, and the cascaded converter with separate dc voltage sources (also called H-bridge converter).

The FC converter has attracted a great deal of interest in recent years mainly due to a number of advantageous features. For instance, it seems that the extension of the converter to higher than three levels is possibly easier than the NPC alternative in commercial applications. However, a number of drawbacks need to be further addressed. These include large capacitor banks, additional pre charging circuitry, and in particular voltage imbalance amongst FCs.

Voltage sags are most common power quality issues which occur in a power system. Sag is a decrease to between 0.1 and 0.9 p.u. in RMS value at the power frequency for durations of 0.5 cycles to 1 minute. The voltage magnitude has to be maintained within the limits for proper operation of industrial customers which are sensitive to RMS voltage variations. The sensitive industrial customers like process automation, semiconductor manufacturing are very sensitive to RMS voltage variations. Sag of 70% depth for 6 cycles can trip Variable Speed Drive (VSD) and sag of 60% for 12 cycles can trip (non linear load). This may lead to shutdown of plants or restart, reduced customer satisfaction and huge revenue losses. This explains the need for sag mitigation. The older techniques for sag mitigation are network based which includes, Ferro-resonant transformers, electronic tap changers and motor generator sets. The response of such devices is very sluggish. The need is for devices with sub cycle response.

The control system presented in this paper has a wide range of applicability. It is used in a DVR system to eliminate voltage sags, harmonic voltages, and voltage imbalances within a bandwidth. Unlike other control schemes with a comparable range of applicability, only one controller is needed to cancel out all three disturbances simultaneously, while exhibiting good dynamic performance. On the one hand, a closed-loop controller, which consists of a feedback of the load voltage and the repetitive controller, guarantees zero tracking error in steady state. On the other hand, the applied control strategy for the voltage balancing of the flying capacitors, along with a feed forward term of the grid voltage and a controller for the output voltage of the DVR filter, provides excellent transient response.

This paper is organized as follows. The model of a five-level flying-capacitor DVR is presented in Section II. The complete control-scheme structure is studied in Section III, including the three different control subsystems, namely, the filter output voltage controller, the repetitive control structure for the load voltage, and the flying-capacitor voltage regulator scheme.

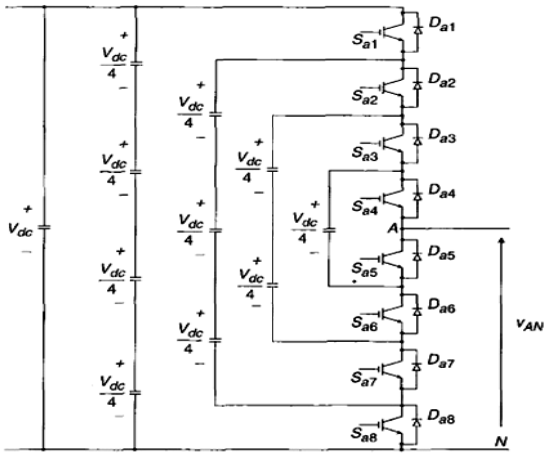

Fig 1: Phase leg of a 5-level flying capacitor multilevel VSC

As well as the modulation method used to operate the multilevel converter. Simulation results obtained by implementing the control system and the five-level flying-capacitor DVR in MATLAB are presented in Section IV. Finally, the main conclusions are given in Section V.

II. DYNAMIC VOLTAGE RESTORER (DVR) SYSTEM CONFIGURATION

A. Five-Level Flying Capacitor

The diodes in the diode-clamped topology can be replaced by clamping capacitors or floating capacitors to clamp the voltages. Such a topology is called flying capacitor multilevel inverter (FCMLI). FCMLI topologies are relatively new compared to the diode-clamped or the cascaded H-bridge cell inverter topologies. Redundancy in the switching states is available by using flying capacitors instead of clamping diodes. This redundancy can be used to regulate the capacitor voltages and obtain the same desired level of voltage at the output. Figure 1 shows a single-phase five-level FCMLI topology. The number of voltage levels at the output can be increased by adding a pair of complementary switches and a capacitor. However, all the capacitors used in such topologies must be rated identically which can prove to be expensive and bulky in size. The major challenge in the flying capacitor multilevel inverter topologies is the voltage regulation across the capacitors. The switching states and the polarity of load current cause the capacitors either to charge or discharge since the current can flow through more than one capacitor. Therefore, the appropriate selection of switching states becomes a priority in FCMLI topologies.

The flying C1 capacitor is charged to Vdc/2, whereas Fig. 1 depicts a phase leg of a five-level Flying capacitor converter. One advantage of the flying capacitor multilevel converter topology is that the extension to converters with more than three levels is easier than in the neutral-point-clamped option. Regarding the five-level topology shown in Fig. 1, the flying capacitors C1 , C2, and C3are charged to 3Vdc/4,Vdc/2 and Vdc/4, respectively. These switching combinations result in different charging or discharging states of the flying capacitors, which provide a degree of freedom for balancing the flying capacitor voltages.

B. Dynamic Voltage Restore(DVR) Connection System

The DVR consists of a five-level flying-capacitor voltage source converter and energy storage which provides the necessary voltage to the dc link. The series connection of the DVR is achieved by means of a coupling transformer. A passive LC filter has been used to filter out the high harmonics generated by the PWM process.

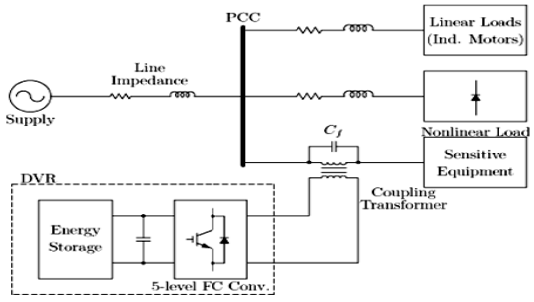

Fig 2: Basic scheme of the system configuration with DVR.

The equivalent circuit for the one-line system is as shown in figure3. Where Vs is the supply voltage, Zs models the line impedance, is the current injected by the supply, which splits at the PCC into the current flowing through the sensitive equipment (this current is divided into the current through the coupling transformer and the current through the filter capacitor), and the current injected into the loads. The voltage is the measured voltage at the PCC, stands for the DVR voltage which has been modelled as an ideal voltage source, the parameters R and L are the resistance and the leakage inductance, respectively, of the coupling transformer Where as is the capacitor used together with the coupling- transformer leakage inductance to filter out the high-frequency harmonics. Finally, and V are the voltages across the filter capacitor and the measured voltage across the sensitive equipment, respectively.

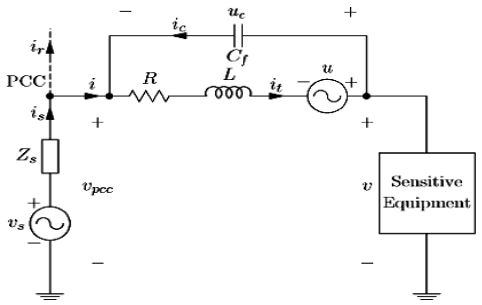

Fig 3: Equivalent circuit for the DVR -connection system.

III. CONTROL STRATEGY OF FILTER OUTPUT VOLTAGE

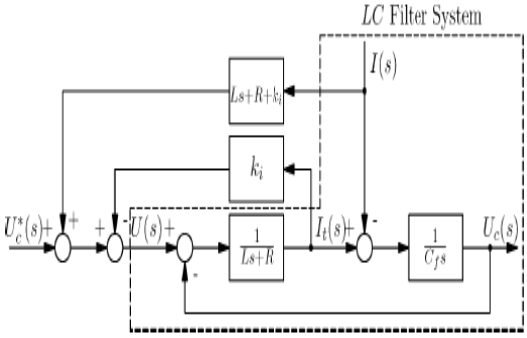

Fig. 4 : Filter output voltage control scheme.

The equation of the sensitive-equipment voltage can be written as

$$v(t) = v_{pcc}(t) + u_c(t) \tag{1}$$

With the following state-variable model for the coupling transformer and the capacitor set:

$$\frac{d}{dt}\begin{bmatrix} i_t(t) \\ u_c(t) \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \frac{-1}{L} \\ \frac{1}{C_f} & 0 \end{bmatrix}\begin{bmatrix} i_t(t) \\ u_c(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{-1}{C_f} \end{bmatrix}\begin{bmatrix} u(t) \\ i(t) \end{bmatrix} \tag{2}$$

Where the state variables are $i_t(t)$ and $u_c(t)$, the control input is $u(t)$ and $i(t)$ is a disturbance input.

- *Flying-Capacitor Voltage Control*

In theory, the phase-shifted PWM method is able to balance the flying-capacitor voltages. Nevertheless, in practical implementations, there may be factors, such as asymmetrical conditions, different characteristics of power switch, etc, that produce voltage imbalances in the flying capacitors. For that reason, a control scheme, which guarantees the balance of the FC voltage, is required. Although there are several research papers which report on FC voltage control, in this paper, the method proposed in has been used because of its simplicity and ease of implementation. Voltage control is based on a closed-loop control scheme which corrects, for each switch, the modulating signal by adding a square-wave in order to increase or decrease the capacitor voltages. In this paper, only a brief description of the method is provided since the algorithm is fully explained.

IV. STUDY CASE AND SIMULATION RESULTS

In order to verify the proposed control algorithm in a five level flying-capacitor DVR, the test system depicted in has been implemented in MATLAB. The test system is comprised of a three-phase voltage source of 11 kV at 50 Hz which feeds a linear load, a nonlinear load, and a sensitive load: the linear load is a three-phase squirrel-cage induction motor of 1350 kW, the nonlinear load consists of an uncontrolled three-phase rectifier with a capacitive filter in the dc side of the rectifier in parallel with an inductive-resistive load. The sensitive load is made up of a 120-kW three-phase squirrel-cage induction motor and an inductive-resistive load of 300 kVA and power factor PF=0.92 . The five-level flying-capacitor converter is connected to the PCC by means of three single-phase coupling transformers of 160 kVA, with unity turns ratio and a star-connected secondary winding. The dc voltage of the multilevel converter is 8 kV. The output filter cut-off frequency was set at $f_c = 2$ kHz with a capacitor $C_f = 0.5uf$. Finally, the value of each flying capacitor is $C_1 = C_2 = C_3 = 250uF$ while the switching frequency was set at $f_{sw} =$ 1650 Hz for each switch. For

the five-level converter studied here (n=5), the effective switching frequency is

$$f_{swT} = (n-1) * f_{sw} = 6600 Hz \quad (3)$$

The main parameters of the test system are summarized in Table I.

TABLE I: PARAMETERS OF THE TEST SYSTEM

Electrical grid	
RMS line-to-line voltage 11 kV	Frequency $f_1 = 50$ Hz
Line parameters	
Resistance $R_s = 60$ mΩ	Inductance $L_s = 3$ mH
Linear load (Induction motor 1)	
Connection inductance $L_1 = 0.5$ μH	
Mechanical power $P_m = 1350$ kW	Rated voltage $V = 11$ kV
Nonlinear load (Rectifier, DC load)	
Connection inductance $L_2 = 0.5$ μH	
Capacitor $C_{dc} = 50$ μF	
Resistance $R_{dc} = 120$ Ω	Inductance $L_{dc} = 0.6$ H
Sensitive Equipment (Resistive-inductive load + Induction motor 2)	
Resistive-inductive load ($S = 300$ kVA)	
Resistance $R_{sl} = 370$ Ω	Inductance $L_{sl} = 0.5$ H
Induction motor 2	
Mechanical power $P_m = 120$ kW	Rated voltage $V = 11$ kV
Coupling transformer (single phase)	
Rated complex power $S = 160$ kVA	
Rated voltage windings $U_{n_1}/U_{n_2} = 8$ kV/8 kV	
Copper loss resistance $R = 0.5$ Ω	Leakage inductance $L = 6$ mH
No-load losses have not been taken into account	
Output filter	
Capacitor $C_f = 1.05$ μF	Cutoff frequency $f_c = 2$ kHz
Flying capacitor converter	
Flying capacitors 250 μF	Single switching freq. 1650 Hz

- *Simulation Results:*

The test system is used to carry out a comprehensive simulation scenario where the multilevel DVR and its control system show their worth. The following sequence of events is assumed to take place:

1) The nonlinear load is connected at time $t = 0$ s and the charging of the flying capacitors also starts at this point in time, a process that is fully completed at time $t = 0.6$ s;

2) At this point, the whole control system is activated and the DVR is connected to the grid together with the inductive-resistive load (sensitive load);

3) In the time period 0.7–1.1 s, induction motor 1 is assumed to be connected with a constant rotor speed of 0.98 p.u.;

4) From $t = 0.8$ s to $t = 1.1$ s, a two-phase-to-ground short-circuit fault is applied at the PCC via a 1.8-resistor;

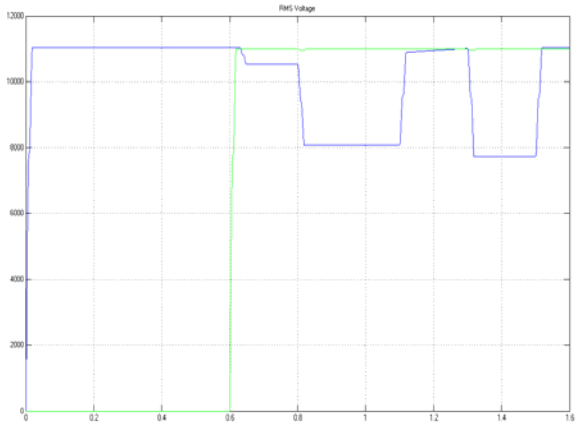

Fig. 5: Three phase rms voltages. (a) green indicates across the sensitive equipment (b)blue indicates at PCC

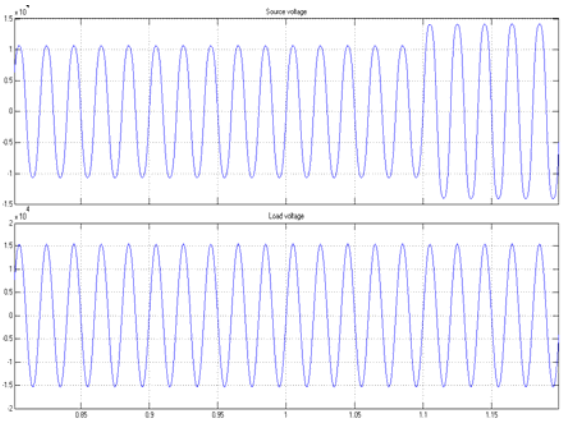

Fig. 6 : Line-to-line voltage at the PCC and across the sensitive equipment.

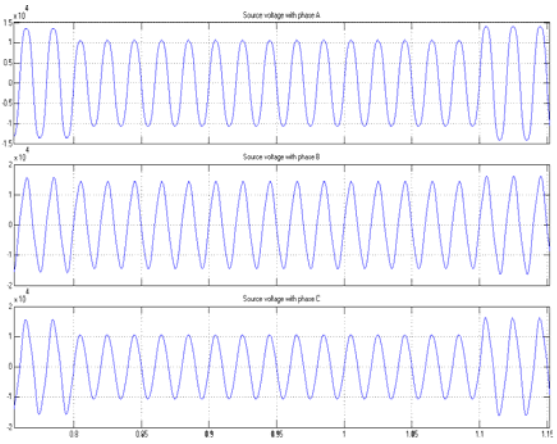

Fig. 7: Line-to-line voltages at the PCC

5) A second induction motor comes into operation right through the fault period, at $t =$ 0.9 s until the end of the simulation time;

6) The nonlinear load is disconnected at $t =$1.3s and, at this point in time, a second short-circuit fault applied at the PCC takes place; this time, there is a three-phase-to-ground fault, with a duration of 200 ms. The total simulation time is 1.6 s.

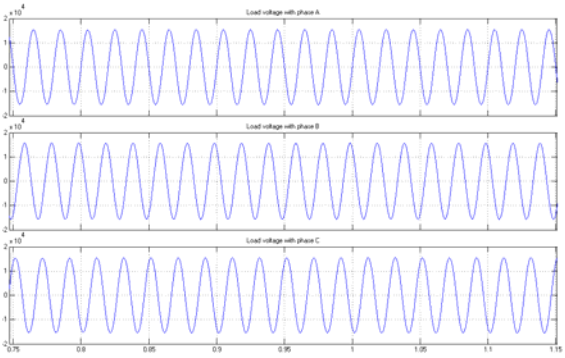

Fig. 8: Line-to-line voltages across the sensitive equipment.

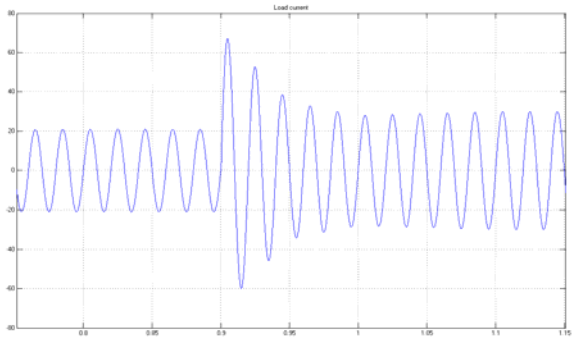

Fig. 9: Line-sensitive-equipment current

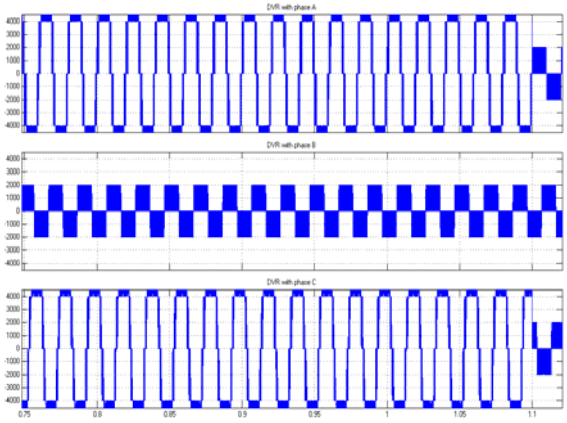

Fig. 10: DVR Multilevel-converter output voltages

The voltage across the sensitive equipment is plotted. The DVR, operated by the control system, compensates the unbalanced voltages with a fast transient response owing to the feed forward term of the sensitive-equipment voltage, while the repetitive control ensures zero-tracking error in steady state. Furthermore, the large current drawn by the induction motor 2 at its connection time $t =$ 0.9 s has no influence in the transient response of the voltage across the sensitive equipment due to the feed forward of the load current (note that only phase A current has been plotted since the sensitive equipment is a three-phase, three-wire system and, hence currents are balanced). The rms values of the fundamental-frequency components are equal to 11 kV for the three line-to-line voltages across the sensitive load.

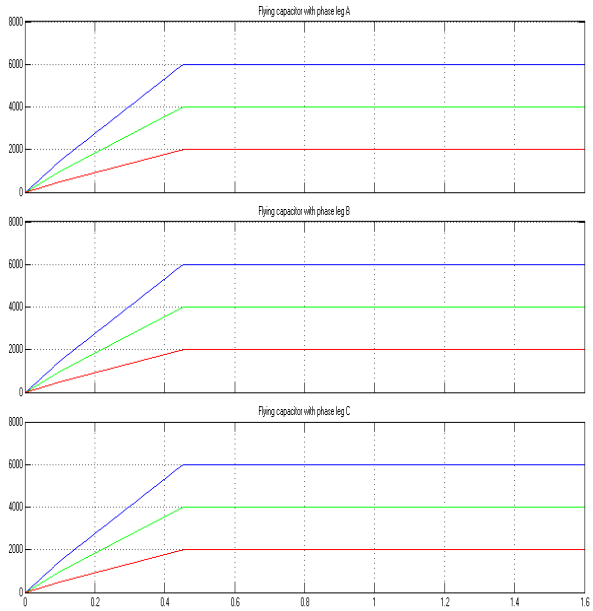

Fig. 11 : Flying-capacitor voltages of three legs in kilovolts

The FC voltage controller keeps constant voltage without significant variations and no voltage imbalances in any of the flying capacitors, regardless of whether there are voltage disturbances at the PCC during the simulation period. As the simulation results show, the dynamic performance of the repetitive control is not impaired by the FC voltage control system. Table II summarizes the main information of the simulation results.

TABLE II: FUNDAMENTAL HARMONIC RMS VALUE AND VOLTAGE TOTAL HARMONIC DISTORTION OF THE LINE-TO-LINE VOLTAGE

AT THE PCC AND ACROSS THE SENSITIVE EQUIPMENT FOR DIFFERENT INSTANTS.

	$V_{rms}^{(1)}$ (kV)	THD_v (%)
Time interval (s): $0 \leq t < 0.6$ (charge of the flying capacitors)		
Time interval (s): $0.6 \leq t < 0.8$ (balanced conditions)		
PCC (ab)	10.52	8.48
Sensitive equipment (ab)	11	1.70
Time interval (s): $0.8 \leq t < 1.1$ (unbalanced conditions)		
PCC (ab)	8.05	6.25
PCC (bc)	9.87	5.13
PCC (ca)	7.52	2.03
Sensitive equipment (ab)	11	0.90
Sensitive equipment (bc)	11	1.02
Sensitive equipment (ca)	11	0.91
Time interval (s): $1.1 \leq t < 1.3$ (balanced conditions)		
PCC (ab)	10.84	8.33
Sensitive equipment (ab)	11	1.70
Time interval (s): $1.3 \leq t < 1.5$ (balanced conditions)		
PCC (ab)	7.7	- -
Sensitive equipment (ab)	11	0.91

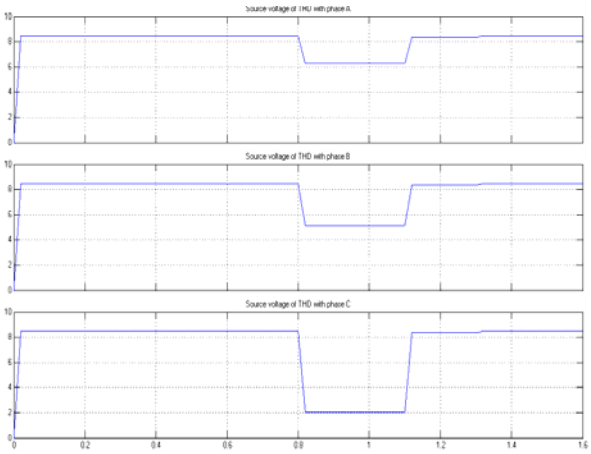

Fig 12: THD across the point of common coupling (PCC)

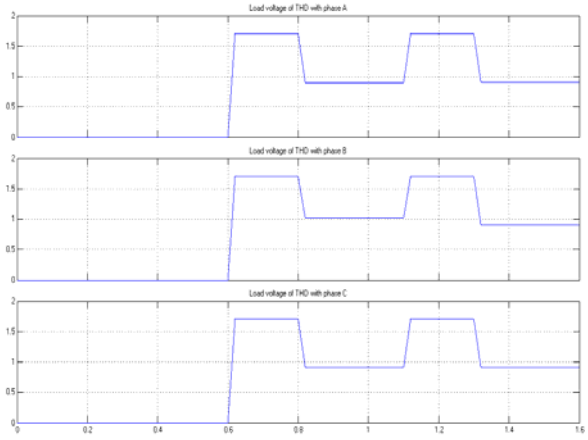

Fig. 13: THD across the sensitive equipment

V. CONCLUSION

In this paper has put forward a DVR based on a five level flying-capacitor multilevel converter scheme. This control structure simultaneously cancels out voltage sags, voltage imbalances, and voltage harmonics other than high-frequency switching harmonics. The control system is split into three subsystems: the first one works to eliminate the resonance peak of the filter used in the converter output voltage; while the second one is the repetitive control, which ensures a fast transient response and zero-tracking error in steady-state for any sinusoidal reference and for any sinusoidal disturbance whose frequencies are an integer multiple of the fundamental frequency. Finally, the third subsystem maintains constant, balanced voltages in the flying capacitors.

The control system, together with the DVR, has been implemented by using the graphical facilities available in MATLAB simulation. Comprehensive simulation results using an MV test system show the DVR's excellent performance and the control system in order to protect sensitive equipment from PQ disturbances.

REFERENCES

[1] Pedro Roncero-Sánchez, Member, IEEE, and Enrique Acha, Senior Member, IEEE

[2] M. H. J. Bollen, Understanding Power Quality Problems: Voltage Sags and Interruptions. Piscataway, NJ: IEEE Press, 2000.

[3] V. Immanuel and G. Yankanchi, "A waveform synthesis technique for voltage sag compensation using dynamic voltage restorer (dvr)," in Proc. IEEE Power Eng. Soc. General Meeting, Jun. 2006, pp. 1–7.

[4] N. G. Hingorani, "Introducing custom power," IEEE Spectr., vol. 32, no. 6, pp. 41–48, Jun. 1995.

[5] Z. Changjiang, A. Arulampalam, and N. Jenkins, "Four-wire dynamic voltage restorer based on a three-dimensional voltage space vector pwm algorithm," IEEE Trans. Power Electron., vol. 18, no. 4, pp.1093–1102, Jul. 2003.

[6] L. Xu and V. G. Agelidis, "Flying capacitor multilevel pwm converter based upfc," Proc. Inst. Elect. Eng., Electr. Power Appl., vol. 149, no.4, pp. 304–310, Jul. 2002.

[7] E. Acha, V. G. Agelidis, O. Anaya, and T. J. E. Miller, Power Electronic Control in Electrical Systems. Oxford, U.K.: Newnes, 2001.

[8] C. Feng, J. Liang, and V. G. Agelidis, “Modified phase-shifted pwm control for flying capacitor multilevel converters,” IEEE Trans. Power Electron., vol. 22, no. 1, pp. 178–185, Jan. 2007.

[9] J. Arrillaga, Y. H. Liu, and N. R.Watson, Flexible Power Transmission. The HVDC Options. Chichester, U.K.: Wiley, 2007.

[10] A. Ghosh and G. Ledwich, Power Quality Enhancement Using Custom Power Devices. Norwell, MA: Kluwer, 2002.

[11] D. Soto and T. C. Green, “A comparison of high-power converter topologies for the implementation of facts controllers,” IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 1072–1080, Oct. 2002.

[12] L. Xu and V. G. Agelidis, “VSC transmission system using flying capacitor multilevel converters and hybrid pwm control,” IEEE Trans. Power Del., vol. 22, no. 1, pp. 693–702, Jan. 2007.

[13] A. Shukla, A. Ghosh, and A. Joshi, “Static shunt and series compensations of an smib system using flying capacitor multilevel inverter,” IEEE Trans. Power Del., vol. 20, no. 4, pp. 2613–2622, Oct. 2005.

[14] P. C. Loh, D. M. Vilathgamuwa, S. K. Tang, and H. L. Long, “Multilevel dynamic voltage restorer,” IEEE Power Electron. Lett., vol. 2, no. 4, pp. 125–130, Dec. 2004.

[15] Z. Yin, M. Han, X. Zhou, and K. Yu, “Project study of dynamic voltage restorer,” in Proc. IEEE Power Eng. Soc. Transm. Distrib. Conf. Exhibit.: Asia and Pacific, 2005, pp. 1–8.

[16] C. Meyer,C. Romaous, and R. W. DeDoncker, “Five level neutral-point clamped inverter for a dynamic voltage restorer,” in Proc. 11th Eur. Conf. Power Electronics and Applications, Dresden, Germany, Sep. 2005, EPE, pp. 1–9.

[17] B.Wang, G. Venkataramanan, and M. Illindala, “Operation and control of a dynamic voltage restorer using transformer coupled h-bridge converters,” IEEE Trans. Power Electron., vol. 21, no. 4, pp. 1053–1060, Jul. 2006.

[18] T. Inoue and M. Nakano, “High accuracy control of a proton synchrotron magnet power supply,” in Proc. Int. Federation of Automatic Control, 8th Triennial World Congr., 1981, vol. XX, IFAC, pp. 216–221.

[19] S. Hara, Y. Yamamoto, T. Omata, and M. Nakano, “Repetitive control system: A new type servo system for periodic exogenous signals,” IEEE Trans. Autom. Control, vol. 33, no. 7, pp. 659–668, Jul. 1988.

[20] K. Zhou and D. Wang, “Digital repetitive controlled three-phase pwm rectifier,” IEEE Trans. Power Electron., vol. 18, no. 1, pp. 309–316, Jan. 2003.

[21] A. García-Cerrada, O. Pinzón-Ardila, V. Feliu-Battle, P. RonceroSánchez, and P. García-González, “Application of a repetitive controller for a three-phase active power filter,” IEEE Trans. Power Electron., vol. 22, no. 1, pp. 237–246, Jan. 2007.

[22] T. J. Summers and R. E. Betz, “Dead-time issues in predictive current control,” IEEE Trans. Ind. Appl., vol. 40, no. 3, pp. 835–844, May/Jun. 2004.

[23] P. Horowitz and W. Hill, The Art of Electronics, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 1989.

[24] Y. Liang and C. O. Nwankpa, “A power-line conditioner based on flying-capacitor multilevel voltage-source converter with phase-shift pwm,” IEEE Trans. Ind. Appl., vol. 36, no. 4, pp. 965–971, Jul./Aug. 2000.

[25] L. Xu and V. G. Agelidis, “Active capacitor voltage control of flying capacitor multilevel converters,” Proc. Inst, Elect. Eng., Electr. Power Appl., vol. 151, no. 3, pp. 313–320, May 2004.

[26] Feng, “Switching frequency reduction in pulse-width modulated multilevel converters and systems,” Ph.D. dissertation, Dept. Electroni.

◈◈◈