International Journal of Smart Sensor and Adhoc Network

Volume 1 | Issue 2 Article 15

October 2011

Design And Implemation Of An Enhanced Dds Based Digital Modulator For Multiple Modulation Schemes

Manoj Kollam
Dept. of E & C,GSSSIETW, Mysore, India, mkollam@gmail.com

Design And Implemation Of An Enhanced Dds Based Digital Modulator For Multiple Modulation Schemes

Manoj Kollam[1], S.A.S.Krishna Chaithanya[2], Nagaraju kommu[3]
Lecturer, Dept. of E & C,GSSSIETW, Mysore, India[1],
Dept. of E & C[2,3] ,VNR VJIET[2,3], Hyderabad, india[2,3]
mkollam@gmail.com

Abstract— This paper deals with the design & implementation of a Digital Modulator based on the FPGA. The design is implemented using the Enhanced Direct Digital Synthesis (DDS) Technology. The basic DDS architecture is enhanced with the minimum hardware to facilitate the complete system level support for different kinds of Modulations with minimal FPGA resources. The size of the ROM look up is reduced by using the mapping logic. The Design meets the present Software Define Radio (SDR) requirements and provides the user selection for desired modulation technique to be used. The VHDL programming language is used for modeling the hardware blocks for powerful and flexible programming and to avoid VHDL code generation tools. The design is simulated in the ModelSim Simulation Tool and Synthesized using the Xilinx ISE Synthesis Tool. The architecture is implemented on the SPARTAN-3A FPGA from Xilinx Family in the SPARTAN-3A evaluation board. The experimental results obtained demonstrate the usefulness of the proposed system in terms of the system resources, its capabilities for design, validation and practical implementation purposes.

Keywords- Field Programmable Gate Array (FPGA), Direct Digital Synthesis (DDS), Software Define Radio (SDR), ModelSim, Xilinx ISE.

I. INTRODUCTION

Modulation is the process of conveying the information over the medium. Digital modulation represents the transfer of the digital bit stream from the transmitter to the receiver(s) via the analogue informational channel (the medium).

During the modulation process the informational signal modifies one or more carrier parameters. Usually, the carrier is a sine wave, defined by amplitude, frequency and phase. Depending on the carrier parameter being changed, there are three basic types of modulation techniques Binary Amplitude Shift Keying (BASK), Binary Frequency Shift Keying (FSK) and Binary Phase Shift Keying (BPSK). All the other known modulation techniques are derived from these three basic types.

The Digital Modulators often require a means to generate sinusoidal waveforms according to strong requirements regarding amplitude, phase or frequency from electronic systems. Both the accuracy and the stability of the generated signals must usually be addressed, particularly when the parameters of interest have to be modified in real time.

The Direct Digital Synthesis (DDS) of signals is a current alternative to classical analog methods based on the use of Phase-Locked Loops providing various advantages [2]. As operations within a DDS device are primarily digital, it can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies.

In this paper, a new Digital Modulator with multiple modulation capabilities has been proposed. The paper mainly focuses on enhancing the existing DDS architecture with minimal hardware elements to provide a single unit solution and for supporting different modulations. It avoids the users to have a modulator for each modulation. The design is made completely using the VHDL programming for avoiding VHDL code generation tools for powerful and flexible programming and synthesized on the SPARTAN-3A FPGA. The Design meets the present Software Define Radio (SDR) requirements and provides the user selection for desired modulation technique to be used.

This paper is organized into 5 sections. In section 1, a brief description of digital modulation technology's present situation and problems are introduced and a new method of designing a Digital Modulator for supporting multiple modulation schemes is proposed. In section 2, DDS Technology, A new method of using the enhanced DDS technology to design digital modulator is proposed. In section 3, the Architecture of the designed Digital Modulator, its construction, operations of various modules used in the architecture are described in detail. In section 4, the analysis of the simulation and synthesis results for the statistical data about the design correctness and the amount of device resource consumption of the design and programming the FPGA device. In the final section, the advantages of using enhanced DDS technology to design digital modulator for multiple modulation techniques have been discussed.

II. DDS TECHNOLOGY

Digital modulator is based on DDS technology and realized on FPGA. Direct digital synthesis (DDS) is a method of producing an analog waveform usually a sine wave, by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. The ability to accurately produce and control waveforms of various frequencies and a profile has become a key requirement common to a number of industries. DDS technique is rapidly gaining acceptance for solving frequency (or waveform) generation requirements in both communications and industrial applications because single-

chip IC devices can generate programmable analog output waveforms simply and with high resolution and accuracy.

Furthermore, the continual improvements in both process technology and design have resulted in cost and power consumption levels that were previously unthinkably low [].

A.DDS Modulation Capabilities

It is simple to add modulation capabilities to the DDS, because the DDS is a digital signal processing device. In the DDS it is possible to modulate numerically all three waveform parameters.

$$S(n) = A(n) \sin(2\pi (\Delta P (n) + P(n)))$$

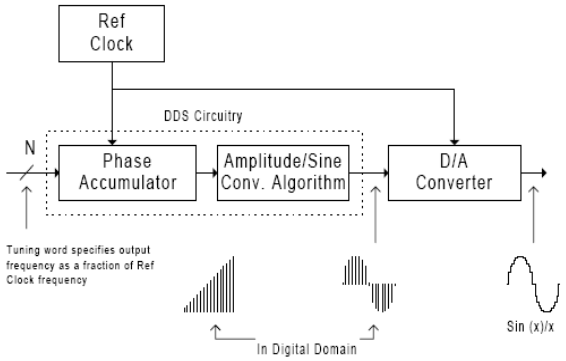
Where A(n) is the amplitude modulation, ΔP (n) is the frequency modulation, and P (n) is the phase modulation. All known modulation techniques use one, two or all three basic modulation types simultaneously. Consequently any known waveform can be synthesized from these three basic types within the Nyquist band limitations in the DDS [1].

B.DDS Operating Principle

The Principle of operation of the DDS can be understood with the Fig.1. The Frequency tuning input is converted into the angular phase by Phase Accumulator and is converted into the sinewave amplitudes by Amplitude/Sine Conv. Algorithm. This is applied to the D/A for analog sinewave output [3].

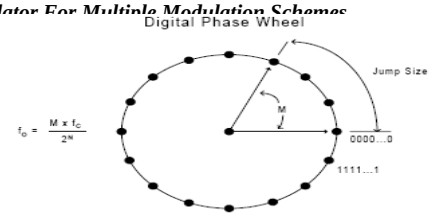
Fig.1: Signal flow through DDS architecture

To understand this basic function, visualize the sine



wave oscillation as a vector rotating around a phase circle as shown in the Fig.2. The number of discrete phase points contained in the wheel is determined by the resolution of the phase accumulator, which determines the tuning resolution of the DDS. Each designated point on the phase wheel corresponds to the equivalent point on a cycle of a sine waveform.

Fig.2: Digital Phase Wheel.



n	NUMBER OF POINTS
8	256
12	4096
16	65536
20	1048576
24	16777216
28	268435456
32	4294967296
48	281474976710656

As the vector rotates around the wheel, a corresponding output sinewave is being generated. One revolution of the vector around the phase wheel, at a constant speed, results in one complete cycle of the output sinewave[3].

The phase accumulator is utilized to provide the equivalent of the vector's linear rotation around the phase wheel. The contents of the phase accumulator correspond to the points on the cycle of the output sinewave. The number of discrete phase points contained in the "wheel" is determined by the resolution, N, of the phase accumulator. The output of the phase accumulator is linear and cannot directly be used to generate a sinewave or any other waveform except a ramp.

Therefore, a phase-to-amplitude lookup table is used to convert a truncated version of the phase accumulator's instantaneous output value into the sinewave amplitude information that is presented to the D/A converter

The relationship between the length of the phase accumulator and output frequency form the basic tuning equation for DDS architecture:

$$FOUT = (M (REFCLK)) /2N$$

Where:

FOUT: Output frequency of the DDS
M: Binary tuning word
REFCLK: Internal reference clock frequency
N: The length in bits of the phase accumulator.

Changes to the value of M in the DDS architecture result in immediate and phase-continuous changes in the output frequency.

C. Algorithm of Rom Compression

In the technology of DDS, the conversion of phase to amplitude is realized by look-up table ROM. Its content is stored in ROM, phase value is the address of ROM and its output is the amplitude of conversion. When the number of phase is big, it is not only increasing quantization error of amplitude, but also the rapid increase of the required hardware [1]. So the algorithm of ROM compression based on the symmetry of sine wave is adopted in the system.

Sine wave of one period is divided into 4 Quarters: [0~π/2], [π/2~π], [π~3π/2], [3π/2~2π] as shown in the Fig.3. Using the symmetrical nature of a sinewave and utilizing the mapping logic to synthesize a complete sinewave cycle

from ¼ cycle of data from the phase accumulator. The phase-to-amplitude lookup table generates all the necessary data by reading forward then back through the lookup table. Fig shows the symmetric nature of the sine wave. This method saves nearly three-fourths resources.

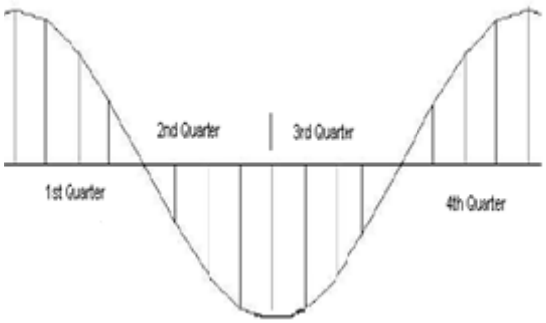


Fig.3: Symmetric Nature of Sine Wave.

III. THE ARCHITECTURE OF DIGITAL MODULATOR

Fig.4: Digital Modulator Architecture

The Digital Modulator architecture is shown in the Fig.4. It consists of Phase Accumulator and Phase-to-Amplitude Converter which are the basic constructs of a DDS and other digital hardware added to support different modulations in the architecture.

The overall functionality of the modulator can be understood with respect to functionality of each element of the design.

The Clock Generator takes the input from the external crystal oscillator from the board and multiplies or divides the clock. Here the It generates two clocks one is (Clock1) System Clock, for the entire operation of the system and supplies all other components with the clock input and the other for the Data buffer, the each bit of the user data is transmitted at high of clock2.

The Resetter supplies all other components with the reset input taking from the external push button on the board.

The Modulation Control Unit is the major part of the architecture which contains the registers to store the Center frequency, Frequency Deviation, Phase Deviation, Center Phase and Amplitude parameters. It supplies the other hardware with these values and sets the control register to facilitate different modulation Techniques.

The Frequency Shifter adds/subtracts the two frequencies i.e. center frequency and frequency deviation to get the mark and space frequencies during FSK. In all other cases it acts as a simple buffer and transmits the data to the successive block.

The Phase Accumulator will keeps on incrementing the instantaneous frequencies with the phase offset to get the instantaneous phase values

The Phase Shifter adds/subtracts the two frequencies i.e. center frequency and frequency deviation to get the mark and space phases during PSK. In all other cases it acts as a simple buffer and transmits the data to the successive block.

The Phase to Amplitude converts these instantaneous values into the sine wave amplitudes for transmission. It is just a look up table containing amplitude values.

The Amplitude Multiplier multiplies the amplitudes stored in internal registers with the sine wave instantaneous amplitudes to get the logic high and low amplitudes during ASK modulation and acts as a buffer in all other cases.

All the blocks of the design can be Enabled/Disabled depending on the control register value for facilitating the selected type of modulation.

To reduce the number of complex additions and multiplications booth's algorithm is used for implementing this module.

A. Booth's Multiplication Procedure

The First step is making the Booth table and the second step is implementing the Booth's Algorithm.

Step 1: Making the Booth table

1. Take two numbers multiplier(X) and multiplicand (Y).
2. From the two numbers, pick the number with the smallest difference between a series of consecutive numbers, and make it a multiplier.
3. Take the 2's complement of Y and call it –Y
4. Load the X value in the table.
5. Load the previous first least significant bit of X for X-1 value
6. Load 0 in U and V rows which will have the product of X and Y at the end of operation.

7. Make the number of rows for each cycle as the number of bits.

Step 2: Booth Algorithm

Booth algorithm requires examination of the multiplier bits, and shifting of the partial product. Prior to the shifting, the multiplicand may be added to partial product, subtracted from the partial product, or left unchanged according to the following rules:

1. Look at the first least significant bits of the multiplier "X", and the previous least significant bits of the multiplier "X - 1".
    a. 0 0 Shift only
    b. 1 1 Shift only.
    c. 0 1 Add Y to U, and shift
    d. 1 0 Subtract Y from U, and shift or add (-Y) to U and shift
2. Take U & V together and shift arithmetic right shift which preserves the sign bit of 2's complement number. Thus a positive number remains positive, and a negative number remains negative.
3. Shift X circular right shifts because this will prevent us from using two registers for the X value.
4. Repeat the same steps until the total cycles are completed.

The advantage of using the booth's algorithm is it reduces the number of complex multiplications and additions from a regular multiplication, which in turn reduces the utilization of number of FPGA resources.

IV. ANALYSIS OF SIMULATION AND SYNTHEIS RESULTS

To verify the design, the overall system is simulated in the ModelSim environment and synthesized in the Xilinx Environment. The modules simulated and synthesized are Modulation Control Unit, Frequency Adder, Clock Generator, Phase Shifter, Phase Accumulator, Phase-to-Amplitude Converter, Amplitude Multiplier, Resetter and the overall system.

The simulation and synthesis results of the digital modulator architectural are shown below with respect to different modulation techniques.

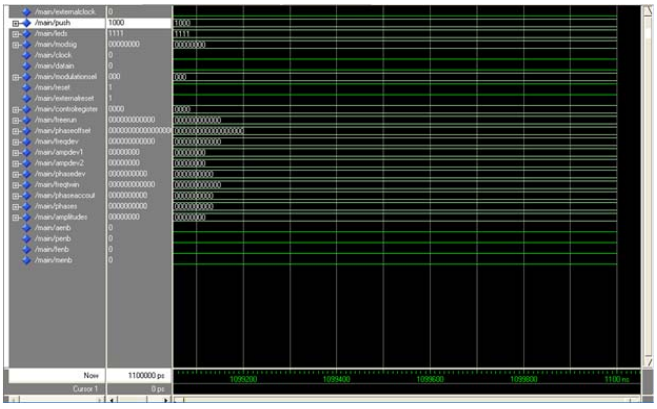


Fig.5: Simulation Result during Reset Condition

The Fig.5 shows the status of all the units in the Digital Modulator design during the reset condition. At this situation all the components are initialized to zero.

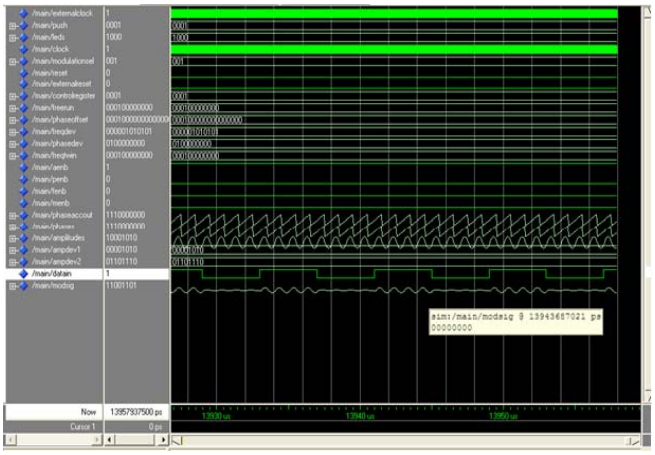


Fig.6: Simulation Result during BASK Condition

During the BASK condition the signal contains two amplitudes depending upon the data input. This is shown in the Fig.6. The simulation result contains the status of different components and signals during ASK condition.

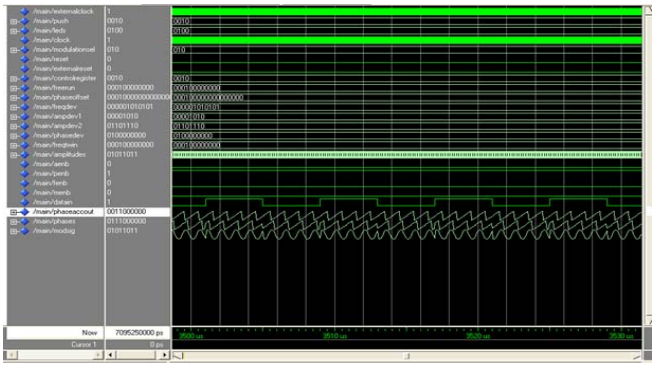


Fig.7: Simulation Result during BPSK Condition

During the BPSK condition the signal contains two phases depending upon the data input. This is shown in the Fig.7. The simulation result contains the status of different components and signals during BPSK condition.

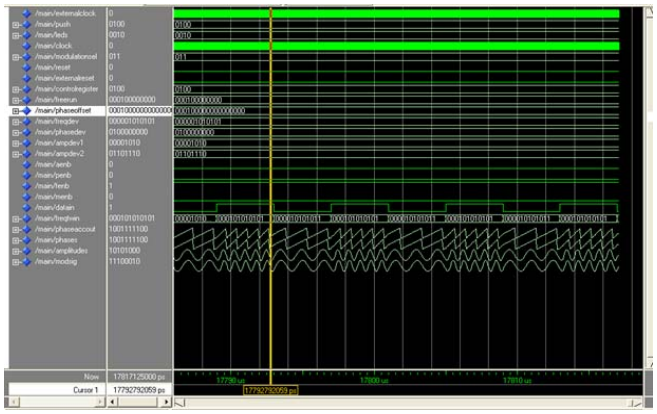


Fig.8: Simulation Result during BFSK Condition

During the BFSK condition the signal contains two frequencies depending upon the data input. This is shown in the Fig.8. The simulation result contains the status of different components and signals during BFSK condition.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	72	7,168	1%	
Number of 4 input LUTs	1,217	7,168	16%	
Logic Distribution				
Number of occupied Slices	682	3,584	19%	
Number of Slices containing only related logic	682	682	100%	
Number of Slices containing unrelated logic	0	682	0%	
Total Number of 4 input LUTs	1,282	7,168	17%	
Number used as logic	1,217			

Fig.9: Device Utilization Summary

In the Device Utilization Summary, we can see the number of flip flops, I/Os and BUFGMUX utilized in the design. This is shown in the Fig.9.

A. Programming the Design into SPI Flash Memory of SPARTAN-3A FPGA Evaluation kit

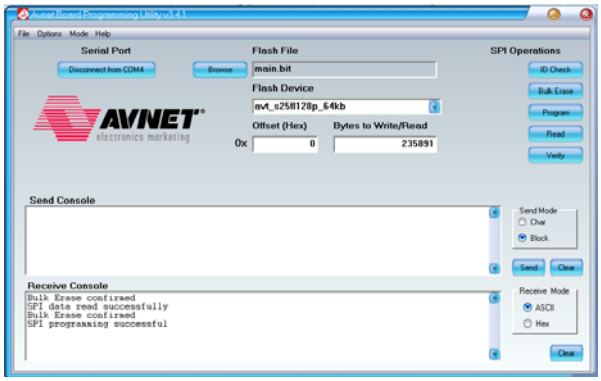


Fig.10: Receive Console showing the SPI Programming Successful.

The Spartan-3A Evaluation board from Avnet is used for implementing the Design because of its low cost. It contains a 128 Mbits of SPI Flash memory that can be used to store a FPGA bit file. With the SPI memory programmed, that FPGA will configure itself on power-up, when the MODE jumpers are set for Master SPI mode[7].

The Fig.10 shows the Receive console showing the SPI Programming Successful.

V. CONCLUSIONS

In this paper, the Enhanced DDS based Digital Modulator is designed using VHDL. The design shows the Digital Modulator architecture is developed with the enhanced DDS architecture and provides more modulation capabilities with the utilization of less hardware resources. The design provides single unit solution for different Modulation Techniques, with the user choice of Modulation type to be used. Presently, the modulations implemented are BASK, BPSK, BFSK.

The simulation results show that the design principles are correct and effective. After synthesizing the system we got the statistical data about the number of input-output buffers, the number of registers, number of flip-flops and latches used in the usage of FPGA tool. These results show that the utilization of the device resources is quite minimal. The final bit file is programmed into the Xilinx XC3S400A FPGA device.

ACKNOWLEDGEMENTS

It is a pleasure to recognize the many individual who have helped me in completing this technical paper. I sincerely express heartiest thanks to my guide Mrs V.Padmaja for all the technical guidance, encouragement and support throughout this process.

REFERENCES

[1] Natural Science Foundation of Jiangxi Province of China with Grand 2008GZS0028,"Design and Implement of Digital Modulator Based on Improved DDS Technology and DSP Builder".

[2] "FPGA-Based Design, Implementation, and Evaluation of Digital Sinusoidal Generators", 2008 IEEE.

[3] Analog Devices, A technical tutorial on digital signal synthesis, 1999.
[4] Wang Meng,Wang Ning(2006). "The Implementation of DDS with FPGA by Less Resources Used" .Microelectronics And Computer,Vol.23, No.8, pp.181-183.
[5] Digital frequency synthesis demystified / Bar-Giora Goldberg, 1999.
[6] Digital modulation techniques / Fuqin Xiong,2000.
[7] Xilinx Spartan-3A Evaluation Kit User Guide,Rev 2.1.