Proceeding of International Conference on Advances in Electrical & Electronics Engineering AEEE-2012

Dr. Srikanta Patnaik

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Editorial

In the emerging knowledge era, the native knowledge has to be preserved and enhanced with latest tools of technology, training and research. The villages have to have access to good education from best teachers wherever they are, must have the benefit of good medical treatment, and must have latest information on their pursuits like agriculture, fishery, horticulture and food processing. That means they have to have Electronic connectivity. Today, about 800 million in India are living in villages, and hence any mission towards prosperity has to be inclusive of the rural regions. As a logical step, we have to address, how the sustainable development of villages can be achieved. The development of six hundred thousand villages is vital for developed India. Only Innovations and research in the field of engineering and technology is the solution for the sustainable growth.

In the 21st century Electrical Engineering & Electronics Engineering has acquired a path breaking trend by making a swift in a number of cross functional disciplines like Bio-Science, Health Science, Atomic Engineering, Agricultural Science, and Artificial Intelligence. Still there remains a substantial relativity in both the disciplines which underscores further extension of existing literature to augment the socio-economic relevancy of these two fields of study. Over the years during the 20th century every branch of Engineering and Applied Sciences has been enriched and developed through continuous efforts, cultivation and contribution by academicians and researchers. Through the passage of time many new areas emerged and developed to cater the needs of modern technological advancements.

Let me highlight some of recent development on Electronics & Electrical engineering. University of Maryland Chemistry Professor John Fourkas and his research group have developed new materials and nanofabrication techniques for building miniaturized versions of components needed for medical diagnostics, sensors and other applications. A new design reduces the areal footprint of nanowire transistors by a factor of two. Xiang Li at the A*STAR Institute of Microelectronics and co-workers have now integrated two transistors onto a single vertical silicon nanowire, pushing the areal density limit of nanowire transistors even further.

The conference designed to stimulate the young minds including Research Scholars, Academicians, and Practitioners to contribute their ideas, thoughts and nobility in these disciplines of engineering. It’s my pleasure to welcome all the participants, delegates and organizer to this international conference on behalf of IRNet family members. We received a great response from all parts of country and abroad for the presentation and publication in the proceeding of the conference. I sincerely thank all the authors for their invaluable contribution to this conference. I am indebted towards the reviewers and Board of Editors for their generous gifts of time, energy and effort.

Editor-in-Chief
Dr. Srikanta Patnaik
Chairman, I.I.M.T., Bhubaneswar
Interscience Campus, At/Po.: Kantabada, Via-Janla, Dist-Khurda
Bhubaneswar, Pin:752054. Orissa, INDIA.
Sliding Mode Current Controller For Transformer Less DC–DC Converter With High Step-Up Voltage Gain

G. Ramanjaneyulu & M. Subbarao
EEE Dept., Vignan University, Vadlamudi, Viatenali, Narakoduru Guntur
g.ramanjaneyulu@gmail.com, g.ramanjaneyulu@hotmail.com, Subbu.mopidevi@gmail.com

Abstract - Conventional dc-dc boost converters are unable to provide high step-up voltage gains due to the effect of power switches, rectifier diodes, and the equivalent series resistance of inductors and capacitors. In this proposed converter, two inductors with same level of inductance are charged in parallel during the switch-on period and are discharged in series during the switch-off period. The structures of the proposed converter and controller are very simple. Finally, comparative results are presented for 12v/100v transformer less dc-dc converter. Moreover, the steady-state analyses of voltage gains and boundary operating conditions are discussed in detail. The proposed work is carried by using matlab/simulink software.

Index Terms—DC–DC boost converter, high step-up voltage gain, power stage, Sliding Mode Control.

I. INTRODUCTION

The DC-DC converter with high step up gain is used for many applications, such as high-intensity-discharge (HID) lamp ballast for automobile headlamps, fuel-cell energy conversion systems, solar-cell energy conversion systems and the battery back-up system for uninterruptible power supplies. Theoretically, the DC-DC boost converter can achieve high step-up voltage gain with an extremely high duty ratio. However, in practice, the step-up voltage gain is limited due to the effect of power switches, rectifier diodes and the equivalent series resistance (ESR) of inductors and capacitors. Also, the extremely high duty-ratio operation will result in serious reverse-recovery problem. Many topologies have been presented to provide high step-up voltage gain without an extremely high duty ratio. The DC-DC fly back converter is a very simple structure with high step-up voltage gain and electrical isolation, but the active switch of this converter will suffer high voltage stress due to the leakage inductance of the transformer. For recycling the energy of the leakage inductance and minimizing the voltage stress on the active switch, some energy-regeneration techniques have proposed to clamp the voltage stress on the active switch and to recycle the leakage-inductance energy. The coupled-inductor techniques provide solutions to achieve high voltage gain, low voltage stress on the active switch and high efficiency without the penalty of high duty ratio. The transformer less DC-DC converters, which include the cascade boost type, the quadratic boost type, the voltage-lift type, the capacitor-diode voltage multiplier type and the boost type integrating with switched-capacitor technique. However, these types are all complex and higher cost. For getting higher step-up voltage gain, the other DC-DC converters are also presented. Compared with the converter as shown in fig.1, proposed converter has the following merits: (i) two power devices exist in the current-flow path during the switch-on period, and one power device exists in the current-flow path during the switch-off period. (ii) The voltage stresses on the active switches are less than the output voltage. (iii) Under the same operating conditions, including input voltage, output voltage, and output power, the current stress on the proposed DC-DC converters fig.2 utilize the switched-inductor technique, which two inductors with same level of inductance are charged in parallel during the switch-on period and are discharged in series during the switch-off period, to achieve high step-up voltage gain without the extremely high duty ratio. The operating principles and steady-state analysis are discussed in the following sections. To analyze the steady-state characteristics of the proposed converters, some conditions are assumed as: (1) All components are ideal. The on-state resistance $R_{DS(ON)}$ of the active switches, the forward voltage drop of the diodes and the ESRs of the inductors and capacitors are ignored. (2) All capacitors are sufficiently large and the voltages across the capacitors can be treated as constant. The modified boost type with switched-inductor technique is shown in fig.1.
II. PROPOSED CONVERTER

A transformer less DC-DC high step-up converter is proposed as shown in figure 2, which consists of two active switches (Sw1 and Sw2), two inductors (L_a and L_b) that have the same level of inductance, one output diode Do, and one output capacitor Co. Switches S1 and S2 are controlled simultaneously by using one control signal. Figure 2(d) and 2(e) shows some typical waveforms obtained during continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The operating principles and steady-state analysis of CCM and DCM are presented in detail as follows.

2.1 CCM Operation:

The operating modes can be divided into two modes, defined as modes 1 and 2.

Mode 1 [t0, t1]:

During this time interval, switches Sw1 and Sw2 are turned on. The equivalent circuit is shown in figure 2(a). Inductors L1 and L2 are charged in parallel from the DC Source and the energy stored in output capacitor C0 is released to the load. Thus, the voltages across L_a and L_b are given as:

\[ V_{L_a} = V_{L_b} = V_d \]  

(1)

Mode 2 [t1, t2]:

During this time interval, Sw1 and Sw2 are turned off. The equivalent circuit is shown in Fig. 2(b). The DC source, L_a and L_b are series-connected to transfer the energies to Co and the load. Thus, the voltages across L_a and L_b are derived as:

\[ V_{L_a} = V_{L_b} = \left( \frac{V_d - V_o}{2} \right) \]  

(2)

By using the volt-second balance principle on L_a and L_b, the following equation can be obtained:

\[ \int_0^{DT} V_i \, dt + \int_T^{2T} \left( \frac{V_d - V_o}{2} \right) \, dt = 0 \]  

(3)

Simplifying (3), the voltage gain is given by
\[ M_{ccm} = \left( \frac{V_o}{V_d} \right) = \left( \frac{1 + D}{1 - D} \right) \]  

(4)

From figure 2(d), the voltage stresses on \( S_{sw1}, S_{sw2}, \) and \( D_0 \) are derived as

\[ V_{sw1} = V_{sw2} = \left( \frac{V_o + V_d}{2} \right) \]

(5)

\[ V_{DO} = V_o + V_d \]

2.2 DCM Operation:

The operating modes can be divided into three modes, defined as modes 1, 2, and 3.

Mode 1 \([t_0, t_1]\): During this time interval, \( S_{sw1} \) and \( S_{sw2} \) are turned on. The equivalent circuit is shown in fig. 2(a). The two peak currents of \( L_a \) and \( L_b \) can be found as

\[ I_{La} = I_{Lb} = \frac{V_d}{2} D T_s \]

(6)

where \( L \) is the inductance of \( L_1 \) and \( L_2 \).

Mode 2 \([t_1, t_2]\): During this time interval, \( S_{sw1} \) and \( S_{sw2} \) are turned off. The equivalent circuit is shown in Figure 2(b). The DC source, \( L_a \) and \( L_b \) are series-connected to transfer the energies to \( C_0 \) and the load. Inductor currents \( i_{La} \) and \( i_{Lb} \) are decreased to zero at \( t = t_2 \). Another expression of \( I_{La} \) and \( I_{Lb} \) is given as

\[ I_{La} = I_{Lb} = \left( \frac{V_o - V_d}{2} \right) D \frac{T_s}{2} \]

(7)

Mode 3 \([t_2, t_3]\): During this time interval, \( S_{sw1} \) and \( S_{sw2} \) are still turned off. The equivalent circuit is shown in Fig. 2(c). The energies stored in \( L_a \) and \( L_b \) are zero. Thus, only the energy stored in \( C_0 \) is discharged to the load.

From (6) and (7), \( D_2 \) is derived as follows:

\[ D_2 = \left( \frac{2D V_d}{V_o - V_d} \right) \]

(8)

From Figure 2(e), the average value of output-capacitor current during each switching period is given by

\[ I_{co} = \left( \frac{\frac{1}{2} D.T_s I_{La} - I_s T_s}{T_s} \right) \]

(9)

Substituting (6) and (8) into (9), \( I_{co} \) is derived as

\[ I_{co} = \left( \frac{D^2 V_o T_s}{2 L (V_o - V_d)} \right) - \frac{V_o}{R} \]

(10)

Since \( I_{co} \) equals zero under steady state, equation (10) can be re-written as follows

\[ \frac{D^2 V_o T_s}{2 L (V_o - V_d)} = \frac{V_o}{R} \]

(11)

Then, the normalized inductor time constant is defined as

\[ \Gamma_L = \left( \frac{L f_s}{R} \right) \]

(12)

where \( f_s \) is the switching frequency (\( f_s = 1/T_s \)).

Substituting (12) into (11), the voltage gain is given by

\[ M_{DCM} = \left( \frac{V_o}{V_d} \right) = \left( \frac{1}{4} + \frac{D^2}{\Gamma_L} \right) \]

(13)

Typical waveforms for proposed converter I
2.3 Boundary Operating Condition between CCM and DCM

If proposed converter I is operated in boundary conduction mode (BCM), the voltage gain of CCM operation equals the voltage gain of DCM operation. From (4) and (13), the boundary normalized inductor time constant $\tau_{LB}$ can be derived as follows:

$$\Gamma_{LB} = \frac{D (1 - D)^2}{2(1 + D)}$$

(14)

![Figure 2(e) DCM operation.](image)

The curve of $\tau_{LB}$ is plotted in Figure 2(f). If $\tau_{L}$ is larger than $\tau_{LB}$, proposed converter I is operated in CCM.

III. SLIDING MODE CURRENT CONTROLLER:

VSS are systems whose physical structure is changed intentionally during the time in accordance with a preset structure control law. The instants at which the changing of the structure occur are determined by the current state of the system. From this point of view, switch-mode power supplies represent a particular class of VSS, since their structure is periodically changed by the action of controlled switches and diodes. During the control process, the structure of the control system varies from one structure to another thus earning the name variable structure control (VSC).

VSC is a high-speed switching feedback control resulting in a sliding mode. For example, the gains in each feedback path switch between two values according to a rule that depends on the value of the state at each instant. The purpose of the switching control law is to drive the nonlinear plant’s states trajectory on this surface for all subsequent time. This surface is called Switching Surface. When the plants state trajectory is “above” the surface, feedback path has one gain and a different gain if the trajectory drops “below” the surface. This surface defines the proper rule for switching. The surface is also called Sliding Surface because, ideally speaking, once intercepted, the switching control maintains the plant’s state trajectory on the surface for all subsequent time and the plant’s state trajectory along this surface. The plant dynamics restricted to this surface represent the controlled system behavior.

A VSC control design breaks into two phases.

The first phase is to design or choose a switching surface so that the plant state trajectory restricted to the surface has desired dynamics.

The second phase is to design a switched control that will drive the plant state to the switching surface and maintain into on the surface upon interception.

A lyapunov approach is used to characterize this second design phase. Here a generalized Lyapunov function, that characterizes the motion of the state trajectory to the surface, is defined in terms of the surface. For each chosen switched control structure, one chooses the “gains” so that the derivative of this lyapunov function is negative definite, thus guaranteeing motion of the state trajectory to the surface. To emphasize the important role of the Sliding mode, the control is also called Sliding mode control. It should be noted that a variable structure control system can be devised without a sliding mode, but such system does not possess the associated merits.


Let us consider now a class of systems with a state model nonlinear in the state vector $x(.)$ and linear in the control vector $u(.)$ in the form

$$x(t) \in R^n$$

(15)
Where \( x(t) \in \mathbb{R}^m \), and \( B(x,t) \in \mathbb{R}^{m \times m} \); further, each entry in \( f(x,t) \) and \( B(x,t) \) is assumed continuous with a bounded continuous derivative with respect to \( x \).

The first phase is to design or choose a switch surface so that the plant state trajectory restricted to the surface has desired dynamics. According to the Sliding mode control theory [17], all state variables are sensed, and the states are multiplied by proper gains \( K_i \) and added together to form the sliding function \( \sigma(x,t) \). Then, hysteretic block maintains this function to zero, so that we can define sliding surface as:

\[
\sigma(x,t) = \sum_{i=1}^{N} K_i x_i = 0
\]  

(16)

Where \( N \) is the system order (number of state variables).

For second order systems

\[
\sigma = x_1 + \tau x_2
\]  

(17)

Which is a linear combination of the two state variables. In the phase plane, equation \( \sigma = 0 \) represents a line, called sliding line, passing through the origin (which is the final equilibrium point for the system).

We now define the following control strategy

If \( \sigma > +\beta \Rightarrow u = 0 \) \hspace{1cm} (18)

If \( \sigma > -\beta \Rightarrow u = 1 \)

Where \( \beta \) defines a suitable hysteresis band. In this way, the phase plane is divided in two regions separated by the sliding line, each associated to one of the two sub topologies defined by switch status \( u \). When the system status is in \( P \), since we are in the region \( \sigma < -\beta \), the switch is closed and the motion occurs along a phase trajectory corresponding to \( u = 1 \). When the system status crosses the line \( \sigma = +\beta \), according to (18), \( u = 0 \) and the system status follows a phase trajectory corresponding to \( u = 1 \). Observing that the phase trajectories, in proximity of the sliding line, are directed toward the line itself, the resulting motion is made by continuous commutations around the sliding line, so that the system status is driven to the final equilibrium point.

Fig.3 Sliding surface

From this example, in the hypothesis of a suitable small value of \( \beta \), two important conclusions arise.

When the system is in the sliding mode, its evolution is independent of the circuit parameters. It depends only on the sliding line chosen. In the example shown in Fig.3 the dynamic is of the first order with a time constant equal to \( \tau \).

If \( N \) is the order of the original system, the dynamic of the controlled system in sliding mode has order \( N-1 \), since the state variables are constrained by the equation \( \sigma = 0 \).

Note that the switching frequency is determined by the amplitude of the hysteresis band \( \beta \). The potentialities of this control technique in the application to switch to switch-mode power supplies are now evident: it exploits the intrinsic non-linear nature of these converters and it is able to provide dynamic behaviors that are different from that of the substructures composing the system, and correspond to that of a reduced system.

3.1 Switching surface design

In the simple case of the second-order systems considered in the previous section, sliding mode control design requires only selection of parameter \( \tau \). Selection, must be done in order to ensure the following three constraints

The hitting condition, which requires that the system trajectories cross the sliding line irrespective of their starting point in the phase plane;

The existence condition, which requires that the system trajectories near the sliding line (in both regions) are directed toward the line itself;

The stability condition of the system motion on the sliding line (i.e. the motion must be toward the equilibrium point).
3.2 Existence Condition:

The existence condition requires that the phase trajectories are directed toward the sliding surface in a small volume around the surface itself. It is achieved by defining the appropriate Lyapunov function $V(x,t,\sigma)$. For signal input systems it is ordinarily convenient to choose a Lyapunov function of the form $V(x,t,\sigma) = 0.5\sigma^2(x)$. To determine the gains necessary to drive the system state to the surface $\sigma(t) = 0$, they may be choose so that

$$\dot{V}(x,t,\sigma) = 0.5 \frac{d\sigma^2}{dt} = \sigma(x) \frac{d\sigma(x)}{dt} = \sigma \cdot \dot{\sigma} < 0 \quad (19)$$

Thus sliding mode does exist on a discontinuity surface whenever the distances to this surface and the velocity of its change $\dot{\sigma}$ are of opposite signs, i.e. when

$$\lim_{x \to +0} \sigma > 0 \quad \text{and} \quad \lim_{x \to -0} \sigma < 0$$

3.3 Stability Condition

Switching surface design is predicted upon knowledge of the system behavior in a sliding mode. This behavior depends on the parameters of the switching surface. In any case, achieving a switching-surface design requires analytically specifying the motion of the state trajectory in a sliding mode. The so called method of equivalent control is essential to this specification.

3.4 Equivalent Control:

Equivalent control constitute an equivalent input which, when exciting the system, produces the motion of the system on the sliding surface whenever the initial state is on the surface. Suppose at $t_1$ the plant’s state trajectory intercepts the switching surface, and a sliding mode exists. The existence of a sliding mode implies that, for all $t \geq t_1$, $\sigma(x(t),t) = 0$, and hence $\sigma(x(t),t) = 0$. Using the chain rule, we define the equivalent control $u_{eq}$ for system of the form eq.3.70 as the input satisfying

$$\sigma = \frac{\partial \sigma}{\partial t} + \frac{\partial \sigma}{\partial x} x + \frac{\partial \sigma}{\partial t} f(x,t) + \frac{\partial \sigma}{\partial x} B(x,t)u_{eq} = 0 \quad (20)$$

Assume that the matrix product $\frac{\partial \sigma}{\partial x} B(x,t)$ is nonsingular for all $t$ and $x$, and one can compute $u_{eq}$ as

$$u_{eq} = - \left[ \frac{\partial \sigma}{\partial t} B(x,t) \right]^{-1} \left( \frac{\partial \sigma}{\partial t} f(x,t) + \frac{\partial \sigma}{\partial x} B(x,t) \right) \quad (21)$$

Therefore, given that $\sigma(x(t),t) = 0$, then for all $t \geq t_1$, the dynamics of the system on the switching surface will satisfy

$$x(t) = \left[ I - B(x,t) \left[ \frac{\partial \sigma}{\partial x} B(x,t) \right]^{-1} \frac{\partial \sigma}{\partial x} \right] f(x,t) - B(x,t) \frac{\partial \sigma}{\partial x} B(x,t) \frac{\sigma}{\partial t} \quad \sigma(t) = \sum_{1}^{N} K_i x_i + r(t) = 0 \quad (22)$$

This equation represents the equivalent system dynamics on the sliding surface. The driving term is present when some form of tracking or regulation is required of the controlled system, e.g. when

$$\sigma(x,t) = \sum_{1}^{N} K_i x_i + r(t) = 0 \quad (23)$$

With $r(t)$ serving as a “reference” signal.

3.5 Physical Meaning of the Equivalent Control

A real control always includes a slow component to which a high rate component maybe added. So decompose the control structure as

$$u(x,t) = u_{eq}(x,t) + u_N(x,t) \quad (24)$$

Where $u_{eq}$ is only valid on the sliding surface and $u_N$ assures the existence of a sliding mode. And $u_N$ is defined as

$$u_N(x,t) = \text{sgn}(\sigma) \quad (25)$$

Where

$$\text{sgn}(\sigma) = \frac{\sigma}{|\sigma|}$$

Since a control plant is a dynamic object, its behavior is largely determined by the slow component while its response to the high rate component is negligible. On the other hand, the equivalent control method demands a substitution of the real control in the motion with a continuous function $u_{eq}(x,t)$, which does not contain any high rate component. The equivalent control equals the slow component of the real control i.e. average control value and may be measured by a first order linear filter provided its time constant is small enough as compared with the slow component, yet large enough to filter out the high rate component and approximately matched with the boundary layer width.
A sliding mode current control (SMC) enables CCM operated rectifiers to be controlled using a much simpler controller.

IV. SIMULATION RESULTS:

SLIDING MODE CURRENT CONTROLLER transformer less dc–dc converters with high step-up voltage gain has been simulated using MATLAB/Simulink. The proposed converter components are selected as $V_{in} = 12$ V, $V_o = 60 - 100$ V, $f_s = 100$ kHz, $P_o = 40$ W, $L_1 = L_2 = 100$ μH, and $C_o = 68$ μF. The simulation diagram of proposed controller is shown in figure 4 and figure 4(a). Simulation results are shown in fig. 5, fig. 6, and fig 6(a).

Fig 4. Simulation diagram of SMC Controller For Transformer Less DC–DC Converter With High Step-Up Voltage Gain

Fig 4(a). Simulation diagram of SMC

Fig 5. Output voltage, output current and output power when load is changes from 40W to 5W at $t=0.5$Sec

Fig 6. Output current when load is changes from 40W to 5W at $t=0.5$Sec
V. CONCLUSION

A sliding mode current control technique has been presented which enables simple, low cost. The technique possesses an inherently stable current loop, and the outer voltage loop is designed in a fashion similar to the other current mode control techniques. This paper has studied SMC controller for transformerless dc–dc converter with high step-up voltage gain. Since the voltage stresses on the active switches are low, active switches with low voltage ratings and low ON-state resistance levels \( R_{\text{ON}} \) can be selected. The steady-state analyses of the voltage gain and the boundary operating condition are discussed in detail. Finally the controller concept was generalized to include average current mode controller. In this case the sensed signal was a filtered version of the inductor current. In SMC controller multiplier present in conventional current mode controller is eliminated as a result of making profitable use of the inherent duty cycle dependent modulator gain. by using the SMC better transient transient responses will come compare to the other current mode controllers.

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International Conference on Advances in Electrical and Electronics Engineering (AEEE), ISBN : 978-93-81693-69-8, 22nd July 2012, Vijayawada 8
Optimum Power Allocation and Bit Loading
for Wireless Communication System

Shaikh Sanobar Naaz Mohd. Amin. & Suman P. Wadkar
Electronics Department, P.I.I.T Engineering College, New Panvel, Navi Mumbai, India
E-mail : sanobarshaikh1712@gmail.com, sp_wadkr@yahoo.com

Abstract – This paper introduces a joint bit loading and power allocation algorithm for system combining bit interleaved coded modulation (BICM) with multi-carrier transmission systems (like OFDM) for efficient Peak to Average power ratio reduction and optimum Bit Error Rate performance. The proposed algorithm in this paper maximizes the mutual information which can be regarded as generalization of mercury/water filling policy that incorporates bit loading and power allocation.

We consider the problem of optimizing the BICM – OFDM system transmitter based on channel information feedback from the receiver side and the problem of bit loading, power allocation, code rate selection for BER minimization and maximization of mutual information is addressed. The followed approach relies on irregular modulation and power to cast problem. This allows deriving the optimum solution without resorting to greedy algorithms.

In this paper the bit loading has been previously determined and then power allocation is done by using mercury/water filling policy (MWF) which leads to maximization of mutual information.

Keywords - Content-based image retrieval (CBIR), human–machine interaction, interactive genetic algorithm (IGA), HSV color space Edge orientation, Micro-structure, Micro-structure descriptor, low-level descriptors.

I. INTRODUCTION

After more than 30 years of research and developments carried out in different places orthogonal frequency division multiplexing (OFDM) has been widely implemented in high speed digital communications. In the conventional serial data transmission system, the information symbols are transmitted sequentially, where each symbol occupy the entire available spectrum bandwidth. But in OFDM system, the information is converted to N parallel sub carriers and sends at lower rates using frequency division multiplexing. The sub carrier frequency spacing is selected such that each sub carrier is located on the other sub carriers zero crossing points. This implies that there is overlapping among the subcarriers but will not interfere with each other. This means that all subcarriers are orthogonal. The OFDM has many advantages such as high bandwidth efficiencies, Robustness to the selective fading problem, use of small guard interval, and its ability to combat the ISI problem.

This paper deals with transmission schemes for BICM-OFDM systems subject to slow fading [1]. The combination of BICM [2] with OFDM [3] provides the low complexity nearly optimal performance approach to broadband transmission in multi path scenarios. On one hand, the paradigm of channel code and modulation separation by means of bit interleaver introduce by BICM has been proved a versatile approach to spectrally efficient transmission in fading channels. BICM allows a large flexibility in constellation selection and channel coding design at the expense of minor performance loses. On the other hand, the use of OFDM allows to get rid of inter symbol interference converting the frequency selective channel in to a set of parallel non interfering channels, thanks to the use multicarrier transmission [1]. The good performance versus complexity trade off provided by BICM – OFDM has motivated a broad interest in this transmission schemes.

In low- mobility areas where the channel state can be accurately tracked by both the transmitter and the receiver and the performance can be improved adapting the signaling to the instantaneous channel spectral shape. By using the BICM-OFDM scheme, optimal performance can be achieved by bit loading and power allocation, i.e. assigning a different constellation (number of bits) and different power to each subcarrier and each channel access according to the channel
frequency response [1]. The most well-known criterion for power allocation is the maximization of the channel capacity under an average power constraint. The solution for the additive white Gaussian noise (AWGN) channel is known as water filling. Unfortunately, this solution assumes a continuous and Gaussian modulation so it is not optimum for practical systems using discrete constellations, since the bit rate assignments are constrained to be integer. In this case, if the bit loading has been previously determined, the power allocation that maximizes the mutual information is provided by the mercury/water filling policy (MWF) [5].

Since MWF only optimizes the power allocation a bit loading algorithm is also required. Unfortunately mutual information cannot be employed as the optimizing criteria for bit loading design when typical constellations (e.g. m-QAM, m-PSK) and optimum transceivers are considered, since for fixed SNR the largest constellation always provides the largest mutual information or we can say that the mutual information is maximized employing the largest constellation available at any.

The proposed algorithm does not provide significant gains in terms of spectral efficiency increase, but rather provides a new tool for joint bit loading and power allocation that maximizes the mutual information while it maintains the computational complexity of mercury/water filling. Although the algorithm is proposed for BICM-OFDM transmission it could be employed in any scenario where parallel subchannels arise (e.g. multiple antenna transmission where the MIMO channel is diagonalized through the use of linear pre/post-filtering based on its singular value decomposition) and where the transmission scheme results information vs. SNR curves that overlap for different configurations (e.g. APSK constellations). The rest of the paper is organized as follows. In section II we describe the BICM system, in section III detailed discussion of OFDM system is carried out in section IV we described Mercury Water filling policy and in V system set up is analyzed and then VI and VII will show simulated results and conclusion is done.

II. BIT INTERLEAVED CODED MODULATION (BICM) SYSTEM

In Coded Modulation System the code diversity, and reliability over Rayleigh fading channel could be further improved by making the code diversity equal to the smallest number of distinct bits along any error event and this can be achieved by Bit wise interleaving at the encoder output and by using appropriate soft decision bit metric as an input to the Viterbi decoder [2].

![Fig. 1: Block diagram of BICM system](image)

As depicted in Fig. 1 above, the basic building blocks of BICM system are 1) an Encoder (ENC), 2) An Interleaver, 3) a modulator, modeled by a labeling map and a signal set, i.e. a finite set of points in the complex dimensional Euclidean space, 4) a stationary finite memory vector channel whose transition probability density function may depend on vector parameter and finally a demodulator (DEM), which is nothing but a branch metric computer, 6) a branch metric de-interleaver, 7) a decoder (DEC).

The BICM can be obtained by employing an encoder ENC for a binary code \( C \), with an N-dimensional memory less modulator over a signal set \( \chi \subseteq \mathbb{C}^N \) of size \( |\chi|=2^m \), through a bit interleaver \( \pi \) and a one-to-one binary map \( \mu : \{0, 1\} \rightarrow \chi \). The code sequence \( C \) is first interleaved by \( \pi \). Next, the interleaved sequence \( \pi(C) \) is broken into subsequence of \( m \) bits each, which is mapped onto signal in \( \chi \). Finally, the resulting signals sequence \( x \) is transmitted over the vector channel. The bit interleaver can be seen as one-to-one correspondence \( \pi : k \rightarrow (k', i) \), where \( k \) denoted the time ordering bits \( c_k \), \( k' \) denoted the time ordering of the signal \( x_k \) transmitted over the vector channel, and \( i \) indicates the position of the bit \( C_i \) in the label of \( x_k \). Here we assume ideal bit interleaving.

Let \( \hat{x}(x) \) denote the \( i \)th bit of the label \( x \) and \( \hat{x}'(x) \) the subset of all the signal \( x \in \chi \) whose label has the value \( b \in \{0, 1\} \) in position \( i \). Further let \( \hat{b} \) denote the complement of \( b \) and \( y \) the channel output resulting from the transmission of \( x \).

The conditional pdf of \( y \), given \( \hat{x}(x) = b \) for \( b \in \{0, 1\} \) and 0, is,

\[
p(\theta(x|y)=b) = \sum_{\chi \in \chi} P(\theta(y|x)\mid P(x|\theta(x)=b) = \theta(y|x)
\]

The last expression is obtain by,

\[
p_b(\gamma(x)\mid \theta(x)=b) = p_b(y|x)
\]

And,

\[
P(x|\theta(x)=b) = \begin{cases} o, & \text{if } \gamma(x) = \hat{b} \\ 2^{-(m-1)}, & \text{if } \theta(x) = b \end{cases}
\]
Where we assume uniform input distribution,

\[ P(b=0) = P(b=1) = \frac{1}{2} \]  \hspace{1cm} (5)

Again the optimum receiver depends on the available CSI. Each time \( k' \) the demodulator Dem produces the set of ML bit metrics,

\[ \lambda_i(y_k, b) = \begin{cases} 
\log \sum \phi(k') \phi(k|x), \text{ for perfect CSI} \\
\log \sum \phi(k') \phi(k|x), \text{ for no CSI} 
\end{cases} \]  \hspace{1cm} (6)

For \( b \in \{0, 1\} \) and \( i=1, \ldots, m \), finally, the ML decoder DEC makes the decision according to the rule implemented by viterbi decoder.

This idea has been extended and employed in this paper with irregular power [6] for the design of practical bit loading scheme that optimize the performance taking into the account channel coding stage

### III. ORTHOGONAL FREQUENCY DIVISION MODULATION (OFDM)

OFDM is a frequency division multiplexing scheme used as digital multicarrier modulation method. A large number of closely spaced orthogonal sub carriers are used to carry data. The data is divided into several parallel data streams or channels, one for each sub carrier. Each sub carrier is modulated with a conventional modulation scheme (Such as QAM or PSK) at a low symbol rate, maintaining total data rate similar to conventional single carrier modulation schemes in the same bandwidth. The low symbol rate makes the use of guard interval between symbols affordable, making it possible to handle time spreading and eliminate inter symbol interference (ISI).

#### Idealized OFDM model

This section describes a simple idealized OFDM system suitable for a time invariant AWGN channel.

#### A. Transmitter

An OFDM carrier signal is the sum of a number of orthogonal sub carriers, with base band data on each sub carrier being independently modulated commonly using some type of QAM or PSK. This composite baseband signal is used to modulate a main RF carrier.

#### B. Receiver

As shown in Fig. 2, \( S[n] \) is a serial stream of binary digits. By inverse multiplexing, this is first demultiplexed into \( N \) parallel stream and each one mapped to a (possibly complex) symbol stream using some modulation constellation (QAM, PSK etc) [4]. Note that the constellation may be different, so some streams may carry higher bit rate than others. An inverse FFT is computed on each set of symbol, giving a set of complex time domain samples these samples are then quadrature – mixed to pass band in the standard way. The real and imaginary components are first converted to the analogue domain using digital to analogue converter, the analogue signals are used to modulate Cosine and Sine wave at the carrier frequency \( f_c \) respectively. These signals are then summed to give the transmission signal \( s(t) \).

#### IV. MERCURY/WATER FILLING (MWF) POLICY

Since the largest spectral efficiency achievable with arbitrary reliability is given by the mutual information, an enticing optimality criterion to allocate power is precisely the maximization of mutual information. For the capacity achieving Gaussian signals, such optimum allocation is solve by classical water filling policy. In practice, however, the ideal Gaussian signals must be forsaken in favor of discrete constellation for which the water filling policy ceases to be the optimal. Rather the
power allocation that maximizes the mutual information is then given by more general mercury water filling policy.

The objective use of mercury water filling policy in an exemplary frequency selective OFDM channel with QAM is twofold,

1. To cast insight on how the non ideal nature of constellation impacts the process of optimally allocating power.

2. To quantify the extent to which conventional water filling, applied in conjunction with QAM constellation is sub optimal when the mutual information is the driving performance major. Note that in contrast with power allocation solutions tailored to specific coding schemes, the information theoretic problem of allocating power in order to maximize the mutual information is technology non specific.

What distinguishes mercury water filling from conventional water filling is the mercury pouring stage, which regulates the water admitted by each vessel thereby tailoring the process to arbitrary signal distributions. Thus skipping step (2) directly turns mercury waterfilling policy into waterfilling and the difference is shown by the Fig. 4 below. Indeed, for Gaussian signal,

\[ \text{MMSE}^{-1}(\zeta) = \frac{1}{\zeta-1} \]

Fig. 4: Top chart: mutual information achieved by MWF as Function of PSK constellation

Bottom: chart: additional power required by water filling to achieve same mutual information with same constellation mercury is dark grey shaded area and the base level is the black shaded area. The mercury in channel 3 and 4 are only due to the interferences caused by the others input, because their allocated power is zero.

In the mercury water filing interpretation for non interfering channels, the mercury level for the J-th channel directly depends on SNR \(|h_{jj}|^2\), through the inverse MMSE, and the water level. The water level is numerically calculated ensuring that \( \{p_j\}_{j=1}^m \) add up to 1. For non diagonal H matrices, we solve the optimization problem in (2-4), jointly obtaining the power allocation and the water level (Lagrange multiplier). Thus the generalized mercury water filling interpretation facilitates understanding how the power is divided between the different inputs but it is not a procedure for setting the optimal power allocation figure belows depicts the generalized mercury water filling reinterpretation for MIMO channels. If \( m_{j<}A^{-1} \) the j-th input is not assigned power if \( m_j<0 \) then \( p_j = A^{-1} - m_j \). The mercury level for \( p_j=0 \) is the main difference between the mercury water filling for mutually interfering channels and for non interfering channels. For non interfering channels the mercury level is 0, if \( p_j=0 \) for interfering channel the mercury level can be non zero, if \( p_j = 0 \). This added mercury accounts for interference the other cause on the j-th input.

This also means that mercury level can be above the water level as depicted in Fig. 5 for channel 3 and 4, which would not be possible in mercury water filling interpretation for non interfering channels.

The base level can be understood as the barrier for an input to be assigned power. The mercury water filling interpretation introduces another barrier, namely the mercury level. In non interfering channels the mercury level accounts for the mismatch between the arbitrary input and the optimal Gaussian distribution. This barrier only kicks in when an input is assigned power. The mercury level measures what we are losing for using a given input instead of an optimal Gaussian distribution. This barrier depends on the used distribution, through the inverse of the MMSE, and all the other input channel responses and distributions, through the water level. Hence power gap approaches typically used to adjust the water filling from Gaussian inputs clearly failed to assign the correct power to each input. Because they do not take into account the effect of the other inputs to define this power gap.
Figure 5 Illustration of the Mercury water filling power allocation for a 7 input MIMO channels. The power for each input is the difference between the mercury level and water. The water is the light grey shaded area, the mercury is the dark grey shaded area and base level is black area. The mercury in channel 3 and 4 are only due to interferences caused by the other input, because their allocated power is zero.

V. SYSTEM MODEL

In this section we have described the system setup in which the proposed bit loading and power allocation policy will be employed. It consists of the application of irregular modulation and power allocation to BICM scheme in a scenario with multiple parallel sub channels.

Fig. 6 depicts the system block diagram including the coding, interleaving, mapping and power allocation stages. Following a BICM scheme, coded bits are subchannels (subcarrier in the case of OFDM) with coefficients \( \{H_1, \ldots, H_Q\} \). Denote by \( p(n) \) the power allocation to and by \( x_q(n) \) the unit-power transmitted through the \( q \)-th subchannel in the \( n \)-th channel access. The symbol belongs to one of the \( N \) available constellations, \( \{C_1, \ldots, C_N\} \), with \( \{m_1, \ldots, m_N\} \) bits per symbol respectively and possibly different labeling. Then the received signal is,

\[
y_q(n) = H_q \sqrt{p_q(n)} x_q(n) + w_q(n) \quad q=1,\ldots,Q\quad (7)
\]

Where \( W_q(n) \) in Eqn. 7, is the additive complex white Gaussian noise term of 0 mean and variance \( \sigma^2 \), independent among sub channels. At the receiver, the sub optimum detector computes the bit log-likelihood ratios (LLR’s) of the transmitted bits.

According to the irregular modulation and power scheme, we allow the transmission of symbols belonging to different constellations with different allocated power within the same sub channel and we let this configuration to be different for each sub channel. If more than constellation is used within a subchannel, the order in which bits are mapped is predefined at transmitter and receiver. Let \( \alpha_{iq} \) be the fraction of symbols transmitted through \( q \)-th subchannels that belongs to constellation \( C_i \), and let \( P_q \) be the power allocated to each one of them. According their definition the parameters must fulfill,

\[
\alpha_{iq} \geq 0, \quad P_q \geq 0 \quad \text{and} \quad \sum \alpha_{iq} \leq 1 \quad (8)
\]

For \( q=1,\ldots,Q \) and \( i=1,\ldots,N \). If \( \alpha_{iq} = 0 \), then constellation \( C_i \) is not employed in \( q \)-th subchannel.

If \( \sum_{i=1}^{N} \alpha_{iq} = 0 \), then \( q \)-th subchannel is not used and if \( 0 < \sum_{i=1}^{N} \alpha_{iq} < 1 \) then it is used during a fraction of channel access this formulation can be mathematically seen as continuous relaxation of usual bit allocation in which \( \alpha_{iq} \in \{0,1\} \).

Bit interleaved coded modulation is a flexible modulation/coding scheme which allows the designer to choose modulation constellation independently of the coding rate. This is because the output of the channel encoder and the input to the modulator are separated by bit-level interleaver. In order to increase spectral efficiency, BICM can be combined with high order modulation scheme such as QAM or PSK. BICM is particularly well suited for fading channels, and it only introduces a small penalty in terms of channel capacity when compared to code modulation capacity for both additive white Gaussian noise and fading channels. At the receiver side the reliability matrix are calculated for coded bits under the form of logarithm likelihood ratios. These metrics are then deinterleaved and further used by the soft input channel decoder.

An additional advantage of BICM compared to other scheme such as Trellis coded modulation is that due to the flexibility imposed by bit level interleaver, the implementation of adaptive modulation and coding scheme is state forward.

The objective of this paper is the derivation and analysis of bit loading and power allocation algorithm that maximizes the mutual information for the system set up defined in previous section. Using the parameters previously defined the power allocated to and the MI of the \( q \)-th subchannel are obtained as the weighted averages of the individual values for each constellation,

\[
P_q = \sum_{i=1}^{N} \alpha_{iq} p_{iq} \quad (9)
\]

\[
I_q = \sum_{i=1}^{N} \alpha_{iq} I_i (p_{iq}, Y_q) \quad (10)
\]

Where \( Y_q = |H_q|^2 / \sigma^2 \) is a measure of the channel reliability (the Snr with unit transmitted power) and \( I_i(\mu) = I_i(\mathbf{x}; \mathbf{LLR}(b_1), \ldots, \mathbf{LLR}(b_m)) \) is the MI between the transmitted symbols and the corresponding bit LLR’s at the Demodulator output for the output of the 1-
th constellation when it is employed in an AWGN channel with SNR $\mu$.

Finally the total MI averaged over all subchannels is,

$$I' = 1/Q \sum_{q=1}^{Q} I'q$$

$$\eta = 1/Q \sum i \sum_{q=1}^{Q} aiq mi$$ (11)

The optimum bit loading and power allocation is as the one that maximizes the MI with respect to $\alpha_{iq}$ and $p_{iq}$ subject to constraint in above equation and the average power constraint, that is,

$$\text{max} \ 1/Q \sum_{q=1}^{Q} \sum_{i=1}^{N} aiq I(i(piq \gamma q))$$

$$\text{s.t.} \ \alpha_{iq} \geq 0, \ p_{iq} \geq 0, \ \ i=1,\ldots,N$$

$$\sum_{i=1}^{N} aiq \leq 1, \ q=1,\ldots,Q$$

(13)

$$1/Q \sum_{q=1}^{Q} \sum_{i=1}^{N} aiq piq \leq PT$$

(14)

Where, $P_T$ is the maximum available power at the transmitter.

According to the average power allocated per subchannel, one can observe the joint optimization of the parameters for all subchannels can be formulated in two step. In first step the optimization of power allocation and bit loading for single AWGN channel is done.

Let us consider AWGN channel with reliability $\gamma$ and allocated power $P$. In this case, we denote parameters $\alpha_{iq}$ as $\alpha_i$ and $p_{iq}$ as $p_i$.

If normalized power parameter $\pi' = pi / P$, then first optimization as a function of SNR $\mu = P\gamma$ as,

$$\tilde{I}_o(\mu) = \text{max} \ \sum_{i=1}^{N} ai li(p^i \mu)$$

$$\text{s.t.} \ \sum_{i=1}^{N} ai = 1$$

(16)

The second step consist of power allocation over parallel subchannels as:

$$\tilde{I}_o(\mu) = \text{max} \ 1/Q \sum_{q=1}^{Q} \tilde{I}_o(\gamma q Pq)$$

$$\text{s.t.} \ 1/Q \sum_{q=1}^{Q} Pq \leq PT$$

In second step no bit loading is done. The power allocation is done by mercury water filling policy. In this way analysis of single AWGN channel and then design for multiple parallel subchannels is done.

### VI. RESULT

In this section we presented selected simulated results for different constellations and different modulation schemes (QAM and PSK) for both types of communication data i.e. for image signal as well as for audio signal, for confirming the efficiency of the proposed algorithm and the accuracy of performance approximation. The results of simulations and graph are shown below. The algorithm also calculates BER and PAPR for given data and plots the graph and frequency spectrum for different combinations.

#### A. Image Signal As Input

![Fig. 7 : For Image signal](image)

#### B. Audio Signal as Input Data

![Fig. 8 : Simulated output for given audio signal](image)
VII. CONCLUSION

In this paper we propose an optimal bit loading and power allocation algorithm that maximizes the mutual information with the power constraint for parallel sub channels. This algorithm can be employed for performance optimization for BICM system in combination with multicarrier transmission system, with channel state information at the transmitter and we have focused on minimization of BER using bit loading and power allocation. The proposed approach employs the constellation constraint mutual information functions and does not result in a greedy algorithm.

Initially, designing and power allocation for an AWGN channel is done which has a closed form solution and then computation of each channel realization is done using mercury water filling policy for power allocation over the set of parallel sub channels employ in all of them the equivalent constellation. Assuming that the optimum mutual information is calculated and tabulated initially, the complexity of our design is equivalent to the complexity of MWF policy, corresponding to search of optimum water level.

Selected simulated results have confirmed efficient performance improvements using the proposed algorithm and good accuracy of the performance approximations. The additional computational load due to incorporation of bit loading is negligible.

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Efficient Adaptive Beam Steering Using INLMS Algorithm for Smart Antenna

E. Anji Naik & CH. Bala Swamy
ECE Department, QIS College of Engineering and Technology, Ongole, India.
E-mail : eslavathanji@gmail.com, ch.balaswamy7@gmail.com,

Abstract – In this project, an efficient method for the pattern synthesis of the linear antenna arrays with the prescribed nulls and steering lobe is presented. The proposed method is based on Least Mean Square (LMS) algorithm; provide a comprehensive and detailed treatment of the signal model used for beam forming, as well as, describing adaptive algorithms to adjust the weights of an array. In order to improve the convergence rate of LMS algorithm in smart antenna system, this paper proposes the Interference Normalize Least Mean Square (INLMS) algorithm. By taking advantage of spatial filtering, the proposed scheme promises to reduce the bandwidth required for transmitting data by improving convergence rate. The performance of the INLMS algorithm in the presence of Multi-path effects and multiple users is analyzed using MATLAB simulations. The simulations when compared to that of the LMS algorithm, a 28% overall improvement in the convergence rate is observed. The results suggest that INLMS algorithm can improve the convergence rate and lead to better system efficiency.

Keywords - Adaptive array, Phase array, INLMS Algorithm, Smart Antenna, Steering.

I. INTRODUCTION

At present the number of cellular users is growing annually by approximately 50 percent. This poses a number of challenges to both governments and mobile service providers. This is a clear indication of issues that confronts governments and mobile service providers. The growing number of users requires increased deployment of mobile infrastructure to ensure greater. Also, the high demand for wireless communication services requires increased system capacities. There is a steady growth in required data rates as the demand for high-bit-rate service increases. To meet those requirements, current and next-generation wireless systems and networks such as IEEE 802.11a will support much higher data rates compared with established standards. Traditionally, increasing bandwidth resources does this. However, as the electromagnetic spectrum becomes a rare commodity, there is increased motivation towards research that exploits space selectivity.

Since the available spectrum for providing high data rate communication to a new subscriber is limited, there is no doubt that Smart Antenna’s are the best solution for increasing the system capacity and performance. Smart Antenna’s also ensure greater coverage; therefore less base stations are needed to cover the same area compared to conventional antennas.

II. SMART ANTENNA SYSTEMS

A smart antenna is a phased or adaptive array that adjusts to the environment. That is, for the adaptive array, the beam pattern changes as the desired user and the interference move, and for the phased array, the beam is steered or different beams are selected as the desired user moves.
Another significant advantage of the adaptive antenna systems is the ability to "create" spectrum. Because of the accurate tracking and robust interference rejection capabilities, multiple users can share the same conventional channel within the same cell.

III. ADAPTIVE BEAM FORMING

The basic adaptive algorithms that have been investigated for beam forming in mobile Communications include the trained and blind adaptive beam forming algorithms as classified in the following Figure under adaptive array (beam forming) algorithms.

A basic adaptive beam former is shown in Figure. The weight vector $w$ is calculated using the statistics of signal $X(k)$ arriving from the antenna array.

IV. TRAINED ADAPTIVE ALGORITHMS

Trained adaptive beam forming algorithms use a finite set of training symbols to adapt the Weights of the array and maximize the SINR. First, a training signal, which is known to both the transmitter and receiver, is transmitted by the transmitter. The beam former in the receiver uses the information of the training signal to compute the optimal weight vector. After the training period, data is sent and the beam former uses the weight vector computed previously to process the receiver signal. The trained adaptive algorithms drawback is the excessive utilization of transmission time and wastage of bandwidth. The trained adaptive algorithms are categorized based on their adaptation criteria and they are the LMS, SMI and RLS methods. For simulation study we use LMS from the trained adaptive algorithm.
V(A). LMS ALGORITHM

<table>
<thead>
<tr>
<th>TABLE</th>
<th>The Least Mean-Square Algorithm</th>
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<tbody>
<tr>
<td>LMS ALGORITHM</td>
<td></td>
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<tr>
<td>for each ( k )</td>
<td></td>
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<tr>
<td>( e(k) = d(k) - w^H(k)x(k) )</td>
<td></td>
</tr>
<tr>
<td>( w(k + 1) = w(k) + \mu \epsilon(k)x(k) )</td>
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</tr>
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</table>

Table: Least Mean-Square (LMS) algorithm

The constant that determines the amount by which the weights are adjusted during each iteration is step size \( \mu \). The choice of \( \mu \) plays a significant role in the performance of the algorithm. If the step size is sufficiently small, the process leads the estimate weights to the near optimal solution with a larger step size the convergence speed improves but at the expense of larger residual MSE. A trade off is involved and \( \mu \) must be carefully chosen according to specific needs of the system.

Some notable aspects of the performance of the Adaptive Filter are:

- LMS tends to reject the noisy data due to the smoothing action of the small step size parameter.
- LMS can track slowly varying systems, and is often useful in non-stationary environments.
- The LMS error function has a unique global minimum, and hence the algorithm does not tend to get stuck at undesirable local minima.
- LMS is computationally simple (m multiplications and m additions per iteration) and memory efficient. (Only one m-vector must be stored).
- The convergence of LMS is often slow (it may take hundreds or thousands of iterations to converge from an arbitrary initialization).

V(B). INLMS ALGORITHM

The adaptive learning rate for INLMS algorithm is

\[ \mu(n) = \min \left( \eta(n - 1), \frac{\sigma^2_e(n)}{\sigma^2_e(n)} \right) \]

Here in the proposed exponential update in place of more standard additive update NLMS. So we have to scale the adaptive parameter as

\[ \eta(n) = \eta(n - 1) \exp \left( \frac{-\rho}{\sigma^2_e(n)} \frac{\partial E(n)}{\partial \eta(n)} \right) \]

When the interference changes abruptly

\[ \overline{\sigma^2_e(n)} \]

Increases causing an instantaneous decrease in the learning rate.

VI. RESULTS AND DISCUSSION

The standard and normalized variants of the LMS algorithm were simulated using MATLAB and investigated to examine the differences in the convergence rate, squared error performance and accuracy of active tap detection in terms of the number, weight, and position of active taps in the unknown communication channel. Smart antenna simulations were then conducted using the Standard LMS algorithm to investigate the multipath and multi-user effects in the mobile environment. The performance of the Interference NLMS algorithm is examined in terms of convergence rate. In order to replicate realistic mobile environments, for those simulations with more than one multipath, each multipath experience a different gain, which contains both amplitude and phase components.

Fig: Convergence curves for different algorithms

The convergence curves that as shown in above figure shows the performance evolution of different algorithms like LMS, NLMS, GNGD including proposed algorithm Interference NLMS.
VII. CONCLUSION

This project work has been successfully presented the concept of Smart Antenna systems and its impact on mobile communication systems. This project work also includes system analyses of Smart Antennas were done with the aid of MATLAB simulation package. The focus of the project was the implementation of a detection-guided Interference normalized LMS algorithm for Smart Antenna systems. The NLMS algorithm is used due to its relatively low computational complexity, good stability properties, and relatively good robustness against implementation errors the detection-guided NLMS algorithm is implemented in the spatial domain by INLMS, as the characteristics of a wireless channel are typically sparse. The thesis examined adaptive array smart antenna systems and the effects that multipath components had on their performance. The results confirmed the great interest in smart antenna systems as they proved that smart antenna systems could steer beams for reception in the direction of desired incoming signals. Furthermore, they can also place nulls in the direction of interfering signals.

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Implementation of a High speed Multiplication on SOC using Twin precission process

G. Swapnasri, D. Chandrashakar & Sk. Sabiha Begum
ECE.Dept., PKSK College, ECE.Dept., VRS&YRN College
E-mail : swapnaautomatic@gmail.com, chandradupati@gmail.com, sabihalogicbytes@gmail.com

Abstract – We present the twin-precision technique for integer multipliers. The Twin-precision technique can reduce the power dissipation by adapting a multiplier to the bit width of the operands being computed. The technique also enables an increased computational throughput, by allowing several narrow-width operations to be computed in parallel. We describe how to apply the twin-precision technique also to signed multiplier schemes, such as Baugh-Wooley and modified-Booth multipliers. It is shown that the twin-precision delay penalty is small (5%—10%) and that a significant reduction in power dissipation (40%-70%) can be achieved, when operating on narrow-width operands. In an application case study, we show that by extending the multiplier of a general-purpose processor with the twin-precision scheme, the execution time of a Fast Fourier Transform is reduced with 15% at a 14% reduction in data path energy dissipation. All our evaluations are based on layout-extracted data from multipliers implemented in 130-nm and 65-nm commercial process technologies.

1. INTRODUCTION

Multiplication is a complex arithmetic operation, which is reflected in its relatively high signal propagation delay, high power dissipation and large area requirement. When choosing a multiplier for a digital system, the bit width of the multiplier is required to be at least as wide as the largest operand of the applications that are to be run on that digital system. The bit width of the multiplier is, therefore, often much larger than its operands, which leads to excessive power dissipation and long delay. This could partially be remedied by having several multipliers, each with a specific bit width, and using the particular multiplier with the smallest bit width that is large enough for the current multiplication. Such a scheme would assure that a multiplication would be computed on a multiplier that has been optimized in terms of power and delay for that specific bit width. Several multipliers with the same bit width could also be used in a Single Instruction Multiple Data (SIMD) fashion, in order to increase throughput, thus reducing total execution time for multiplication-intensive applications. However, using several multipliers with different bit widths would not be an efficient solution because of area overhead due to having multiple multipliers instances, and power overhead due to static power dissipation of inactive multipliers. Ever increasing performance requirements make it challenging to implement multipliers that are efficient in terms of throughput, delay, power, and area for a wide range of bit widths. There have been several studies on operand bit widths of integer applications and it has been shown that for the SPECint95 benchmarks more than 50% of the instructions are instructions where both operands are less than or equal to 16 bits (henceforth called narrow-width operations). This property has been explored to save power, through operand guarding. In operand guarding the most significant bits of the operands are not switched, thus power is saved in the arithmetic unit when multiple narrow-width operations are computed consecutively. Narrow-width operands have also been used to increase instruction throughput, by computing several narrow-width operations in parallel on a full-width data path. For the SPECint95 and media benchmarks, the power reduction of an operand guarded integer unit was 54% and 58%, respectively, which accounts for a total power reduction of around 5-6% for an entire data path. There have been several studies on operand guarding for multipliers. Huang introduced a two-dimensional operand guarding for array multipliers, resulting in a power dissipation that was only 33% of a conventional array multiplier. While there have been a lot of work on simple schemes for operand guarding, work to increase the throughput of a multiplier is more scarce. Achieving double throughput for a multiplier is not as straightforward as for an adder, where the carry chain can be cut at the appropriate place to achieve narrow width additions. It is of course possible to use several multipliers, where at least two have narrow bit width,
and let them share the same routing, as in the work of Loh. But this scheme has several drawbacks: i) The total area of the multipliers would increase, since several multiplier units are used. ii) The use of several multipliers increases the fan-out of the signals that drive the inputs of the multipliers. Higher fan-out means longer delays and/or higher power dissipation. iii) There would be a need for multiplexers that connect the active multiplier to the result route. These multiplexers would be in the critical path, increasing total delay as well as power dissipation. Work has been done to use 4:2 reduction stages to combine small tree multipliers into larger multipliers. This can be done in several stages, creating a larger multiplier out of smaller for each extra 4:2 reduction stage. The desired bit width of the multiplication is then obtained by using multiplexers. This technique requires extra reduction stages for the larger multipliers, which has a negative impact on the delay for these. We present the twin precision technique that offers the same power reduction as operand guarding and the possibility of double-throughput multiplications. The twin-precision technique is an efficient way of achieving double throughput in a multiplier with low area overhead and with practically no delay penalty. We show how to apply the twin-precision technique on signed multipliers based on the regular High Performance Multiplier (HPM) reduction tree. The two algorithms for signed multiplications that have been used are Baugh-Wooley and the popular modified-Booth algorithm.

II. TWIN PRECISION

2.1 Introduction to Twin precision:

During the last decade of integrated electronic design ever more functionality has been integrated onto the same chip, paving the way for having a whole system on a single chip. The strive for ever more functionality increases the demands on circuit designers that have to provide the foundation for all this functionality. The desire for increased functionality and an associated capability to adapt to changing requirements, has led to the design of reconfigurable architectures. With an increased interest and use of reconfigurable architectures there is a need for exited and reconfigurable computational units that can meet the demands of high speed, high throughput, low power, and area efficiency. Multiplications are complex to implement and they continue to give designers headaches when trying to efficiently implement multipliers in hardware. Multipliers are therefore interesting to study, when investigating how to design flexible and reconfigurable computational units.

The twin-precision technique can reduce the power dissipation by adapting a multiplier to the bit width of the operands being computed. The technique also enables an increased computational throughput, by allowing several narrow-width operations to be computed in parallel. In this thesis the results from investigations on flexible multipliers are presented. The new twin-precision technique, which was developed during this work, makes a multiplier able to adapt to different requirements. By adapting to actual multiplication bit width using the twin-precision technique, it is possible to save power, increase speed and double computational throughput.

2.2 Applying twin precision to general multiplication:

For a first analysis of the twin-precision technique, the discussion will be based on an illustration of an unsigned binary multiplication. In an unsigned binary multiplication each bit of one of the operands, called the multiplier, is multiplied with the second operand called multiplicand that way one row of partial products is generated. Each row of partial products is shifted according to the position of the bit of the multiplier, forming what is commonly called the partial-product array. Finally, partial products that are in the same column are summed together, forming the final result. An illustration of an 8-bit multiplication. Let us look at what happens when the precision of the operands is smaller than the multiplier we intend to use. In this case, the most significant bits of the operands will only contain zeros, thus large parts of the partial-product array will consist of zeros. Further, the summation of the most significant part of the Partial-product array and the most significant bits of the final result will only consist of zeros.

Figure 2.2.1: Illustration of an unsigned 8-bit multiplication, where the precision of the operands is smaller than the precision of the multiplication. Unused bits of operands and product, as well as unused partial products, are shown in gray. One can also observe that the column at position S7 should not be used either. This is because that column might have a carry from the active part of the partial-product array that will constitute the final S7. Altogether this makes only the partial products in the most significant part of the partial-product array available for a second.
In order to be able to use the partial products in the most significant part, there has to be a way of setting their values. For this we can use the most significant bits of the operands, since these are not carrying any useful information. If we are only looking at the upper half of the operands, the partial products generated from these bits are the ones. By setting the other partial products to zero, it is then possible to perform two multiplications within the same partial-product array, without changing the way the summation of the partial-product array is done. How the partial products, shown in gray, can be set to zero will be investigated in the implementation section later on. Assume, for now, that there is a way of setting unwanted partial products to zero, then it suddenly becomes possible to partition the multiplier into two smaller multipliers that can compute multiplications in parallel. In the above illustrations the two smaller multiplications have been chosen such that they are of equal size. This is not necessary for the technique to work. Any size of the two smaller multiplications can be chosen, as long as the precision of the two smaller multiplications together are equal or smaller than the full precision (NFULL) of the multiplication. To be able to distinguish between the two smaller multiplications, they are referred to as the multiplication in the East Significant Part (LSP) of the partial-product array with size NLSP, shown in white, and the multiplication in the Most Significant part (MSP) with size MSP, shown in black.

\[ \text{NFULL} = \text{NLSP} + \text{MSP} \]

It is functionally possible to partition the multiplier into even more multiplications. For example, it would be possible to partition a 64-bit multiplier into four 16-bit multiplications. Given a number K of low precision multiplications their total size need to be smaller or equal to the full precision multiplication.

\[ \sum_{k=1}^{K} \text{N} = \text{NFULL} \]

For the rest of this investigation, the precision of the two smaller multiplications will be equal and half the precision (N=2) of the full precision (N) of the multiplier.

### 2.3 First Implementation:

The basic operation of generating a partial product is that of a 1-bit multiplication using a 2-input AND gate, where one of the input signals is one bit of the multiplier and the second input signal is one bit of the multiplicand. The summation of the partial products can be done in many different ways, but for this investigation we are only interested in parallel multipliers that are based on 3:2 full adders. For this First implementation an array of adders will be used because of its close resemblance to the previously used illustration of a multiplication. In the previous section we assumed that there is a way of setting unwanted partial products to zero. This is easily accomplished by changing the 2-input AND gate to a 3-input AND gate, where the extra input can be used for a control signal. Of course, only the AND gates of the partial products that has to be set to zero need to be changed to a 3-input version. During normal operation when a full-precision multiplication is executed the control signal is set to high.

![Figure 2.3.1: Block diagram of an unsigned 8-bit array multiplier](image)

Figure 2.3.1: Block diagram of an unsigned 8-bit array multiplier thus all partial products are generated as normal and the array of adders will sum them together and create the final result. When the control signal is set to low the unwanted partial products will become zero. Since the summation of the partial products is not overlapping, there is no need to modify the array of adders. The array of adders will produce the result of the two multiplications in the upper and lower part of the final output. The block diagram of an 8-bit twin-precision array multiplier capable of computing two 4-bit multiplications is shown in Fig.2.3.1. The two multiplications have been colored in white and black to visualize what part of the adder array is used for what multiplication. More flexibility might be wanted, like the possibility to compute a single low-precision multiplication or two parallel low-precision multiplications, within the same multiplier. This can be done by changing the 2-input AND gates for the partial product generation of the low-precision multiplication as well. In the array multiplier in Fig.2.5 the AND gates for the 4-bit MSP multiplication, shown in black, can be changed to 3-input AND gates to which a second control signal can be added. Assuming the multiplier is divided into two equal parts, this modification makes it possible to either compute an N-bit, a single N=2-bit or two concurrent N=2-bit multiplications.

### 2.4 An HPM Implementation:

The array multiplier in the previous section was only used to show the principle of the twin-precision technique. For highspeed and/or low-power
implementations, a reduction tree with logarithmic logic depth, such as TDM, Dadda, HPM is preferred for summation of the partial products. Such a log-depth reduction tree has the benefit of shorter logic depth. Further, a log-depth tree suffers from fewer glitches making it less power dissipating. A twin-precision implementation based on the regular HPM reduction tree is shown in Fig. 2.4.1.

Fig2.4.1: Block diagram of an unsigned 8-bit twin-precision multiplier that is based on the regular HPM reduction tree. A 4-bit multiplication, shown in white, can be computed in parallel with a second 4-bit multiplication, shown in black. For simplicity of the figure the AND gates for partial-product generation is not shown and a ripple carry is used as final adder.

III. BAUGH-WOOLEY MULTIPLICATION

Baugh-Wooley multiplier
- Algorithm for two’s-complement multiplication.
- Adjusts partial products to maximize regularity of multiplication array.
- Moves partial products with negative signs to the last steps; also adds negation of partial products rather than subtracts.

3.1 Algorithm For Baugh-Wooley:

The BW algorithm is a relative straightforward way of doing signed multiplications. Fig. 8 illustrates the algorithm for an 8-bit case, where the partial product array has been reorganized. The creation of the reorganized partial-product array comprises three steps: i) the most significant partial product of the first N-1 rows and the last row of partial products except the most significant has to be negated, ii) a constant one is added to the Nth column, iii) the most significant bit (MSB) of the final result is negated.

3.2 Twin Precision Using Baugh-Wooley Algorithm:

To combine twin-precision with BW is not as simple as for the unsigned multiplication, where only parts of the partial products needed to be set to zero. To be able to compute two signed N=2 multiplications, it is necessary to make a more sophisticated modification of the partial-product array. Fig. 1.8 shows an illustration of an 8-bit BW multiplication, where two 4-bit multiplications have been depicted in white and black. When comparing the illustration of Fig. 3.1 with that of Fig. 3.2 one can see that the only modification needed to compute the 4-bit multiplication in the MSP of the array is an extra sign bit ‘1’ in column S12. For the 4-bit multiplication in the LSP of the array, there is a need for some more modifications. Looking at the active partial-product array of the 4-bit LSP multiplication (shown in white), we see that the most significant partial product of all rows, except the last, needs to be negated. For the last row it is the opposite, here all partial products, except the most significant, are negated. Also for this multiplication a sign bit ‘1’ is needed, but this time in column S4. Finally the MSB of the result needs to be negated to get the correct result of the two 4-bit multiplications.

To allow for the full-precision multiplication of size N to coexist with two multiplications of size N=2 in the same multiplier, it is necessary to modify the partial-product generation and the reduction tree. For the N=2-bit multiplication in the MSP of the array all that is needed is to add a control signal that can be set to high, when the N=2-bit multiplication is to be computed and to low, when the full precision N multiplication is to be computed. To compute the N=2-bit multiplication in the LSP of the array, certain partial products need to be negated. This can easily be accomplished by changing the 2-input AND gate that generates the partial product to a 2-input NAND gate followed by an XOR gate. The second input of the XOR gate can then be used to invert the output of the NAND gate. When computing the...
N=2-bit LSP multiplication, the control input to the XOR gate is set to low making it work as a buffer. When computing a full-precision multiplication the same signal is set to high making the XOR work as an inverter. Finally the MSB of the result needs to be negated and this can again be achieved by using an XOR gate together with an inverted version of the control signal for the XOR gates used in the partial-product generation. Setting unwanted partial products to zero can be done by 3-input AND gates as for the unsigned case.

IV. MODIFIED-BOOTH IMPLEMENTATION

4.1 Algorithm for Modified-Booth:

The original Booth algorithm is a way of coding the partial products generated during a \( s = x \times y \) multiplication. This is done by considering two bits at a time of the x operand and coding them into \{ -2, -1, 0, 1, 2 \}. The encoded number is then multiplied with the second operand, y, into a row of recoded partial products. The number of recoded partial products is fewer than for a scheme with unrecoded partial products and this can be translated into higher performance. The drawback of the original-Booth algorithm is that the number of generated partial products depends on the x operand, which makes the Booth algorithm unsuitable for implementation in hardware. The MB algorithm remedies this by looking at three bits at a time of operand x. Then we are guaranteed that only half the number of partial products will be generated, compared to a conventional partial product generation using 2-input AND gates. With a fixed number of partial products the MB algorithm is suitable for hardware implementation. Fig.4.1 shows which parts of the x operand that are encoded and used to recode the y operand into a row of partial products.

![Fig 4.1:8-bit Modified-both encoding](image)

A MB multiplier works internally with two's complement representation of the partial products, in order to be able to multiply the encoded \{-2,-1\} with the y operand. To avoid having to sign extend the rows of of recoded partial products, the sign-extension prevention scheme by has been used. In two's complement representation, a change of sign includes the insertion of a '1' at the Least Significant Bit (LSB) position. To avoid getting an irregular partial-product array we draw on the idea called modified partial-product array. The idea is to pre-compute the impact on the two least significant positions of a row of recoded partial products by the insertion of a '1' during sign change. The pre-computation calculates the addition of the LSB with the potential '1', from which the sum is used as the new LSB for the row of recoded partial products. An potential carry from the pre computation is inserted at the second least significant position. The pre-computation of the new LSB can be done according to Eq.4.1. The pre-computation of a potential carry is as given by Eq.4.2.

\[
\begin{align*}
\bar{y}_{LSB} &= \bar{y}(2_{2i-1} \oplus \bar{y}2_{i}) \\
q_i &= x_{2i+1}(\bar{y}_{2i} \oplus \bar{x}2_{i} + y_{LSB} + x_{2i} + \bar{x}y_{LSB} + \bar{x}_{2i-1})
\end{align*}
\]  

(4.1),(4.2)
4.2 Twin-Precision Using the modified-Booth Algorithm:

Implementing twin-precision together with the MB algorithm is not as straightforward as Baugh-wooley algorithm. It is not possible the partial products from the full-precision MB multiplication and use only the partial products that are of interest for the low-precision MB multiplications. The reason for this is that all partial products are not computed the same way and there exist several special cases that need to be handled.

- The partial-products that are denoted p42 and p43 during normal 8-bit multiplication need to define pLSB2 and pLSB3 for the low-precision 4-bit multiplication in the MSP.
- The aMSP0 and aMSP1 that are needed for the multiplication in the MSP have to be added.
- The pattern of 1's and 0's for the normal 8-bit multiplication cannot be used in low-precision mode. For the two 4-bit multiplications, we need two shorter patterns of 1's and 0's.

The implementation of the MB twin-precision multiplication does not call for any significant changes to the reduction tree of a conventional MB multiplier. When comparing the multiplications we can see that the position of the signals in the lowest row is the only difference that has an impact on the reduction tree. This means that there is a need for an extra input in two of the columns (N=2 and 3N=2) compared to the conventional multiplier; this requires two extra half adders in the reduction tree. The biggest difference between a conventional MB multiplier and a twin precision MB multiplier is the generation of inputs to the reduction tree. To switch between modes of operation, logic is added to the recoder to allow for generation of the partial products needed, for sign-extension prevention as well as pLSBi, which are needed for N=2-bit multiplications in the LSP and the MSP, respectively. There is also a need for multiplexers that, depending on the mode of operation, select the appropriate signal as input to the reduction tree. Further, partial products that are not being used during the computation of N=2-bit multiplications have to be set to zero in order to not corrupt the computation. The logic encode and decode can be implemented in many different ways. For this implementation we have chosen the encoding scheme presented, since they claim that their recoding scheme is faster than competing schemes. The circuits for encoding and decoding is shown in Fig.4.5. For the partial products that need to be set to zero, an extra 2-input AND gate has been added at the output of the decode stage. The second input of the AND gate can then be used as a control signal, as in the case of for the unsigned and BW implementations. This is a straightforward method, and it is possible to construct even more efficient solutions for setting the partial product to zero. A decode circuit based on a custom layout, capable of setting the output to zero. The outputs of the encoders have also been set to zero by using AND gates. This is not necessary for correct operation, but it reduces the power dissipation when computing N=2-bit multiplications due to reduced switching.

![Encode and Decode circuit for Modified-Booth](image)

For correct operation the input to the encoder for the first row in the N=2-bit MSP multiplication has to be set to zero, instead of using xN=2 1 as its input. An example of the encoding scheme for two 4-bit multiplications can be seen in Fig.4.6.

![Encoding sheme for two 4-bit multiplications](image)

In order to separate the two different N=2-bit multiplications, such that the multiplication in the LSP does not interfere with the multiplication in the MSP, we need to consider some other issues. By looking at the pattern of 1's and 0's that is used for sign-extension prevention, we see that the most significant '1' is only used to invert the final s2N 1-bit. However, the carry that this extra '1' potentially could generate is not of interest for the final result. If the most significant '1' for the multiplication in the LSP would be inserted into the reduction tree it would mean that a carry could be generated. This potential carry would propagate into the multiplication in the MSP and corrupt the result. To avoid inserting the most significant '1', an XOR gate is added after the final adder allowing the MSB of the N=2 bit LSP multiplication to be negated, which is the sole purpose of the most significant '1'.

5.1 Simulation Setups:

To evaluate the efficiency of the twin-precision technique a multiplier generator has been written. The generator is capable of generating VHDL descriptions of conventional Baugh-Wooley (BW) and modified Booth
Implementation of a High speed Multiplication on SOC using Twin precision process

(MB) multipliers as well as twin-precision versions of both of these, according to the schemes presented in the previous sections. An adder was chosen as final adder for all types of multipliers. The VHDL generator has been verified to generate correct multipliers of sizes up to 16 bits by simulating all possible input patterns and verifying the result VHDL. For multipliers larger than 16 bits, the functionality was verified by feeding the multipliers with a finite random input pattern and verifying the result. The VHDL descriptions were synthesized using Design Compiler by Synopsis together with a commercially available 0.13nm technology. For delay and power estimations, Synopsis Primetime and Prime Power were used. The delay has been estimated by assuming a 10 fF load on the primary output signals and a medium-size buffer from the cell library as driver for primary input signals. The chosen buffer cell is specified to be capable of driving approximately 150 minimum-size XOR gates. This is of course an overkill for the smaller multipliers of this evaluation but the same driver has been used for consistency of our analysis. For average power analysis, a clock period of 5 ns (200 MHz) and Prime Power’s default values for switching activity. Further, it was assumed that the twin-precision multipliers will operate in the same mode (Full, 1xN=2, or 2xN=2 precision) for a long period of time. The power for the control signals has not been included, since these low-activity signals would only have a minor contribution to the total power.

5.2 Synthesized Baugh-Wooley Net list:

The synthesis and the timing analyses showed that the simplicity of the BW implementation comes with an added benefit in that it does not create high fan-out signals. The signals with highest fan-out in the BW case are the input signals, which are connected to the input of N 2-input AND gates for a multiplier of size N. This creates a reasonable fan-out of the input signals for multipliers up to at least 64 bits without losing any significant performance2. The mapping of the BW multiplier VHDL code to gate-level net list during synthesis was only constrained in the way that half and full adders of the reduction tree was mapped to their respective minimum-size cells and the map effort was set to high.

5.3 Synthesized Modified-Booth Net list:

The first attempt of synthesizing the VHDL code for the generated multipliers exposed a big problem with high fan-out signals. This can easily be realized by investigating the encode and decode circuits from Fig. 1.14. As can be seen, the x2i+1 input signal goes straight through the encoder as the NEG signal and drives two XNOR gates for each partial product of a single row. This means that the fan-out of half of the primary x-inputs is at least 2N XNOR gates for a multiplier of size N. Further, the encoder outputs X1, Z, and X2 drive N decoders creating a need for large XOR and XNOR gates in the encode stage, which increases the fan-out of the x-inputs even more. To deal with the fan-out problem, the X1, Z and X2 signals fan-out have been reduced by instantiating multiple encoders for each row of partial products. To limit the fan-out of the x2i+1 signal an inverter buffer has been inserted to drive the NEG signal. Finally min-size inverters have been added to xi-1, xi, and xi+1, inputs of the encoder, thus, the fan-out of primary x-inputs is reduced. The new encode circuit can be viewed in Fig.5.1.

Fig 5.1: Buffered encode circuit for fan-out reduction

The mapping of the MB multiplier VHDL code to gate-level net list has been constrained in such way that Design Compiler could not remove the minimum size inverters of the new encoder, Fig. 1.16. In all other respects the synthesized net list of the MB multiplier has been constrained in the same way as the BW net list. In other words half and full adders of the reduction tree have been mapped to their respective cells of minimum size from the cell library and the map effort was set to high.

VI. RESULTS:

6.1 Twin General Multiplier:

Fig 6.1: Output represents Twin general multiplication
6.2 Twin Baugh Wooley:

Fig 6.2: Output represents Baugh-wooley multiplication using twin precision

6.3 Twin Modified Booth:

Fig6.3: Output represents Modified-booth multiplication using twin precision

6.4 Comparision:

One of the goals of the twin-precision technique is to keep the performance degradation of the multiplier’s full-precision operation at a minimum. To compare twin-precision implementations against conventional Baugh–Wooley (BW) and modified-Booth multipliers (MB), each multiplier was taken through the EDA flow outlined previously. The delay and power dissipation for conventional and twin-precision BW and MB multipliers of size 16, 32, and 48 bits. The figure shows how the power changes as the timing requirements are relaxed with 100, 300, and 600 ps. A clear trend is that a BW implementation is more power efficient than a MB implementation. However, a MB implementation can, in some cases, exhibit higher maximum speed. The result of the comparison of the twin-precision implementations with their conventional counterparts is that a twin-precision implementation of Baugh–Wooley performs equal in terms of delay for the 16- and 48-bit case and is only 160 ps slower for the 32-bit case. When we consider power, the twin-precision implementation dissipates 8%, 5%, and 6% more power than a conventional 16-, 32-, and 48-bit BW implementation. From our results it is clear that the complexity of the MB recoding circuit makes it difficult to efficiently update an MB implementation into a twin-precision multiplier. The MB twin-precision implementation has the poorest performance, both in terms of delay and power, of the four compared implementation choices.

6.5 Power Reduction by the Use of Power Gating:

Even though the reduction in power by the use of the twin-precision technique is substantial, the power overhead of an N-bit multiplication compared to a conventional multiplier of size is high. For the 32-bit twin-precision BW implementation operating on a single 16-bit data, the overhead is 55% in our 130-nm technology evaluation. This overhead is reduced to 15% per operation if the twin-precision multiplier is operating on two 16-bit data concurrently. The reduction in power overhead is due to less logic of the multiplier being idle and leaking, and that the static power dissipation of the idle logic is amortized over two 16-bit operations. To reduce the power dissipation overhead of the narrow-width mode it is possible to apply power gating, instead of only setting the partial products to zero by the use of three-input AND gates. Power gating involves adding power switches to the logic cells that should be gated off when idle, effectively isolating the cell from the power supply when the cell is idle. The output of the power-gated cells will, thus, be undefined and to avoid these signals to interfere with the computation in the active part of the multiplier, they need to be forced to zero.

A previous work of ours showed that by using precision dependent power gating based on the SCCMOS technique, the power overhead for a 16-bit BW multiplier can be reduced by 53% at a delay penalty of less than 3%. To be able to apply power gating to different areas of the partial-product generation, the reduction tree, and the final adder, a suitable power grid is needed.

VII. CONCLUSION:

It turns out that the Baugh-Wooley algorithm implemented on a HPM reduction tree is particularly suitable for a twin-precision implementation. Due to the simplicity of the implementation, only minor
modifications are needed to comply with the twin-precision technique. This makes for an efficient twin-precision implementation, capable of both signed and unsigned multiplications.

**VIII. FUTURE SCOPE:**

Currently a lot of research is done on reconfigurable architectures, where the architecture can be adapted to the applications that are being executed. Some of these proposed architectures can adapt their arithmetic logic units to operate on different bitwidths, depending on the application. One such reconfigurable architecture is that of the FlexSoC project. In these types of architectures it is necessary to have a multiplier that can efficiently operate over a wide range of bitwidths. The twin-precision technique, which offers flexibility at a low implementation overhead, makes it possible to efficiently deploy these flexible architectures.

**REFERENCES:**


Design Approaches for Low Power- Low Area
D Flip Flop_S in Nano Technology

Fayaz khan & Sireesh Babu
Department of Electronics and Comm Engineering, Prakasam Engineering College,
Kandukuru (M); Prakasam(Dt); A.P, India
E-mail : fayazkhan4u@gmail.com, sireesh1984@gmail.com

Abstract – This paper enumerates design of D flip flop with low power and low area for low power applications, for that analysis of various D-flip flops for low power dissipation, area and delays is carried out at 0.12um to achieve low power, low-area the technology is scaled down to nanometer ranges, due to shrinking process, the leakage power tends to play a vital role in total power consumption at nano meter technology. In this paper, different D flip flop circuits are designed using Berkeley Short Channel Insulated Gate MOSFET (BSIM4) model equations, in this paper to reduce leakage power at 90nm 70nm and 50nm we implement leakage power reduction techniques six techniques are considered they are namely Sleep transistor, sleepy stack, Dual sleep, Dual stack, Forced Transistor sleep (FTS) and Sleepy keeper. From the results, it is observed that SLEEP TRANSISTOR, and SLEEPY KEEPER, FORCED TRANSISTOR SLEEP techniques produces lower power dissipation than the other techniques, in this paper a qualitative comparison is done with the help of Dsch, Micro wind Simulation tools, this paper concludes that a leakage reduction technique produce different power optimization levels for different architectures and employing a suitable technique for a particular architecture will be an effective way of reducing the leakage current and thereby static power.

Keywords - D Flip Flop, Leakage power, Forced Transistor Sleep, sleep transistor, sleepy keeper.

I. INTRODUCTION

Flip-Flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. Flip-flops are often used in Computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period. At each rising or falling edge of a clock signal, the data stored in a set of flip-flops is readily available so that it can be applied as inputs to other combinational or sequential Circuitry. Delay Flip-Flop (DFF) has been the integral part of any digital system to construct the sequential part of it, to achieve low power low area we have design various D flip flop to analyze the performance of various architectures of DFF with respect to performance metrics such as power, delay, area and Power Delay Product(PDP) at. But as technologies scales down to the nanometer regime (Deep Sub-Micron (DSM)), the static power dissipation becomes more dominant than the dynamic power consumption.

With technology downscaling, interconnect resistance and capacitance increase the propagation delay. Leakage power optimization will be a key design objective in future CMOS circuits, power will continue to be a limiting factor in future technologies. Two major factors for the increase in power dissipation are the speed and the number of gates on the silicon. The two main effects that contribute to the total power dissipation on a chip are the active and static power dissipation. The expression to compute the total power is as follows

\[ P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}} + P_{\text{leak}} \]  

Dynamic dissipation power occurs when a transistor switches state and is due to capacitive charging and discharging associated with the output wiring. A small proportion of dynamic power arises from the short-circuit current that flows momentarily while the complementary devices (push/pull) in a circuit are simultaneously conducting during a change in the output state. This dynamic power is considerable during normal mode of operation, especially at high operating frequencies. The dynamic power consumption \( P_{\text{dynamic}} \) is given by

\[ P_{\text{dynamic}} = KCV_{\text{dd}}^2 \alpha_i \]  

International Conference on Advances in Electrical and Electronics Engineering (AEEE), ISBN : 978-93-81693-69-8, 22nd July 2012, Vijayawada 32
Where \( k \) is the technology factor, \( C \) is the capacitance of switching nodes, \( V_{dd} \) is the supply voltage and \( f_{sw} \) is the effective switching frequency. During the transition of signals from 0 to 1 (or) from 1 to 0 both nmos and pmos network of CMOS circuits will be on for a while which leads to short-circuit power dissipation (\( P_{sc} \)) and given by

\[
P_{sc} = I_{sc} V_{dd} T_s f_{sw}
\]  

(3)

Where \( I_{sc} \) is the short circuit current, \( T_s \) is the switching delay. Both sources of power dissipation (\( P_{dyn} \) and \( P_{sc} \)) in CMOS circuits are related to transitions at gate outputs and are therefore collectively referred to as active dissipation. In contrast, the third source of power dissipation (\( P_{static} \)) is due to leakage current, which flows when the inputs and outputs are changing their state and is called static dissipation. In standard CMOS circuits, only static dissipation is due to leakage current, usually small in magnitude and will be computed by

\[
P_{static} = I_{leak} V_{dd}
\]  

(4)

But as the supply voltage is being scaled down to reduce dynamic power, lower threshold transistors have to be used to maintain performance, yet the lower the threshold voltage, greater the standby leakage current. Due to the substantial increase in leakage current, the static power consumption is expected to exceed switching portion of power consumption unless effective measures are taken to reduce leakage power. Leakage power plays a vital role in deciding the overall power consumption.

II. LEAKAGE POWER ANALYSIS

We have different types of leakage components. They are

1. Sub-threshold leakage (weak inversion current)
2. Gate oxide leakage (Tunneling current)
3. Channel punch through
4. Drain induced barrier lowering

A. Sub Threshold Leakage:

One of the main reasons causing the leakage power increase is increase of sub-threshold leakage power. The Sub-threshold conduction or the sub-threshold leakage or the sub threshold drain current is the current that flows between the source and drain of a MOSFET when the transistor is in sub-threshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage. The sub-threshold region is often referred to as the weak inversion region. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially a sub threshold voltage decreases which increases the sub-threshold leakage power. Sub threshold or weak inversion conduction current between source and drain in a MOS transistor occurs when gate voltage is below the transistor threshold voltage (Vt). The Sub threshold or weak inversion current (\( I_{ds} \)) can be expressed as

\[
I_{ds} = \mu_{n} C_{ox} W \left( \frac{2}{L} \right) \left( V_{gs}-V_{th} \right) e^{\frac{V_{gs}}{2V_{th}}} \left( 1-e^{-\frac{V_{ds}}{V_{th}}} \right)
\]  

(5)

Where

\[
m = 1 + \frac{C_{dm}}{C_{ox}} \left[ \frac{5}{10} \right] \left( \frac{V_{gs}}{V_{th}} \right)
\]

and is threshold voltage and is the thermal voltage, is the gate oxide capacitance, is the zero bias mobility and is the body effect coefficient, is the maximum depletion layer width and is the gate oxide thickness is the capacitance of the depletion layer. Reverse biasing well to source junction of a MOSFET widens the bulk depletion region and increases the threshold voltage. The effect of body bias can be considered in the threshold voltage equation.

B. The Gate Oxide Leakage:

The gate oxide, which serves as insulator between the gate and channel, should be made as thin as possible to increase the channel conductivity and performance. But as the gate oxide is made thinner the barrier voltage of the oxide changes. For the positive gate voltage thus some positive charges get stuck in the oxide. Therefore, current flows through the oxide. This is also known as tunneling current.

C. Channel Punch Through:

Punch through in a MOSFET is an extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region. The field underneath the gate then becomes strongly dependent on the drain-source voltage, as is the drain current. Punch through
causes a rapidly increasing current with increasing drain-source voltage. This effect is undesirable as it increases the output conductance and limits the maximum operating voltage of the device.

III. REVIEW OF LEAKAGE CURRENT REDUCTION TECHNIQUES

For a CMOS circuit, the total power dissipation includes dynamic and static components during the active mode of operation. In the standby mode, the power dissipation is due to the standby leakage current. Dynamic power dissipation consists of two components. One is the switching power due to charging and discharging of load capacitance. The other is short circuit power due to the nonzero rise and fall time of input waveforms. The static power of a CMOS circuit is determined by the leakage at the circuit level.

A. Existing Approaches: (Sleep Transistor Approach)

In previous MTCMOS approach, sleep and sleep bar transistors of high threshold voltages are inserted in series between the circuit and VDD and ground. Due to this high threshold voltage the additional delay will add to the main circuit so in sleep transistor approach we use same threshold voltage to sleep transistors. When sleep input is OFF and sleep bar input is ON, there is no current flow in the low threshold voltage main circuit. When sleep is ON and sleep bar input is OFF then the circuit works in normal mode, the sleep transistor technique dramatically reduces leakage power during sleep mode. The additional sleep transistors increase area and delay but it is low compare to MTCMOS.

B. Sleepy Stack Approach:

The sleepy stack approach uses sleep transistor and the stacked transistor in each network are made parallel. Here the width of the sleep transistors is reduced. The activity of the sleep transistors in sleepy stack is same as the activity of the sleep transistors in the sleep transistor technique. The sleep transistors are turned on during active mode and turned off during sleep mode. The high Vth transistors are used for the sleep transistor and the transistors parallel to the sleep transistor without incurring large delay increase. The delay time is increase sing here but it gives low leakage. During sleep mode both the sleep transistors are turned off. But the sleepy stack structure maintains exact logic state.

C. Dual Sleep Approach:

In dual sleep method two sleep transistors in each NMOS or PMOS block are used. One sleep transistor is used to turn on in ON state and the other one is used to turn on in OFF state. Dual sleep approach uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. It uses two pull-up sleep transistors and two pull-down sleep transistors. When S=1 the pull down NMOS transistor is ON and the pull-up PMOS transistor is ON since S"=0. So the arrangement works as a normal device in ON state. During OFF state S is forced to 0 and hence the pull down NMOS transistor is OFF and PMOS transistor is ON and the pull-up PMOS transistor is OFF while NMOS transistor is ON. So in OFF state a PMOS in series with an NMOS both in pull-up and pull-down circuits which is liable to reduce power.

D. Dual Stacked Sleep Approach:

This technique uses two stacked sleep transistor in Vdd and two stacked sleep transistor in ground. So, leakage reduction in this technique occurs in two ways. First, the stack effect of sleep transistors and second, the sleep transistor effect. It is well known that pmos transistors are not efficient at passing GND; similarly, it is well known that nmos transistors are not efficient at passing Vdd. But this stacked sleep technique uses pmos transistor in GND and nmos transistor in Vdd for maintaining the exact logic state during sleep mode. The extra two transistors of the design for maintaining the logic state during sleep mode.

E. Advance Approaches:

1. Sleepy Keeper Approach:

The sleepy keeper circuit maintains output value of and an NMOS transistor continue this value during sleep mode. An additional NMOS transistor is added in parallel to the pull up sleep transistor connected to Vdd. In sleep mode this NMOS transistor is the only source of Vdd to the pull-up network since the sleep transistor is off. Similarly, to maintain a 0" value, The sleepy keeper approach maintain output value of 0" and a PMOS transistor maintains the value during sleep mode. An additional PMOS transistor is added in parallel to the pull down sleep transistor connected to GND. At sleep mode this PMOS transistor is only source of GND the pull down network since the sleep transistor is off. The draw backs of sleepy keeper is that it consumes 31% more dynamic power than the sleepy stack.

2. Forced Sleepy Approach:

The forced sleep method has a structure merging the forced stack technique and the sleep transistor
technique, uses $W/L = 3$ for the pmos transistors and $W/L = 1.5$ for the nmos transistors, ld use $W/L = 6$ for the pull-up transistor and $W/L = 3$ for the pull-down transistor (assuming $\mu_n = 2\mu_p$). Then sleep transistors are added in series to each set of two stacked transistors. We use two sleep transistors here, the nmos sleep transistor with Vdd and the pmos sleep transistor with ground. Conventionally the nmos transistor is connected to ground because it is very efficient passing ground voltage and the pmos transistor is connected to Vdd because it is efficient passing Vdd. In forced sleep method we just reverse the connection. That’s why we have some delay penalty in our method. We use same $W/L$ for all the pmos and nmos transistors.

IV. EXPERIMENT SET UP AND RESULTS

This paper aims at analyzing the performance of different architectures of DFF with respect to performance metrics such as power, area, delay and Power Delay Product (PDP). Four D flip flop architectures with True Single Phase Clocking (TSPC) has been considered with 12, 8 and 5 transistors Figures 1,2,3,4 respectively and observe the simulated results and for low area, design the DFF which has low power dissipation, at nano meter technology 90nm,70nm,50nm and apply the different leakage power reduction techniques and comparison of the above performance metrics for different leakage reduction techniques is carried out. The Simulation results of average 20ns are observed. Since all the parameters are derived using Berkley Short Channel Insulated Gate FET simulation model, the simulated results are expected to be very close to actual results.

From the results, it is observed from Table (1) that the proposed 5T-TSPC circuit produces low power dissipation (4.23uw), compare to other 12,8,5 transistor D flip flop and in nano meter technology when leakage reduction techniques were applied on this type of D flip flop the Sleepy transistor technique produces best result of $P_{avg}$ (30%) power reduction when compared to base case, and sleep transistor Technique reports (99.9%) reduction of the leakage power and Power Delay Product is also minimum for sleepy transistor technique.
Fig. 4: Shows the Model Diagram of 5t proposed DFF

Fig. 5: Shows the Simulated waveform 1 of 12t DFF

Fig. 6: Shows the Simulated waveform 2 of 8t DFF

Fig. 7: Shows the Simulated waveform 3 of 5t DFF

Fig. 8: Shows simulated waveform 4 of proposed 5t DFF

From table (2) observe that sleepy keeper and forced sleep techniques also report the better power reduction. From the results, it is observed that, proposed 5T-TSPC D-flip-flop architecture has the better percentage of average power reduction for 3 cases (ST(30%), FTS (28%) and SK(23%)) and also in the case of leakage power reduction, 5T-DFF has better results for 3 techniques.

V. CONCLUSION

In this paper performance analyses of different D-Flip-flop Circuits are presented. Proposed 5t DFF has lower power consumption compared to all other DFF, the efficiency of power reduction varies with different topology with different leakage reduction technique. Best average power reduction $p_{avg}$ (30%) and $p_{leak}$ (99.90%) is reported with sleep transistor.
technique, due to its power gating ability. Lowest 
Power (0.301uw) is reported ,and sleepy keeper and 
forced sleep also gives better results.  the election 
of leakage power reduction technique is dep ends upon 
topology and designing technology of DFF

TABLE 1

Performance analysis of different D flip flop 
Architectures

<table>
<thead>
<tr>
<th>CIRCUIT TYPE</th>
<th>POWER (uw)</th>
<th>DELAY (ns)</th>
<th>PDP (fj)</th>
<th>AREA (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12t DFF</td>
<td>9.909</td>
<td>1.000</td>
<td>9.909</td>
<td>336</td>
</tr>
<tr>
<td>8t DFF</td>
<td>6.709</td>
<td>0.047</td>
<td>0.307</td>
<td>228</td>
</tr>
<tr>
<td>Con. DFF</td>
<td>5.329</td>
<td>0.053</td>
<td>0.291</td>
<td>144</td>
</tr>
<tr>
<td>Pro. DFF</td>
<td>4.230</td>
<td>0.055</td>
<td>0.230</td>
<td>132</td>
</tr>
</tbody>
</table>

TABLE 2

Performance Analysys of Different Leakage Reduction 
Techniques on 5tDFF at 50nm Technology

<table>
<thead>
<tr>
<th>circuit</th>
<th>Power(uw)</th>
<th>Delay(ns)</th>
<th>pdp(fj)</th>
<th>Area(um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>base case</td>
<td>0.418</td>
<td>0.052</td>
<td>0.021</td>
<td>40</td>
</tr>
<tr>
<td>sleep transistor</td>
<td>0.301</td>
<td>4.028</td>
<td>1.513</td>
<td>60</td>
</tr>
<tr>
<td>sleepy stack</td>
<td>0.420</td>
<td>1.028</td>
<td>0.438</td>
<td>72</td>
</tr>
<tr>
<td>dual sleeps</td>
<td>0.375</td>
<td>1.425</td>
<td>0.605</td>
<td>72</td>
</tr>
<tr>
<td>dual stack</td>
<td>0.378</td>
<td>1.029</td>
<td>1.019</td>
<td>105</td>
</tr>
<tr>
<td>sleepy keeper</td>
<td>0.322</td>
<td>4.017</td>
<td>1.293</td>
<td>72</td>
</tr>
<tr>
<td>forced sleep</td>
<td>0.304</td>
<td>4.018</td>
<td>1.221</td>
<td>84</td>
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Implementation of Effects of the Partial Shading on PV Array Characteristics by MATLAB

G. Haritha & S. Thirumaliah
JNTUA, EEE Dept., St. Johns College of Engineering & Technology, Kurnool, India
E-mail: g_hari_g@yahoo.com, sampath.thirumalesh@gmail.com

Abstract – The performance of a photovoltaic (PV) array is affected by temperature, solar insolation, shading, and array configuration. Often, the PV arrays get shadowed, completely or partially, by the passing clouds, neighboring buildings and towers, trees, and utility and telephone poles. The situation is of particular interest in case of large PV installations such as those used in distributed power generation schemes. Under partially shaded conditions, the PV characteristics get more complex with multiple peaks. Yet, it is very important to understand and predict them in order to extract the maximum possible power. This paper presents a MATLAB-based modeling and simulation scheme suitable for studying the $I-V$ and $P-V$ characteristics of a PV array under a non-uniform insolation due to partial shading.

Keywords - Partial Shading, maximum power point tracking, MPPT, photovoltaic, PV, direct current, DC.

I. INTRODUCTION

With a spurt in the use of nonconventional energy sources, photovoltaic (PV) installations are being increasingly employed in several applications, such as distributed power generation and stand-alone systems. However, a major challenge in using a PV source is to tackle its nonlinear output characteristics, which vary with temperature and solar insolation. The characteristics get more complicated if the entire array does not receive uniform insolation, as in partially cloudy (shaded) conditions, resulting in multiple peaks. The presence of multiple peaks reduces the effectiveness of the existing maximum power point tracking (MPPT) schemes [1]–[3] due to their inability to discriminate between the local and global peaks. Nevertheless, it is very important to understand and predict the peaks. Nevertheless, it is very important to understand and predict the PV characteristics in order to use a PV installation effectively, under all conditions.

II. MODEL OF A PV ARRAY

A PV cell can be represented by an equivalent circuit, as shown in Fig. 1. The characteristics of this PV cell can be obtained using standard equations [4]. For simulating an entire PV array, the model of a PV module is developed first. Each PV module considered in this paper comprises 36 PV cells connected in series providing an open circuit voltage ($V_{oc}$) = 21 V and a short-circuit current ($I_{sc}$) = 3.74 A. The shading pattern for a large array is very complex to model.

A special categorization and terminology is used in this paper

Fig. 1. Equivalent circuit of a PV cell.

Fig. 2. PV array terminologies. (a) PV module. (b) Series-assembly with two series-connected
subassemblies S1 and S2. (c) Group. (d) PV array with groups G1 to G4. to describe the various components of a PV array. These are explained with the help of Fig. 2. A “subassembly” is formed with several series-connected PV modules receiving the same level of insolation. Several such series-connected subassemblies, each with a different level of insolation, form a series assembly [Fig. 2(b)]. Series assemblies, having similar shading patterns, form a “group” [Fig. 2(c)]. Various groups (with ith group represented by “Gi”), having different shading patterns and connected in parallel, form a PV array, as shown in Fig. 2(d).

III. SIMULATION PROCEDURE

This section describes the procedure used for simulating the $I-V$ and $P-V$ characteristics of a partially shaded PV array. It is important to understand how the shading pattern and the PV array structure are defined in MATLAB using the proposed scheme. This procedure consists of defining groups, assemblies, etc., for use with the MATLAB model developed corresponding to Fig. 2(d). This is explained with the help of illustration 1. To begin with, a simple case is considered with just two different shades on the PV array.

A. Illustration 1

Given a PV array consisting of 1000 PV modules arranged into 100 series assemblies, connected in parallel, each having 10 modules. It is desired to obtain the $I-V$ and $P-V$ characteristics of the various components (module through group, as described in Fig. 2) of this PV array, which consists of three groups with different insolation patterns, as given in Table I. Groups G1 through G3 have 40, 38, and 22 series assemblies, respectively. The complete PV array is shown in Fig. 3. As seen in Fig. 3,

### TABLE I

<table>
<thead>
<tr>
<th>Group</th>
<th>Number of unshaded modules in series assembly ($\lambda=1$)</th>
<th>Number of shaded modules in series assembly ($\lambda=0.1$)</th>
<th>No. of series assemblies in a group</th>
</tr>
</thead>
<tbody>
<tr>
<td>G1</td>
<td>4</td>
<td>6</td>
<td>40</td>
</tr>
<tr>
<td>G2</td>
<td>7</td>
<td>3</td>
<td>38</td>
</tr>
<tr>
<td>G3</td>
<td>10</td>
<td>0</td>
<td>22</td>
</tr>
</tbody>
</table>

$\lambda=$Solar insolation in kW/m².

only two different insolation levels are considered for simplicity. Shaded modules, receiving an insolation, $\lambda=0.1$ kW/m², are indicated in dark color. The aforementioned illustration explains the method and the format in which the input parameters are fed and the array configuration is described in the software to obtain the PV characteristics.

1) Effect of Bypass and Blocking Diodes on PV Characteristics:

Fig. 4 shows a PV array with bypass and blocking diodes connected in the array. It is important to note that the characteristics of an array with bypass and blocking diodes differ from that of an array without these diodes. The developed simulation tool has a provision to simulate the array characteristics, for any value of temperature, insolation, and for any array configuration, with and without the bypass and blocking diodes. Illustration 1 considers the case where bypass diodes are connected across every module and at
least one blocking diode is connected in series with each of the series assemblies, as shown in Fig. 4. To learn more on how the characteristics differ in these two cases, an illustration (Illustration 2) is included in a later section. Fig. 5 shows a screen shot of the MATLAB command window through which the given array configuration, temperature, and the insolation level(s) are described to the software. The matrix $U$ of size $G \times 3$, where $G$ is the number of groups, represents the array configuration. Each row indicates a group with a particular shading pattern on the series assemblies within that group.

The elements of each row represent the number of unshaded and shaded modules, respectively, in a series assembly, and the number of such series assemblies in the group. This implies that the first row of $U$ is same as the first row of Table I corresponding to $G_1$ and so on. “Diodes = 1” indicates the presence of bypass and blocking diodes, while their absence is indicated by entering “Diodes = 0.” “Highinsol” and “Lowinsol” are the insolation levels ($\lambda = 1$ and $\lambda = 0.1$ kW/m$^2$) on the unshaded and shaded modules, respectively. Similarly, “Thigh” and “Tlow” denote the working temperatures (in degrees Celsius) of the respective modules. Once the information is fed into the software, various windows pop up on the monitor, as shown in Fig. 6. These windows display the $I$–$V$ and $P$–$V$ characteristics of different components of the PV array described in Fig. 2.

The $I$–$V$ and $P$–$V$ characteristics of the two PV (shaded and unshaded modules of Fig. 3) modules at the same temperature but at different insolation levels are shown in Fig. 6. It is

Fig. 6. Characteristics of the PV modules under different insolation levels ($\lambda = 1$ and $\lambda = 0.1$ kW/m$^2$).
(a) $I$–$V$ characteristics. (b) $P$–$V$ characteristics.

Fig. 7. Characteristics of series assemblies with different insolation levels. (a) $I$–$V$ characteristics. (b) $P$–$V$ characteristics.
assumed that a shaded module consists of at least three shaded cells displaying the characteristics shown in Fig. 6(a) and (b). If these two PV modules are connected in series, they will conduct the same current, but the voltage across them will be different. In order to obtain the $I-V$ characteristics of the series-connected modules (series assembly) conducting a current $I_o$, the voltages across these modules, $V_1$ and $V_2$, are added to determine the resultant output voltage. The characteristics for series assembly are, thus, obtained internally by the software by applying similar procedure at all the points on the $I-V$ curve of the series-connected modules. Fig. 7 shows the resulting characteristics of series assemblies C1, C2, and C3 belonging to groups G1, G2, and G3, respectively.

(b) $P-V$ characteristics. If similar series assemblies having identical insolation patterns are connected in parallel to form a group, the current output is multiplied, but there is no change in the output voltage. Fig. 8 shows the characteristics of these groups. To obtain the overall resultant characteristics of all these groups (i.e., of the entire array), a common voltage is considered, while the current output of each of these groups is added to obtain the resultant current. The resultant characteristics of the PV array are shown in Fig. 9.

IV. SIMULATION RESULTS WITH THE PROPOSED MODEL

This section describes the usefulness of the proposed simulation model in simulating and understanding the effect of bypass and blocking diodes, array configuration,

Fig. 7. Results of the entire array considered in illustration 1. (a) $I-V$ characteristics. (b) $P-V$ characteristics.

Fig. 8. Output characteristics of the groups (parallel-connected series assemblies). (a) $I-V$ characteristics.

Fig. 9. Output characteristics of the entire array considered in illustration 1. (a) $I-V$ characteristics. (b) $P-V$ characteristics.

varying insolation level(s), and different shading pattern(s) on the global peak power and its position. This is studied with the help of illustrations 2, 3, and 4, given next.

Illustration 2

The effect of the bypass and blocking diodes on the PV characteristics under partially shaded conditions has been simulated for the array described in Table 1. The curves C1, C2, and C3, in Fig. 10, represent the $I-V$ and $P-V$ characteristics of the array in the following three cases, respectively: 1) under uniform insolation ($\lambda = 1$ kW/m$^2$); 2) under partially shaded condition ($\lambda = 1$ kW/m$^2$); and 3) under blocking condition ($\lambda = 0$ kW/m$^2$).
and $\lambda = 0.1 \, \text{kW/m}^2$ and without diodes; and 3) under partially shaded condition as in case (2), but with diodes.

It is seen from the $I$–$V$ characteristics shown in Fig. 10(a) that the presence of bypass diodes will allow the unshaded modules of all the series assemblies to conduct their maximum current at a given insolation and temperature. On the other hand, if the bypass diodes are not present, the shaded modules will limit the current output of the unshaded modules of the series assembly. This may not only lead to a thermal destruction of the PV modules but may also decrease the available output power from the PV array. The blocking diodes will prevent the reverse current through the series assemblies, which generate lower output voltage as compared to the others connected in parallel. This reverse current may cause excessive heat generation and thermal breakdown of PV modules. Fig. 10 reveals that the array having these diodes introduces multiple steps in the $I$–$V$ characteristics

Table III presents the PV array configuration to study the global peak and its position.

<table>
<thead>
<tr>
<th>Group</th>
<th>U</th>
<th>S</th>
<th>Ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>G1</td>
<td>3</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>G2</td>
<td>5</td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td>G3</td>
<td>6</td>
<td>4</td>
<td>20</td>
</tr>
<tr>
<td>G4</td>
<td>8</td>
<td>2</td>
<td>20</td>
</tr>
<tr>
<td>G5</td>
<td>10</td>
<td>0</td>
<td>20</td>
</tr>
</tbody>
</table>

Fig. 11. $P$–$V$ curves showing the effect of array configuration. “C$i$” implies a curve for the $i$th configuration of Table II.

It is desired to investigate the $P$–$V$ curves of this array as the insolation changes in steps of 0.15 kW/m$^2$. The response is shown in Fig. 12.

Fig. 12 shows the resulting $P$–$V$ characteristics at various insolation levels. It is observed that the number of prominent peaks increases with decrease in the insolation.

Fig. 10. Three different cases discussed in illustration 2. (a) $I$–$V$ curves. (b) $P$–$V$ curves.

and multiple peaks in the $P$–$V$ characteristics, under the partially shaded conditions.
inverter, is used to feed the power generated by the PV array to the grid and grid-connected loads. The conventional hill climbing method is used for MPPT. The performance of this method, in tracking global MPP, is tested for two different cases for an array given in Table I (illustration 2): 1) under uniform insolation (\( \lambda = 1 \text{ kW/m}^2 \)) and 2) under partially shaded condition (\( \lambda = 1 \text{ and } \lambda = 0.1 \text{ kW/m}^2 \)). It is assumed that the array initially receives uniform insolation of \( \lambda = 1 \text{ kW/m}^2 \) [case 1]. A step change in insolation level (from \( \lambda = 1 \text{ and } \lambda = 0.1 \text{ kW/m}^2 \)) is considered at \( t = 0.3 \text{ s} \) that causes partial shading of the array [case 2].

**Fig. 16.** System configuration for PV-based system feeding power into the grid

**Fig. 17.** (a)–(c) Output voltage, current, and output power from the PV array. (d) Output voltage of the boost converter (illustration 6).

It can be observed from Fig. 18 that no power is transferred to the grid, after \( t = 0.8 \text{ s} \). In fact, the grid has to supply the power. If the grid is replaced by a weak source, it may lead to a collapse of the system.

**Fig. 18.** (a) Variation in the load current \( I_L \). (b) Current fed from inverter \( I_{in} \). (c) Grid current \( I_g \) (illustration 6).

**Fig. 19.** Experimental setup for validation of the model.

**Fig. 20.** Simulation and experimental results on the test setup. (a) \( I-V \) characteristics. (b) \( P-V \) characteristics.

Fig. 20 shows the simulated and experimental results. Fig. 20 shows the characteristics of the PV array used for experiments. As expected and discussed in illustration 2, the presence of diodes introduces an additional peak in the \( P-V \) characteristic and generates more output power compared to the case where the diodes are absent.
V. CONCLUSION

A method to obtain the \( I-V \) and \( P-V \) characteristics of a PV array, having a large number of series- and/or parallel-connected modules under partially shaded conditions is described. The PV curves show multiple peaks under partially shaded conditions. The existing MPPT schemes, which assume a unique maximum power point, therefore, remain inadequate. The magnitude of the global peak is dependent on the PV array configuration and shading pattern besides the commonly known factors, i.e., insolation level and temperature.

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Leakage Power Reduction in CMOS Circuits using Leakage Control Transistor Technique in Nanoscale Technology

B. Dilip¹, P. Surya Prasad² & R. S. G. Bhavani³
¹²Dept. of ECE, MVGR college of Engineering, Vizianagaram, AP, India
³Dept. of ECE, JNTU Kakinada, AP, India
E-mail : dil.bagadi@gmail.com¹, suryaprasadp@yahoo.com², bhavani.rsg@gmail.com³

Abstract – In CMOS circuits, as the technology scales down to nanoscale, the sub-threshold leakage current increases with the decrease in the threshold voltage. LECTOR, a technique to tackle the leakage problem in CMOS circuits, uses two additional leakage control transistors, which are self-controlled, in a path from supply to ground which provides the additional resistance thereby reducing the leakage current in the path. The main advantage as compared to other techniques which involves the sleep transistor is that LECTOR technique does not require any additional control and monitoring circuitry, thereby limits the area increase and also the power dissipation in active state. Along with this, the other advantage with LECTOR technique is that it does not affect the dynamic power which is the major limitation with the other leakage reduction techniques.

Keywords - subthreshold leakage current; transistor stacking; self-controlled LCTs; deep-submicron.

I. INTRODUCTION

The rapid progresses in semiconductor technology have leaded the feature sizes to be shrunk through the use of deep-submicron processes; thereby the extremely complex functionality is enabled to be integrated on a single chip. In the growing market of mobile hand-held devices used all over the world today, the battery-powered electronic system forms the backbone. To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers has to be realized with very low power requirements. With miniaturization and the growing trend towards wireless communication, power dissipation has become a very critical design metric. The longer the battery lasts, the better is the device.

The power dissipation has not diminished even with the scaling down of the supply voltage. The problem of heat removal and power dissipation is getting worse as the magnitude of power per unit area has kept growing. For the rapid increase in power consumption of present day chips, the innovative cooling and packaging strategies are of little help. Also, the cost associated with the packaging and the cooling of such devices is becoming prohibitive. In addition to cost, the issue of reliability is a major concern. Component failure rate roughly doubles for every 10°C increase in operating temperature. With the on-chip devices doubling every two years, minimizing the power consumption has become currently an extremely challenging area of research.

Leakage power of a CMOS transistor depends on gate length and oxide thickness [4]. To decrease the dynamic power, the supply voltage is decreased which leads to the performance degradation. To speed up the device, the threshold voltage should also be scaled down along with the supply voltage, which results in exponential increase in the sub-threshold leakage current, thereby increase in the static power dissipation. The main components of leakage current in a MOS transistor are shown in Figure 1.

Fig. 1 : Static CMOS leakage sources.
The leakage power in a CMOS is due to sub-threshold leakage current; which is the reverse current flowing through the OFF transistor, indicated with arrows in Figure 2. As the technology scales down which is the shrinking of feature size of transistor, the channel length decreases, thereby increasing the amount of leakage power in the total power dissipated as shown in Figure 3.

![CMOS Inverter Diagram](image)

**Fig. 2 : Reverse current in CMOS inverter**

The leakage power in a CMOS is due to sub-threshold leakage current; which is the reverse current flowing through the OFF transistor, indicated with arrows in Figure 2. As the technology scales down which is the shrinking of feature size of transistor, the channel length decreases, thereby increasing the amount of leakage power in the total power dissipated as shown in Figure 3.

![Technology Vs Leakage Power](image)

**Fig. 3 : Technology Vs Leakage Power.**

### II. LIMITATIONS WITH RELATED WORK

#### A. MTCMOS

A high-threshold NMOS gating transistor is connected between the pull-down network and the ground, and low-threshold voltage transistors are used in the gate. The reverse conduction paths exist, which tends the noise margin to reduce or may result in complete failure of the gate. There also exists a performance penalty due to the high-threshold transistors in series with all the switching current paths.

Dual $V_T$ technique is a variation in MTCMOS, in which the gates in the critical path use low-threshold transistors and high-threshold transistors for gates in non-critical path [3], [7]. Both the methods requires additional mask layers for each value of $V_T$ in fabrication, which is a complicated task depositing two different oxides thickness, hence making the fabrication process complex. The techniques also suffer from turning-on latency i.e., the idle subsections of circuit cannot be used immediately after reactivated since some time is needed to return to normal operating condition. The latency is typically a few cycles for former method, and for Dual technology, is much higher. When the circuit is active, these techniques are not effective in controlling the leakage power.

#### B. SLEEP Transistor Technique

This is a State-destructive technique which cuts off either pull-up or pull-down or both the networks from supply voltage or ground or both using sleep transistors. This technique is MTCMOS, which adds high-$V_{th}$ sleep transistors between pull-up networks and $V_{dd}$ and pull-down networks and ground while for fast switching speeds, low-$V_{th}$ transistors are used in logic circuits [8]. Isolating the logic networks, this technique dramatically reduces leakage power during sleep mode. However, the area and delay are increased due to additional sleep transistors. During the sleep mode, the state will be lost as the pull-up and pull-down networks will have floating values. These values impact the wakeup time and energy significantly due to the requirement to recharge transistors which lost state during sleep.

#### C. Forced Stack

In this technique, every transistor in the network is duplicated with both the transistors bearing half the original transistor width [6]. Duplicated transistors cause a slight reverse bias between the gate and source when both transistors are turned off. Because sub-threshold current is exponentially dependent on gate bias, it obtains substantial current reduction. It overcomes the limitation with sleep technique by retaining state but it takes more wakeup time.

#### D. ZIGZAG Technique

Wake-up cost can be reduced in zigzag technique but still state losing is a limitation. Thus, any particular
state which is needed upon wakeup must be regenerated somehow. For this, the technique may need extra circuitry to generate a specific input vector.

E. SLEEPY STACK Technique

This technique combines the structure of the forced stack technique and the sleep transistor technique. In the sleepy stack technique, one sleep transistor and two half sized transistors replaces each existing transistor [10]. Although using of $W0/2$ for the width of the sleep transistor, changing the sleep transistor width may provide additional tradeoffs between delay, power and area. It also requires additional control and monitory circuit, for the sleep transistors.

F. LEAKAGE FEEDBACK Technique

This technique is based on the sleep approach. To maintain logic during sleep mode, the leakage feedback technique uses two additional transistors and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage feedback. Performance degradation and increase in area are the limitations along with the limitation of sleep technique.

G. SLEEPY KEEPER Technique

This technique consists of sleep transistors connected to the circuit with NMOS connected to Vdd and PMOS to Gnd. This creates virtual power and ground rails in the circuit, which affects the switching speed when the circuit is active [9]. The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware capable of predicting the circuit states accurately, increasing the area requirement of the circuit. This additional circuit consumes power throughout the circuit operation to continuously monitor the circuit state and control the sleep transistors even though the circuit is in an idle state.

III. LECTOR TECHNIQUE

The effective stacking of transistors in the path from supply voltage to ground is the basic idea behind the LECTOR technique for the leakage power reduction. This is stated based on the observation from [1], [2] and [5] that “a state is far less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with only one OFF transistor in the path”. The number of OFF transistors is related to leakage power as shown in Figure 4.

In this technique, two leakage control transistors are introduced between pull-up and pull-down network within the logic gate (one PMOS for pull-up and one NMOS for pull-down) for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. This arrangement ensures that one of the LCTs always operates in its near cutoff region.

![Fig. 4: Transistor-stacking Vs Leakage Power.](image)

![Fig. 5: LECTOR CMOS Gate](image)
Leakage Control Transistor (LECTOR) technique is illustrated in detail with the case of an inverter. A LECTOR INVERTER is shown in Figure 6. A PMOS is introduced as LCT1 and a NMOS as LCT2 between N1 and N2 nodes of inverter. The output of inverter is taken from the connected drain nodes LCT1 and LCT2. The source nodes of LCT1 and LCT2 are the nodes N1 and N2 respectively of the pull-up and the pull-down logic. The gates of LCT1 and LCT2 are controlled by the potential at source terminal of LCT2 and LCT1 respectively. This connection always keeps one of the two LCTs in its near cutoff region for any input.

When $V_{dd} = 1V$, input A = 0, the voltage at the node N2 is 800 mV. LCT1 cannot be completely turned OFF as the voltage is not sufficient. Hence, the LCT1 resistance will be near to but slightly lesser than it’s OFF resistance, allowing conduction. The resistance provided by LCT1, even though not equal to the OFF resistance, increases the resistance in the path of supply voltage to ground, thereby reducing the sub-threshold leakage current, attaining reduction in leakage power.

Similarly, when input A = 1, the voltage at the node N1 is 200 mV; hence LCT2 will be operated in near cutoff state. The states of all the transistors in the LECTOR inverter for all possible inputs are tabulated in Table I.

<table>
<thead>
<tr>
<th>Transistor Reference</th>
<th>Input Vector (A)</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>ON State</td>
<td>OFF State</td>
<td></td>
</tr>
<tr>
<td>M2</td>
<td>OFF State</td>
<td>ON State</td>
<td></td>
</tr>
<tr>
<td>LCT1</td>
<td>Near Cut-OFF State</td>
<td>ON State</td>
<td></td>
</tr>
<tr>
<td>LCT2</td>
<td>ON State</td>
<td>Near Cut-OFF State</td>
<td></td>
</tr>
</tbody>
</table>

Along with the resistance in the path, the propagation delay of the gate also gets increased. The transistors of LCT inverter are sized such that the propagation delay is reduced or equal to its base case.

In the sleep related technique, the sleep transistors have to be able to isolate the power supply and/or ground from the rest of the transistors of the gate. Hence, they need to be made bulkier dissipating more dynamic power. This offsets the savings yielded when the circuit is idle. Sleep transistor technique depends on input vector and it needs additional circuitry to monitor and control the switching of sleep transistors, consuming power in both active and idle states. In comparison, LECTOR generates the required control signals within the gate and is also vector independent.

Two transistors are added in LECTOR technique in every path from $V_{dd}$ to gnd irrespective of number of transistors in pull-up and pull-down network. Whereas, forced stacks have 100% area overhead. The loading requirement with LCTs is a constant which is much lower. Whereas, the loading requirements with forced stacks depend on number of transistors added and are huge. Hence, the performance degradation is insignificant in the case of LECTOR, and we overcome the drawback faced by forced stack technique.

IV. APPLYING LECTOR TO CMOS Circuits

Various circuit applications of the LECTOR technique are explored in this section. The LECTOR technique is applied to the following CMOS circuits and also their respective base case are implemented to calculate the amount of leakage power reduced in LECTOR technique.

A. LECTOR based NAND gate
Leakage Power Reduction in CMOS Circuits using Leakage Control Transistor Technique in Nanoscale Technology

The 2-input CMOS NAND gate is shown in Figure 7 with the two LCTs added to pull-up and pull-down network between the Vdd and gnd path. The simulation waveforms of LECTOR NAND from Figure 8 show that the basic characteristics of NAND are retained by LECTOR NAND.

B. 4-input AND-OR-Invert

\[ Z = (A \cdot B) + (C \cdot D) \]

Fig. 9 : Four input AOI

The SCCG (static CMOS complex gate) implementation of a 4-input AOI is shown in Figure 9, through which the area overhead can be reduced. The LECTOR implementation here needs only two additional transistors to be placed between the pull-up and pull-down network at the node from which the output is taken.

Through the simulation waveforms shown in Figure 10, the characteristics of LECTOR AOI resemble the base case.

C. 4:1 Multiplexer

The gate level schematic of 4:1 multiplexer is shown in Figure 11. The LECTOR implementation involves the addition of two LCTs in each gate between the supply and ground path.
The simulation waveforms for full adder as shown in Figure 14, resembles the characteristics of conventional full adder.

V. EXPERIMENTAL RESULTS

The leakage power is measured using the HSPICE simulator. The results obtained through the technique for 2-input NAND gate is shown in Table III. Simulation for the 2-input NAND is performed by taking four different process parameters Viz. 180nm, 90nm, 65nm and 45nm.

<table>
<thead>
<tr>
<th>Technology</th>
<th>180nm</th>
<th>90nm</th>
<th>65nm</th>
<th>45nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.8V</td>
<td>1.2V</td>
<td>1.1V</td>
<td>1V</td>
</tr>
<tr>
<td>NMOS $V_T$ (V)</td>
<td>0.3999</td>
<td>0.2607</td>
<td>0.22</td>
<td>0.1711</td>
</tr>
<tr>
<td>PMOS $V_T$ (V)</td>
<td>-0.42</td>
<td>-0.303</td>
<td>-0.22</td>
<td>-0.1156</td>
</tr>
</tbody>
</table>

The supply voltages to be considered for the four process parameters (technologies) along with the threshold voltages for NMOS and PMOS in the respective technologies are as shown in Table II.

**TABLE II. SUPPLY VOLTAGES AND THRESHOLD VOLTAGE VALUES**

<table>
<thead>
<tr>
<th>Technology</th>
<th>180nm</th>
<th>90nm</th>
<th>65nm</th>
<th>45nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leakage power (nW)</td>
<td>1.158</td>
<td>2.884</td>
<td>13.977</td>
<td>1503.66</td>
</tr>
<tr>
<td>%age decrease in power dissipation</td>
<td>19.035</td>
<td>42.883</td>
<td>15.313</td>
<td>24.514</td>
</tr>
</tbody>
</table>

Table IV gives the results for 4-input AOI for 90nm and 45nm technologies. Table V gives the results for 4:1 Multiplexer and Full Adder under 90nm process parameters.

**TABLE IV. RESULTS FOR 4-INPUT AOI**

<table>
<thead>
<tr>
<th>Leakage Power(W)</th>
<th>4-input AOI</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CONVENTIONAL</strong></td>
<td>3.76E-09</td>
</tr>
<tr>
<td><strong>LECTOR</strong></td>
<td>2.45E-09</td>
</tr>
<tr>
<td>Percentage decrease in Power Dissipation</td>
<td>34.914</td>
</tr>
</tbody>
</table>
TABLE V. RESULTS FOR 4:1 MULTIPLEXER AND FULL ADDER

<table>
<thead>
<tr>
<th>Leakage Power(nW)</th>
<th>4:1 Multiplexer</th>
<th>Full Adder</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONVENTIONAL</td>
<td>38.558</td>
<td>42.37</td>
</tr>
<tr>
<td>LECTOR</td>
<td>21.354</td>
<td>24.248</td>
</tr>
</tbody>
</table>

| Percentage decrease in Power Dissipation | 44.618 | 42.771 |

Leakage power dissipation is taken as the average of power dissipations obtained at all the possible input vectors of the CMOS circuit. There are 4 possible combinations for 2-input NAND, hence the average of the four power dissipations gives the leakage power. In the case of 4-input AOI, power dissipations corresponding to all the 16 combinations are averaged. For Multiplexer, the average of 64 power dissipations is considered and for full adder, the average of 8 power dissipations is considered to be as the static power dissipated. In each case, the leakage power is measured by exciting both the circuits (Conventional and LECTOR) with same set of input vectors.

VI. CONCLUSION

The increase in leakage power because of the scaling down of device dimensions, supply and threshold voltages in order to achieve high performance and low dynamic power dissipation, becomes more with the deep-submicron and nanometer technologies and thus it becomes a great challenge to tackle the problem of leakage power. LECTOR uses two LCTs which are self-controlled transistors. LECTOR achieves the reduction in leakage power like other leakage reduction techniques, such as sleepy stack, sleepy keeper, etc, along with the advantage of not affecting the dynamic power, since this technique does not require any additional control and monitor circuitry and also in this technique, the exact logic state is maintained.

The LECTOR technique when applied to generic logic circuits achieves up to 40-45% leakage reduction over the respective conventional circuits without affecting the dynamic power. A tradeoff between Propagation delay and area overhead exists here as the delay reduction by sizing the transistors will increase the area overhead.

REFERENCES

Design and Implementing of Serial Ports to Ethernet Gateway on Embedded System

R.V. Sonawane & A.A. Naik
Department of Electronics & Tele Communication, Maharashtra Institute of Technology, Pune, India
E-mail: rashmi_2711@yahoo.com, apurva.naik@mitpune.edu.in

Abstract – The use of the multi-serial/Ethernet conversion gateway simplifies the networked control and distributed management of information for serial devices. So the design of a new type of gateway for data converting from serial ports to Ethernet based on Embedded system is highlighted in this paper. The design is based on ARM7 (LPC2138) processor and serial ports to Ethernet data conversion gateway that will convert the serial data of various components to Ethernet data. The communication between the serial devices and monitor computer is simplified with the Ethernet protocol. Data transmission from number of serial devices used in industrial applications can be effectively achieved. The use of such system will improve the CPU efficiency of the system to ensure real-time data processing.

Keywords - Ethernet; gateway; ARM7; serial ports; TCP/IP protocol.

I. INTRODUCTION

There is a strong interest of using cheap and simple Ethernet technology for control networks. Its advantage of low price and robustness, resulting from its wide acceptance and deployment, has created an eagerness to meet the real time requirements.

Microcontrollers are low cost embedded systems that control and monitor no. of appliances. Enabling a microcontroller to a ubiquitous data communication network e.g the Ethernet network, will allow developers and end users to monitor and control microcontroller operated devices with greater flexibility.

The communications between existing computer monitor and equipment are all standard forms of asynchronous serial, the controller is connected with the various components by serial port expansion. The use of the process system makes frequent interruptions of the computer and greatly reduces the efficiency of the CPU. So a new type of system design based on Serial ports to Ethernet data conversion gateway, to convert the serial data of various components to Ethernet data, simplifying the communication between the various components and monitor computer only with the protocol of Ethernet.[1]

As seen in Fig. 1, the communication between the serial devices and computer takes place through the gateway. The gateway will send data from serial devices to the Computer and the control commands from the computer in the Ethernet format will be converted to serial frame format and then send to each serial device. [2]

![Fig. 1: System Diagram](image)

II. METHODOLOGY

The entire system will be designed using ARM development board and Ethernet development board. The functional diagram of the system is mainly divided into two main sections:

1) Hardware interface unit (RTL8019AS)
2) Processing unit (LPC2138)
Hardware interface unit (RTL8019AS):

An embedded system that supports Ethernet requires Ethernet controller and a cable to provide network interface. The board consists of Ethernet controller. It is complaint to Ethernet II and IEEE 802.3 10 base5, 10 base2, 10 baseT Ethernet interface.

Processing unit (LPC2138):

In the Ethernet capable embedded system a CPU manages communication with the Ethernet controller. The minimum requirement for the CPU is a microcontroller with external 8 bit data bus.

The Ethernet controller hardware normally handles the sending and receiving of frames including detecting collision and deciding when to try again after collision. The CPU writes the data to send into memory that the CPU can access and the controller stored the received data in the memory that the CPU can access.

The system is based on high-speed Ethernet communication technique and Real-time Operating System (RTOS). It is a serial equipment which incorporates Ethernet with serial data transmission. [2]

The design is based on ARM7 (LPC2138) processor and serial ports to Ethernet data conversion gateway that converts the asynchronous serial data of various components to Ethernet data. ARM7 microprocessor (LPC2138) is used and its parallel port is expanded for communication using Quad UART (ST16C554) with serial ports data. RTL8019 is a highly integrated Ethernet Controller used for connecting the ARM board to the Ethernet port of the PC. The processor will take the data from the RTL8019 decode it and accordingly send it to the corresponding PC.[3]

The project consists of two primary elements

1) server consisting of ARM7 microcontroller, LPC2138, interfaced with Ethernet IC, Realtek RTL8019AS and
2) no. of serial devices connected to the system through Quad UART.

The serial devices send/receive data to/from the microcontroller using TCP packets. The transfer speed of Ethernet has developed to 10Gbps from initial 10Mbps.

III. HARDWARE DESIGN

The hardware consists of ARM Processor (LPC2138), Ethernet Controller (RTL8019) and Quad UART (ST16C554).

The Ethernet controller hardware normally handles the sending and receiving of frames including detecting collision and deciding when to try again after collision. The CPU writes the data to send into memory that the CPU can access and the controller stored the received data in the memory that the CPU can access. [5]

The LPC2138 microcontrollers are based on a 16/32-bit ARM7TDMI-S CPU with real-time emulation and embedded trace support, that combine the microcontroller upto 512 kB of embedded high-speed flash memory. A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at maximum clock rate. 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty. Due to the low power consumption, these microcontrollers are ideal for applications where miniaturization is a key requirement.

Ethernet has become the most popular LAN scheme in last decade. It is simple, efficient, easily integration and bus based architecture is particularly used for wide applications. The system is based on high-speed Ethernet communication technique and Real-time Operating System (RTOS). It is a serial equipment which incorporates Ethernet with serial data transmission. [6]
In sending a frame, a controller will do the following:

1) Receives the message to send and destination address.
2) Calculates the Ethernet frame check sequence.
3) Places data, address and other information in the frames field.
4) Attempts to transmit the frame when the network is idle.
5) Half duplex interface detects collisions, cancels any transmitted frame with a collision and tries according to protocol standard IEEE802.3; in full duplex Ethernet segment does not need to support collision detecting because there are no collisions to detect.
6) Provides an indication of success or failure of a transmission.

In receiving a frame, a controller will do the following:

1) Detects and synchronizes to new received frames.
2) Ignores if any frames that is less than the minimum size.
3) Ignores if any frames that donot contain the interfaces address or a valid multicast or broadcast address in the Destination Address field.
4) Calculates the frame check sequence value, compares the result with the received value and indicates the errors if they dont match.
5) Makes the received frames data and other information available to the receiving computer and reads the data.

IV. SOFTWARE DESIGN

Description of Software

It mainly realizes conversion processing between serial data and Ethernet data. It can identify a serial port through IP address and the NO. of port. It is developed using Keil software. It includes RTL8019AS control functions and all needed communications (ARP, IP, TCP). [2]

Frame format

<table>
<thead>
<tr>
<th>Synchronous head 1</th>
<th>Synchronous head 2</th>
<th>data</th>
</tr>
</thead>
</table>

Fig. 3: Frame format of serial data

<table>
<thead>
<tr>
<th>Synchronous head 1</th>
<th>Synchronous head 2</th>
<th>Serial Number</th>
<th>data</th>
</tr>
</thead>
</table>

Fig. 4: Frame format of Ethernet data

The received data of serial device must go through as part of Ethernet frames after the package, and Ethernet must analyze all receive data, in which way control data will be accurately sent to each serial equipment, which requires the serial data frame and Ethernet data frame for a unified treatment. Ethernet transmits data using UDP communication protocol through IP address aiming at high stability. [4]

Fig. 5: Flowchart of the system

V. CONCLUSION

The paper proposes embedded system architecture based on real-time Ethernet. It will provide a uniform environment for integration of real-time control and information exchange. Using Ethernet as the communications backbone for the embedded systems has several advantages. In recent years, Ethernet network protocol has been widely adopted as the choice method of data communication for personal computers and other digital devices. Its popularity is due to the immense use of the Internet, an information exchange infrastructure that communicates the data via the Ethernet network. Furthermore Ethernet is readily available on most of the currently deployed PCs as a data communication protocol. Such systems can be used in electric power net automatic system, transmission and distribution of electric power control system,
Internet/LAN based systems, long-distance video frequency transmission system, industry/factory's automatic system and SCADA system.

REFERENCES


Design and Implementation of Digital Signal
Oscilloscope using VHDL

Sarah Qurrat ul ain¹, Rajashree D.B² & Ajay Kumar D³
¹,²The Oxford College of Science, Bangalore-02, India
³The BMS College of Engineering, Bangalore-19, India
E-mail : qurrat.iqbal13@gmail.com¹, rajashree.raj12@gmail.com², d.ajay402@gmail.com³

Abstract – The objective is to design and Implement a low cost, high performance, single channel Digital Storage Oscilloscope (DSO). Analog to Digital Converter (ADC), Digital to Analog Converter (DAC) are of prime important to interface with the real world signals, hence interfacing them is primary aim of this paper which intern help us in using the real-world signals for our use and further processing if required to extract vital information. These control units of DSO are designed and implemented using a Field Programmable Gate Array (FPGA) making the system flexible and cost effective.

Keywords - DSO, VHDL, FPGA, ADC, DAC, SPI.

I. INTRODUCTION

The aim of the project is to design a PC based Digital Storage Oscilloscope (DSO). A standard oscilloscope displays the changes in a voltage over time, as the display is continuously updated with the current state of the input signal. A standard oscilloscope is of limited use for non-repeating signals or for observing signal glitches.

A storage scope is more useful as it captures and stores the signal. Which can then be displayed to the user. Because the screen is not continuously refreshed with the current state of the signal the scope can be used to analyse non-repeating signals and signal glitches. Both analog storage and digital storage scopes are available, with digital scopes being by far the most common. A Digital Storage Oscilloscope (DSO) uses digital memory to store a waveform. In order to do this the incoming signal must first be digitised, once this is complete the data in the memory can be continuously replayed through a digital to analog converter and displayed on a CRT. Unlike a normal oscilloscopes which uses an electron beam, which is swept across a phosphor screen, the vertical deflection of the beam being proportional to input voltage. Areas of the screen that are bombarded by the electron beam will emit light, resulting in an image that shows the waveform of the input signal. Analog storage scopes use a specially modified cathode ray tube (CRT) to store the signal.

II. BLOCK DIAGRAM

A. Clock Synthesizer:

This block gets the input from the crystal. The crystal operates at 3.3 volts and produces 50MHz frequency. By making use of this fundamental frequency, we generate frequencies ranging from 20MHz to 2Hz using a 32-bit counter. Thus the required frequency is selected by Multiplexer using select lines. The MUX used here is a 32*1. The RTL synthesis view of clock synthesizer is shown in the figure 2.
B. **ADC Control Block:**

An analog to digital converter is an electronic circuit which transforms a signal from analog (continuous) to digital (discrete) form. The need for analog to digital converter is that when the signals are in digital form they are susceptible to deleterious effects of additive noise.

The FPGA board consists of two channel Analog-Capture circuit consisting of programmable pre-amplifier and analog to digital converter. The analog-capture circuit consists of Linear Technology LTC6912-1 programmable pre-amplifier that scales the incoming input signal (Programmable Gain Amplifiers are programmable on a SPI bus and thus add gain control and input channel selection to the embedded control system). This PGA’s are optimized for high speed, low offset voltage and single supply operation. The LTC6912-1 provides two independent inverting amplifiers with programmable gain. The purpose of the amplifier is to scale the incoming voltage VINA and VINB (pins of ADC on FPGA) so that it maximizes the conversion rate of the DAC. The gain of each amplifier is programmable from -1 to -100 which enable signals as small as ±12.5mV to apply full scale inputs to the A/D converters.

The output of a pre-amplifier connects to a linear technology LTC1407A-1 ADC. The LTC1407A-1 provides two analog to digital converters. Both analog inputs are sampled simultaneously when AD_CONV signal is applied. The analogue input range is ±1.25v relative to 1.65v. Both the pre-amplifier and ADC are serially programmed or controlled by FPGA and digital values to be read. The ADC is 32-bit wide, having two channels of 14-bit each and the maximum sample rate is 1.5MHz. The RTL synthesis view of ADC controller and the simulated waveform is shown in figure (3) and figure (4).
C. Dual Port RAM:

Dual-ported RAM (DPRAM) is a type of Random Access Memory that allows multiple reads or writes to occur at the same time and at different memory cells at different addresses. The dual-ports offer high-bandwidth communication between processors, they also provide the flexibility that is often required in fast-evolving design environments. The performance of these dual-ports is highly dependent on device utilization and how memory blocks are instantiated.

The Spartan 3E FPGA board used here includes 512Mbits micron technology DDR SDRAM with a 16-bit data interface. We have written a VHDL code, wherein 512 bits of data is read and written. The RTL synthesis block diagram of Dual Port RAM and the simulated waveform for both data read and data write is shown in the figures 5, 6 and 7.

D. Digital to Analog Converter

Digital to analog conversion is the process of changing one of the characteristics of an analog signal based on the information on digital data. The Spartan-3E FPGA Starter Kit board includes an SPI-compatible, four-channel, serial Digital-to-Analog Converter (DAC). The DAC device is a Linear Technology LTC2624 quad DAC with 12-bit unsigned resolution.

Inside the D/A converter, the SPI interface is formed by a 32-bit shift register. Each 32-bit command word consists of a command, an address, followed by data value. The FPGA first sends eight dummy or “don’t care” bits, followed by a 4-bit command. The most commonly used command with the board is COMMAND [3:0] = “0011”, which immediately updates the selected DAC output with the specified data value. Following the command, the FPGA selects one or all the DAC output channels via a 4-bit address field. Following the address field, the FPGA sends a 12-bit
unsigned data value that the DAC converts to an analog value on the selected output(s). Finally, four additional dummy or don’t care bits pad the 32-bit command word. DAC output level is the analog equivalent of a 12-bit unsigned digital value, D[11:0], written by the FPGA to the DAC via the SPI interface. The RTL view of DAC is shown in figure 8.

E. Serial Peripheral Interface(SPI)

The SPI bus is a full-duplex, synchronous, character-oriented channel employing a simple four-wire interface. They are widely used to provide economical board-level interface between devices such as microcontrollers, DACs, ADCs and others. A SPI system consists of a master and one or more slaves where a master is a microcomputer and slave is any integrated circuit which receives clock from the master. As each bit is transmitted by the master, the slave also transmits a bit allowing one byte to be passed in each direction at the same time. All SPI transfers are full-duplex where an 8-bit data character is transferred from the master to the slave and an independent 8-bit data character is transferred from the slave to the master. This can be viewed as a circular 16-bit shift register, an 8-bit shift register in the SPI master device and another 8-bit shift register in a SPI slave device that are connected.

The Spartan 3e FPGA board includes a 16Mbit SPI serial flash, useful in variety of application. It provides an alternative means to configure FPGA. For example, a bus master-the FPGA drives the bus clock signal (SPI_SCK) and transmits serial data (SPI_MOSI) to the selected bus slave-the DAC. At the same time, the bus slave provides serial data (SPI_MISO) back to the bus master. The SPI bus signals are shared by other devices on the board. It is vital that other devices are disabled when the FPGA communicates with the Amplifier, ADC or DAC to avoid bus contention. Each bit is transmitted or received relative to the SCK clock.

III. CONCLUSION

The design of ADC and DAC Controllers for the LTC1407A and LTC2624 are written using VHDL and Implemented on FPGA. All the designs use State machine approach for controllers. Designed clock synthesizer will cater clocking needs of all the system. The sampled Digital data is stored in a designed DPRAM of depth 512. Entire controlling is done by the designed DSO Control unit.

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Vector Control Scheme for Induction Motor with Different Controllers for Neglecting the End Effects in HEV applications

M.LakshmiSwarupa¹, G.TulasiRamDas² & P.V.RajGopal³

¹Malla Reddy Engineering College, ²JNTUK & ³BHEL R&D
E-mail : swarupamalladi@gmail.com¹, das_tulasiram@yahoo.co.in² & pv_rajgopal@bhelrnd.co.in³

Abstract - This paper develops the application of different control strategies to the vector control of the voltage-fed induction motor. The proposed model decomposes the control task into three loops, namely, the speed loop, the d-axis flux loop and the q-axis flux loop. Then, tracking of speed with different controllers is designed for each loop. Proportional-Integral update laws are used to adjust the control parameters, which increases the tracking performance (Z-N Method). Simulations are obtained shows good robustness against parameter variations, high tracking performance and simplicity of implementation.

Keywords - Induction motor, vector control, Proportional Integral Derivative controller, Neural Network controllers.

I. INTRODUCTION

Even though it requires highly much more complex control strategies, the induction machine is traditionally and for a long time used in fixed speed applications for reasons of cost, efficiency, reliability and size. when compared with the AC machine, DC machine for a variable speed application is required, appears to be the most appropriate electromechanical device where torque and flux are naturally decoupled and can be controlled independently, thus allowing a fast torque response and high precision of speed regulation to be achieved.

The vector control for induction motors was introduced for the first time by Blaschke in the early 1970s [1]. The main objective of this control method is, as in separately excited DC machines, to independently control the speed, torque and the flux; this is done by choosing d–q rotating reference frame synchronously with the rotor flux space vector (or stationary frame). Once the orientation is correctly obtained, the torque is controlled by the torque producing current, which is the q-component of the stator current space vector. At the same time, the flux is controlled by the flux producing current, which is the d-component of the stator current space vector. If the electrical parameters set in the field-orientation scheme cannot be tuned according to their actual values, the torque generating characteristics will become sluggish and oscillatory (since highly sensitive)[5]. On the other hand, in many industrial applications the drive operates under a wide range of varying load characteristics and the mechanical system parameters vary substantially.

In order to cope with the problems mentioned above, various, vector control schemes with fuzzy estimation (AI) of the induction motor parameters were developed. In recent years, the reference model controls for dynamic systems have been a topic of considerable interest. Thus, the application of the fuzzy logic control to the induction motor drive was only considered for the speed control due to the linearity of the mechanical part, and facility to realize matching conditions by conventional controllers.
Based on soft computing technique, this paper proposes a new robust architecture to realize vector control of the induction motor drive. The control problem is namely, the speed loop, the d-axis flux loop and the q-axis loop. Then, for each subsystem, an control input is designed to achieve the tracking objective with compensation of the coupling due to the other loops.

The major contributions of the work presented in this paper are: (1) considering the whole voltage-fed drive dynamics, ie, no simplification is made, which permits mastering of both the transient and steady state dynamics (2) considering all the electrical and mechanical parameters as unknown, and designing the control loops to account for this situation; (3) Proportional-Integral update laws are used to tune the control parameters, which, compared with simple Integral update laws, provides faster tracking and convergence performance.

This paper is organized as follows. In Section 2, we briefly review the voltage-fed induction motor model and the vector control principle. The proposed control of the induction motor speed and fluxes is discussed.

II. INDUCTION MOTOR MODEL

The Voltage-fed induction motor model established in d-q synchronously rotating frame is given by the following equations

\[
\begin{align*}
\dot{\psi}_d &= -\omega \psi_d + \omega_d \psi_q + \beta I_d \\
\dot{\psi}_q &= -\omega \psi_q - \omega_d \psi_d + \beta I_q \\
\dot{\omega} &= -\omega + \left( \mu (\psi_d I_q - \psi_q I_d) - T_I \right)
\end{align*}
\]

where $\omega$ is the electrical rotor speed; $\omega_d$ is the slip frequency; $I_d, I_q$ are the d, q axis stator currents; $\psi_d, \psi_q$ are the d, q axis flux rotors; $R_s$ is the rotor resistance; $L_r$ is the rotor inductance; $M$ is the mutual inductance; $J$ is the moment of inertia; $f$ is the viscosity coefficient; $P$ is the number of pairs of poles; $T_I$ is the load torque; $\alpha = R_s/L_r$ is the rotor time constant, $\beta = \omega M, \mu = P M/L_r, a = f/J$ and $b = P/J$.

In the vector control, speed is controlled by the torque producing current $I_q$ to track the speed reference command. The d-axis flux is forced to follow some reference flux command using the flux producing current $I_d$. Further, the slip frequency $\omega_d$ is used as the third control input to force the q-axis flux to zero, i.e to achieve the correct flux orientation.

III. DESIGN OF PID CONTROLLERS

The characteristics of the each of proportional (P), the integral (I), and the derivative (D) controls, and how to use them to obtain a desired response. In this paper following unity feedback system is considered:

![Fig2:PID controller]

Plant: A system to be controlled Controller: Provides the excitation for the plant; Designed to control the overall system behavior.

A. The three-term controller

The transfer function of the PID controller looks like the following:

\[
\frac{K_p u + \frac{1}{s} K_i}{s} + \frac{K_d}{s^2} = \frac{K_e}{s} \tag{4}
\]

Kp = Proportional gain
KI = Integral gain
Kd = Derivative gain

First, considering the PID controller working principle in a closed-loop system using the schematic shown above. The variable $e$ represents the tracking error, the difference between the desired input value (R) and the actual output (Y). This error signal $e$ will be sent to the PID controller, and the controller computes both the derivative and the integral of this error signal. The signal $u$ past the controller is now equal to the proportional gain (Kp) times the magnitude of the error plus the integral gain (Ki) times the integral of the error plus the derivative gain (Kd) times the derivative of the error.

\[
u = K_pe + K_i \int e dt + K_d \frac{de}{dt} \tag{5}
\]

This signal $u$ will be sent to the plant, and the new output (Y) will be obtained. This new output (Y) will be sent back to the sensor again to find the new error signal (e). The controller takes this new error signal and
computes its derivative and its integral again. This process goes on and on.

B. The characteristics of P, I, and D controllers

A proportional controller (Kp) will have the effect of reducing the rise time and will reduce, but never eliminate, the steady. An integral control (Ki) will have the effect of eliminating the steady-state error, but it may make the transient response worse. A derivative control (Kd) will have the effect of increasing the stability of the system, reducing the overshoot, and improving the transient response. Effects of each of controllers Kp, Kd, and Ki on a closed-loop system are summarized in the table shown below.

<table>
<thead>
<tr>
<th>CL response</th>
<th>Rise time</th>
<th>Overshoot</th>
<th>Settling time</th>
<th>S-s error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kp</td>
<td>Decrease</td>
<td>Increase</td>
<td>Small Change</td>
<td>Decrease</td>
</tr>
<tr>
<td>Ki</td>
<td>Decrease</td>
<td>Increase</td>
<td>Increase</td>
<td>Eliminate</td>
</tr>
<tr>
<td>Kd</td>
<td>Small Change</td>
<td>Decrease</td>
<td>Decrease</td>
<td>Small Change</td>
</tr>
</tbody>
</table>

Table 1: Comparison between controllers

A PI controller responds to an error signal in a closed control loop and attempts to adjust the controlled quantity to achieve the desired system response. The controlled parameter can be any measurable system quantity such as speed, torque, or flux. The benefit of the PI controller is that it can be adjusted empirically by adjusting one or more gain values and observing the change in system response.

A digital PI controller is executed at a periodic sampling interval. It is assumed that the controller is executed frequently enough so that the system can be properly controlled. The error signal is formed by subtracting the desired setting of the parameter to be controlled from the actual measured value of that parameter. The sign of the error indicates the direction of change required by the control input. The Proportional (P) term of the controller is formed by multiplying the error signal by a P gain, causing the PI controller to produce a control response that is a function of the error magnitude.

As the error signal becomes larger, the P term of the controller becomes larger to provide more correction. The effect of the P term tends to reduce the overall error as time elapses. However, the effect of the P term reduces as the error approaches zero. In most systems, the error of the controlled parameter gets very close to zero but does not converge. The result is a small remaining steady state error.

The Integral (I) term of the controller is used to eliminate small steady state errors. The I term calculates a continuous running total of the error signal. Therefore, a small steady state error accumulates into a large error value over time. This accumulated error signal is multiplied by an I gain factor and becomes the I output term of the PI controller.

IV. TUNING OF PI CONTROLLERS

Proportional-integral (PI) controllers have been introduced in process control industries. Hence various techniques using PI controllers to achieve certain performance index for system response are presented. The technique to be adapted for determining the proportional integral constants of the controller, called Tuning, depends upon the dynamic response of the plant.

In presenting the various tuning techniques we shall assume the basic control configuration wherein the controller input is the error between the desired output (command set point input) and the actual output. This error is manipulated by the controller (PI) to produce a command signal for the plant according to the relationship.

\[ U(t) = K_p \left(1 - \frac{1}{\tau_p}\right) \]

Or in time domain

\[ U(t) = K_p \left[ e(t) + \int_{0}^{t} \frac{1}{\tau_i} de\right] \]

where \( K_p \) = proportional gain
\( \tau_i \) = integral time constant

If this response is S-shaped as in, Ziegler-Nichols tuning method is applicable.

Figure 3: S shaped response of the plant

Ziegler- Nichols Rules for tuning PI controllers:

First Rule: The S-shaped response is characterized by two constants, the dead time \( L \) and the time constant
$T$ as shown. These constants can be determined by drawing a tangent to the $S$-shaped curve at the inflection point and state value of the output. From the response of this nature the plant can be mathematically modeled as first order system with a time constant $T$ and delay time $L$ as shown in block diagram.

The gain $K$ corresponds to the steady state value of the output $C_{ss}$. The value of $K_p$, $T_i$ and $T_d$ of the controllers can then be calculated as below:

$$K_P = 1.2\left(\frac{T}{L}\right)$$

$$\tau_i = 2L$$

V. NEURAL NETWORKS BASED CONTROLLER

Neural networks can perform massively parallel operations. They exhibit fault tolerance since the information is distributed in the connections throughout the network[4]. By using neural PI controller the peak overshoot is reduced and the system reaches the steady state quickly when compared to a conventional PI controller.

Program for creating the Neural Network:

```matlab
load n
k1=max(i');
k2=max(o1');
P=i'/k1;
T=o1'/k2;
n=157128;
net = newff(minmax(P),[5 1],{'tansig' 'purelin'});
net.trainParam.epochs = 200;
net = train(net,P,T);
Y = sim(net,P);
plot (P,T,P,Y,'o')
gensim(net,-1)
```

VI. SIMULATION RESULTS

Specifications:

<table>
<thead>
<tr>
<th>Kp</th>
<th>Ki</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>1000</td>
</tr>
<tr>
<td>Rr=9.295e-3ohm</td>
<td>Lrl=0.3027e-3H</td>
</tr>
<tr>
<td>Rs=14.85e-3ohm</td>
<td>Lsl=0.3027e-3H</td>
</tr>
<tr>
<td>Lm=10.46e-3H</td>
<td>P=8</td>
</tr>
</tbody>
</table>

The simulation of Field Oriented control of induction motor is done by using MATLAB-SIMULINK. The results for the following different cases are studied.

Case-1: No Load Condition

Case-2: Step Change in Load

Case-3: Speed Reversal Command

The simulation results along with the relevant waveforms for on-road tested vehicle parameters are below:

Case-1: No Load Condition:
Vector Control Scheme for Induction Motor with Different Controllers for Neglecting the End Effects in HEV applications

**a. Torque Response**

![Figure 7: Torque (N-m) versus Time (Sec)](image)

**Reference Speed = 150 rad/sec**

![Figure 10 Speed (rpm) versus Time (Sec)](image)

**b. Speed Response**

Reference Speed=150 rad/sec

![Figure 8: Speed (rpm) versus Time (Sec)](image)

Case-2: Step Change in load
A load torque of 200 N-M is applied at t = 2 sec

![Figure 9: Torque (N-m) versus Time (Sec)](image)

![Figure 11: Torque (N-m) versus Time (Sec)](image)

Case-3: Speed Reversal Command
Speed reversal command is given at t = 2 sec. i.e. Speed is changed from 150 rad/sec to -150 rad/sec at t = 2 sec.

![Figure 12: Speed (rpm) versus Time (Sec)](image)

Speed and Torque characteristics of an Induction Motor using a conventional PI controller:
Vector Control Scheme for Induction Motor with Different Controllers for Neglecting the End Effects in HEV applications

Figure 13: Torque (N-m) versus Time (sec)

Speed and Torque characteristics of an Induction Motor using a conventional NN controller:

With and without end effects:

Figure 14: Speed (rpm) versus Time (Sec) With end effects

Figure 15: Magnified speed with end effects
Vector Control Scheme for Induction Motor with Different Controllers for Neglecting the End Effects in HEV applications

Figure 16: Magnified speed without end effects

Figure 17: Magnified thrust with end effects

Figure 18: Magnified Thrust without end effects

Figure 19: Current d-axis with end effects
REFERENCES


VII. CONCLUSIONS

A control schemes applied to vector control of an induction motor drive was presented in this. The overall speed and flux control system was verified to be globally stable and robust to the variations of motor mechanical and electrical parameters variations. Simulation results obtained in MATLAB-SIMULINK were used to demonstrate the characteristics of the proposed method. It is shown that the proposed Neural Network controller has better tracking performance and robustness against parameters variations as compared with the conventional controller.
## Mathematical Modelling and Simulation of Grid Connected Solar Photovoltaic System

K.N. Dinesh Babu¹, R. Ramaprabha² & V. Rajini³

¹University of Petroleum & Energy Studies, Dehradun, India
²&³SSN College of Engineering, Chennai, India
E-mail: dineshbabu.nagalingam@ge.com, ramaprabhar@ssn.edu.in & rajiniv@ssn.edu.in

### Abstract

This paper presents the mathematical modeling of three-phase grid connected inverter fed by Solar Photovoltaic (SPV) system with Maximum Power Point Tracking (MPPT). Analysis has been carried out to choose the proper modulation index for maximum output for three-phase inverter. With this modulation index, the variation of the active and reactive power for different loads has been presented along with major parameters like Transfer ratio and Efficiency. Also the Real and Reactive power output of the SPV has been measured with various solar Radiation levels.

### 1. INDEX TERMS

Solar Photovoltaic cell, Mathematical model, Three Phase Inverter, Grid Modelling, Transfer ratio, Efficiency.

### 2. NOMENCLATURE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Iₚₘ</td>
<td>Light current of SPV Module (A)</td>
</tr>
<tr>
<td>Iₜ</td>
<td>Diode reverse saturation current in the equivalent circuit (μA)</td>
</tr>
<tr>
<td>Rₛₑ</td>
<td>Series Resistance in the equivalent circuit of the module (mΩ)</td>
</tr>
<tr>
<td>Rₛₜ</td>
<td>Shunt Resistance in the equivalent circuit of the module (mΩ)</td>
</tr>
<tr>
<td>D</td>
<td>Diode used in the equivalent circuit</td>
</tr>
<tr>
<td>Iₛₜ</td>
<td>Current through the shunt resistance (mA)</td>
</tr>
<tr>
<td>Iₛₑ</td>
<td>Short circuit current of the module (A)</td>
</tr>
<tr>
<td>Vₛₑ</td>
<td>Open circuit voltage of the module (V)</td>
</tr>
<tr>
<td>Iₛₙ</td>
<td>Current flowing through inverter circuit (A)</td>
</tr>
<tr>
<td>Iₛₘ, Iₛₙ, Iₛₜ</td>
<td>Three phase output of Inverter</td>
</tr>
<tr>
<td>Sₚ, Sₛ, Sₜ</td>
<td>Switching pulse for individual phases of Inverter circuit</td>
</tr>
<tr>
<td>M,Ø</td>
<td>Modulation index and Phase angle</td>
</tr>
<tr>
<td>Iₚᵥ</td>
<td>Solar PV Module current (A)</td>
</tr>
<tr>
<td>Vₚᵥ</td>
<td>Solar PV Module voltage (V)</td>
</tr>
<tr>
<td>Kᵢ</td>
<td>Temperature co-efficient of short circuit current</td>
</tr>
<tr>
<td>Iₚᵥₙ</td>
<td>Photovoltaic current at nominal condition</td>
</tr>
<tr>
<td>Gₙ</td>
<td>Nominal insolation level (1000 W/m²)</td>
</tr>
<tr>
<td>Udc</td>
<td>Input DC voltage for Inverter (V)</td>
</tr>
<tr>
<td>Iₛₙₙ</td>
<td>Short circuit current at nominal condition</td>
</tr>
<tr>
<td>G</td>
<td>Insolation level W/m²</td>
</tr>
<tr>
<td>Vₐᵦ, Vₐᵦ, Vₐᵦ</td>
<td>Line Voltage – Inverter output (V)</td>
</tr>
<tr>
<td>Vₐᵦ, Vₐᵦ, Vₐᵦ</td>
<td>Phase Voltage – Inverter output (V)</td>
</tr>
<tr>
<td>P₁, P₂, P₃</td>
<td>Active power for R, Y and B phase respectively</td>
</tr>
<tr>
<td>Q₁, Q₂, Q₃</td>
<td>Re-active power for R, Y and B phase respectively</td>
</tr>
</tbody>
</table>

### I. INTRODUCTION

The problem of power injection into the grid must be investigated by modelling the SPV system as well as the grid. The design should be a controlled inverter output suitably interfaced with SPV system and grid, which can be capable of controlling real and reactive power.
power. The SPV system exhibits non-linear characteristics due to the following reasons.

- Insolation and temperature of SPV cell
- Movement of clouds and other natural factors mask the Sun’s ray from the SPV Cells
- The output of the SPV Cells needs to be converted to three phase power and synchronized with the grid
- The load in the grid is also a variable that depends on time, location and season
- A trip command issued by a relay to a major load would often result in power swing and the output of the SPV cells to the grid needs to be stable during this period
- Loss of a generator in the grid would result in power swing and the output of the SPV Cells to the grid needs to be stable during this period

In this paper the mathematical model of Solar Cell, Inverter, load and power measurement is discussed. The active and reactive power measurement with simulation results under different conditions is shown. It helps the user to understand the fundamental parameters of grid connected SPV system. The basic block diagram of the system is shown in Fig.1.

In the following sections, the detailed modeling of each block in Fig.1 is discussed. The required analyses have been carried out with the help of the developed mathematical models.

![Fig 1. SPV Grid integrated system](image)

A well-known five-parameter model of a SPV cell is considered for this work [2]-[3]. The mathematical equations used to simulate the realistic model of SPV cell are given in equations (1) and (2)

\[
I = I_{pv} - I_d - I_{sh} \quad (1)
\]

\[
I = I_m - I_{sh} \quad \text{where} \quad I_m = I_{pv} - I_d ;
I_m = I_{pv} N_{pp} - I_o N_{pp} \exp(A - 1) ;
A = \frac{V + I(R_{m} N_{o} / N_{pp})}{N_{m} V_{o}} ;
\]

\[
I_{pv} = [I_{pv} + K_d \cdot dt] \frac{G}{G_n} \quad \text{and} \quad I_{pv} = \frac{(R_s + R_p)}{R_p} I_{SC_n} \quad (2)
\]

For this work SOLKAR model having the following specifications have been used. The specifications at STC are: \( I_{SC}=2.55A, \ V_{oc}=21.24V, \ I_{mp}=2.25A, \ V_{mp}=16.56V, \ P_{mp}=37.08W \). The mathematical model of SPV system has been developed using MATLAB/SIMULINK with equations (1) and (2). To get the requisite voltage and current for the grid connected system considered for this work (5A and 230V), number of cells in series and parallel have been properly increased in the model. SPV array consists of 12 panels in series to obtain 230V and 2 panels in parallel to obtain 5A. The simulated characteristic of 12x2 array is shown in Fig. 2.
III. IMPLEMENTATION OF MAXIMUM POWER POINT TRACKING ALGORITHM

In this work, Perturb and Observe (P&O) algorithm [4] is used for MPP tracking. It has a simple feedback structure and fewer measured parameters. It operates by periodically perturbing (i.e. incrementing or decreasing) the array terminal voltage and comparing the SPV output power with that of the previous perturbation cycle. In rapidly changing atmospheric conditions, the MPPT takes considerable time to track the MPP. The illumination for 12 hours during a sunny day is obtained (Fig 3). The program runs for the recorded illumination for 12 hours in a sunny day. The simulation of algorithm is also given in Fig.3. From Fig.3, it is inferred that the P and O algorithm tracks MPP for various illumination levels.

IV. MATHEMATICAL MODEL OF THREE PHASE INVERTER

A Three Phase inverter is used to convert the DC output from the Solar Module to a constant AC three-phase 50Hz output. Analytical model is an important tool for prediction of dynamic performance and stability limits using different control laws and system parameters. Mathematical model of the inverter must be established before the design stage. The typical configuration of a three-phase full-bridge inverter is considered [6]. Semiconductor switching devices (Q1–Q6) of the inverter are controlled by PWM signals to...
obtain three-phase near sinusoidal ac voltages of the desired magnitude and frequency at the inverter output [5].

The switching functions can be mathematically represented as follows

\[
S_a(t) = \sum_{k=1}^{\infty} A_k \sin(\omega t + \phi)
\]

\[
S_b(t) = \sum_{k=1}^{\infty} A_k \sin(\omega t - \frac{2\pi}{3})
\]

\[
S_c(t) = \sum_{k=1}^{\infty} A_k \sin(\omega t - \frac{4\pi}{3})
\]

(6)

\[
\begin{bmatrix}
T_{AV} \\
T_{BV} \\
T_{CV}
\end{bmatrix} = \frac{1}{2} \begin{bmatrix}
1 & -1 & 0 \\
0 & 1 & -1 \\
-1 & 0 & 1
\end{bmatrix} \begin{bmatrix}
S_a \\
S_b \\
S_c
\end{bmatrix}
\]

(7)

The matrix expansion gives the \( T_{AV} \), \( T_{BV} \) and \( T_{CV} \) values, which can be used to obtain the line and phase voltages as shown.

\[
T_A = \frac{1}{2} [S_a - S_b]; T_B = \frac{1}{2} [S_b - S_c]; T_C = \frac{1}{2} [S_c - S_a]
\]

(8)

**Line Voltage Equations**

\[
V_{AB} = T_A \times V_{DC}; V_{BC} = T_B \times V_{DC}; V_{CA} = T_C \times V_{DC}
\]

(9)

**Phase Voltage Equations**

\[
V_{AN} = \frac{1}{3} (T_{AV} \times V_{DC}) \times V_{DC}
\]

\[
V_{BN} = \frac{1}{3} (T_{BV} \times T_{AV}) \times V_{DC}
\]

\[
V_{CN} = \frac{1}{3} (T_{CV} \times T_{BV}) \times V_{DC}
\]

(10)

**V. VARIATION OF INVERTER PARAMETER WITH SOLAR INSOLATION CHANGES**

The Solar radiation levels are modified to study the effect on inverter output. The Real and Reactive power output of the inverter for various solar insolation levels are shown in Fig 4. The maximum insolation for tropical countries like India is around 1000 W/m².
From the above result the following points can be summarised.

- When the $\varphi$ value varies there is no significant change in Active and Reactive power. The above measurement was noted for $\varphi =0$ and $\varphi =180$.
- The Active and Reactive power are at their maximum when $m=0.7$

Hence for further investigation the $m$ value is taken as 0.7 and real, reactive power and transfer ratio is shown in Fig 7.
VI. CONCLUSION

The mathematical model developed for the Grid connected SPV system has provided a constant Voltage and Power output after 10 cycles. This model can be used as the fundamental building block for further study on Grid connected SPV system.

REFERENCES


A Low Power New Data Compression Algorithm for Wire/Wireless Sensor Network using K-RLE

Kollipara Vasavi Chaithanya
Adithya Engineering college, JNTU KAKINADA, India
E-mail : chaitu.490@gmail.com

Abstract – In the context of the use of Wireless Sensor Network technology for environmental monitoring, the two main elementary activities of wire/wireless Sensor Network are data acquisition and transmission. However, transmitting/receiving data are power-consuming task. In order to reduce transmission-associated power consumption, in this proposed project I explore and suggest data compression by processing information locally. In order to improve the compression results with different statistics of data sources. Here I want to introduce in-network processing technique in order to save energy. In-network processing techniques allow the reduction of the amount of data to be transmitted. The well-known in-network processing technique is data compression and/or data aggregation.

The research work presents a development of the multi-sensor embedded system for measuring sensor parameters optimized by appropriate algorithms. Since most of the industrial applications use the analog sensors with transmitters for sensing the process parameters particularly in harsh environment because of their strong mechanical packaging and ruggedness. In this research work, I will evaluate and compare existing smart sensor systems performance with proposed system RLE.

Keywords - wire/wireless sensor network, data compression.

1. INTRODUCTION

Recent technological breakthrough in low power processing units and communication devices have enabled the development of distributed autonomous nodes able to sense environmental data, compute and transmit it using wireless communication to a base station known as Sink for future analysis; thus, forming a Wireless Sensor Network. However, Wireless Sensor Network is driven by a severe constraint which is power management. This power management has led researchers to explore scheduling sensor states. Scheduling sensor states is a technique that decides which sensor may change its state (transmit, receive, idle, Sleep), according to the current and anticipated communications needs. The most common technique for saving energy is the use of sleep mode where significant parts of the sensor’s transceiver are switched off. As described in, in most cases, the radio transceiver on board sensor nodes is the main cause of energy consumption: hence, it is important to keep the transceiver in switched off mode most of the time to save energy. Nevertheless, using the sleep mode reduces data transmission/reception rate and thus communication in the network. The question is how to keep the same data rate sent to the base station by reducing the number of transmission. In this article, I want to introduce In-network processing techniques, allow the reduction of the amount of data to be transmitted. The well-known in-network processing technique is data compression and/or data aggregation. Data compression is a process that reduces the amount of data in order to reduce data transmitted and/or decreases transfer time because the size of the data is reduced. However, the limited resources of sensor nodes such as processor abilities or RAM have resulted in the adaptation of existing compression algorithm to WSN’s constraint. Two main kinds of compression algorithms are available: lossless and lossy. The best known lossless compression Algorithm for WSN is S-LZW. Nevertheless, S-LZW which is an adaption for WSN of the popular LZW data compression algorithm is a dictionary-based algorithm. Compression algorithms based on dictionary require extensive use of RAM: such algorithms cannot be applied to most sensor platform configurations due to limited RAM. We hence introduce a generic data compression algorithm usable by several sensor platforms. In this article, we study the adaptation of a basic compression algorithm called Run Length Encoding (RLE). A "smart sensor" is a transducer (or actuator) that provides functions beyond what is necessary to generate a correct representation of a sensed or controlled quantity. The "smart sensor" functionality will typically simplify the integration of...
III. K-RUN-LENGTH ENCODING

The idea behind this new algorithm is this: let K be a number, If a data item d or data between d+K and d-K occur n consecutive times in the input stream, we replace the n occurrences with the single pair nd.

We introduce a parameter K which is a precision. K is defined as:

- If K = 0, K-RLE is RLE. K has the same unit as the dataset values, in this case degree. However, the change on RLE using the K-precision introduces data modified. Indeed, while RLE is a lossless compression algorithm K-RLE is a lossy compression algorithm. This algorithm is lossless at the user level because it chooses K considering that there is no difference between the data item d, d+K or d-K according to application.

II. RUN-LENGTH ENCODING

Run-Length Encoding (RLE) is a basic compression algorithm. The simple idea behind this algorithm is this: If a data item d occurs n consecutive times in the input stream, we replace the n occurrences with the single pair nd.

Fig.1.1 and Fig.1.2 are the graphical representation of the RLE algorithm applied on temperature readings. However, because RLE is based on the same consecutive input stream, its results depend on the data source. In this way, in order to perform RLE results with different data sources statistics, we have introduced a new compression algorithm which is inspired from RLE named K-RLE which means RLE with a K-Precision.
IV. SYSTEM DESCRIPTION

The generic architecture of system is shown in Figure 3. It consists of eight sensors with transmitters. To make the system more compact MICROCHIP’s 8 bit PIC18F452 has been used which has most of the peripherals on chip. It has low power consumption, fast executing speed and on chip 1536 bytes of flash and 256 bytes of data EEPROM memory. It can operate up to 10 MIPS (DC to 40 MHz). There are 18 interrupt sources, two-timer modules, two capture/ compare / PWM modules, 8x8 hardware multiplier and master synchronous serial port module having SPI and I2C interface. On chip serial communication supports both RS232 and RS485. The system can work up to 40 MHz clock frequency. But response time of many sensors is of the order of 100μs or more. So, a processor speed of 10 MHz to 15 MHz should be adequate. Considering the optimum performance and cost of the overall system and due to easy availability of crystal oscillators up to 16 MHz, the system clock of 10 MHz is selected for current application. There is 10 bits, 8 analog is selected for current application. There is 10 bits, 8 analog input channels A/D converter with acquisition time 12.86μs. The eight input sensor nodes operate under stored program control. The micro controller A/D converter performs periodic scans of these sensors. The scan rate is programmable and can be adaptive based on the rate of change of sensor reading.

All measured data is stored in on chip Flash and also serial EEPROM has been interfaced via I2C bus to utilize the non – volatile memory. All values are transmitted to LCD unit using the LCD interface. The
parameter values and their set-point values can be transmit via RS232 or wireless module (DIGI’s X-Bee – PRO 802.15.4 transceiver) which has capability to transmit data up to 1.6 km line of sight at frequency 2.4 GHz. In general, a lower frequency allows a longer transmission range and stronger capability to penetrate through walls and glasses. However, the GHz bands of 2.400-2.4835 are worldwide acceptable. The Microcontroller apart from the measurement of analog parameters also performs all the required housekeeping tasks and interacts with the other peripherals. A battery supply monitoring circuit generates an interrupt on detection of a battery fail condition and initiates an emergency measurement backup. There are two main time intervals that need to be maintained. The sensors with their transmitters carefully timed using software timers.

V. CONCLUSION AND FUTURE WORK

A development of the multi sensor embedded system for measuring up to eight sensor parameters optimized by appropriate algorithms with its various features are presented. In this paper, we have evaluated several data compression algorithms on an ultra-low power microcontroller from Texas Instrument known as MSP430. We have compared a famous dictionary-based data compression algorithm for WSN named S-LZW with RLE using real temperature datasets. Because of the difficulty in using S-LZW on a sensor platform with a limited RAM, we have introduced a new algorithm inspired from RLE named K-RLE which increases the ratio compression compared to RLE and SLZW. The developed system is cost effective, versatile, and based on generic platform. Currently, efforts are going on to increase measurements up to 16 sensors channels, which are suitable for most of our current applications like RO Plant automation and Smart pond fish management system, where in up to 15 parameters are to be monitored. Also implementation of appropriate wireless reconfigurable sensor network for future perspective so as to make the developed embedded system more applicable in Agro based Industrial applications.

VI. EXPERIMENTAL RESULTS

VII. ACKNOWLEDGMENT

The author wish to thank Mr. Varasala prasanth and K Raghu ram for their valuable comments and suggestions on an earlier draft of this paper.

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Steganalysis of GIF Images by Generalized Difference Image and Spatial Correlation of Pixels

S. Rakesh Kumar & S. Srinivas Kumar
Department of E.C.E., JNTUK College of Engineering, Kakinada, Andhra Pradesh
E-mail : kumarsrakesh@gmail.com, dr.srinivaskumar@gmail.com

Abstract - In this paper, we attempt to propose a universal steganalysis for palette type images such as GIF images. The generalized difference image of the adjacent pixels is obtained. Then color corellogram method is used to extract the local spatial correlation of colors in order to measure the dependencies of adjacent colors. The center of mass of the characteristic function of color corellogram and the absolute magnitude of Fourier coefficients is obtained. Total of 13 dimension features were classified with support vector machine (SVM) learning technique. Here in this paper, we consider images with embedded rate greater than 20% as the lower rate cannot be detected by any method and the performance is evaluated by three algorithms such as OPA, SoC and MBAS etc and ROC curves are obtained.

I. INTRODUCTION

Steganography is the science which disguises the presence of communication by encrypting it in a digital media. This media are called covers. A cover may be a digital image, an audio or a video. The first and foremost aim of this technique is to avoid having attention on the cover in which the message is embedded with a suspicion. There are two domains in which steganography are done. They are spatial domain which includes LSB embedding, pixel value differentiation, half toning and the transform domain which includes JP hide, out guess, yet another steganography scheme (YASS). There are many more such algorithms which can be studied in Ref. [1].

It is obvious that the probability of detection on hidden message gradually increases with the amount of information embedded. The choice of the cover media will matter a lot. Some experts in steganography recommend gray scaled images as best cover images apart from uncompressed scanned images of photographs or images taken from a digital camera. There are three different aspects in information hiding. First is Capacity, the cover can with hold. Second is Security that covers can provide and the third is Robustness of the cover media. Generally steganographic methods strive for high capacity and security and robustness is not a main concern, usually.

It is very common that everything have the other side, these steganography techniques can be used by anti-social elements for destruction of the nation. Steganalysis is the counter part of steganography. It is the science of detecting the presence of hidden message in a steganogram. Steganalysis is of two types, active steganalysis and passive steganalysis. Passive steganalysis refers to the method of detecting the presence of hidden secret message (present or not). Active steganalysis is the method of detecting the presence and length of the hidden secret message and also abstract it. Steganalysis is mainly categorized into two, namely target steganalysis and universal (blind) steganalysis. Target steganalysis is used for a specific steganographic algorithm. These are not useful methods other than what it is designed for. Whereas universal steganalysis techniques (blind steganalysis) can be used on any steganographic algorithm irrespective of the knowledge of embedding algorithm. But it is less accurate than the former.

RS [2] attack can detect even the message is embedded randomly or sequentially, whereas, chi-square detection method is good at detecting sequentially embedded message but not randomly embedded message. WAM and its advanced version can analyze the spatial steganography to a considerable level. Li et al.[4-5] and Zhang and Zhang could discover, yet another steganography scheme (YASS)[6] and LSB matching.

On observing, we can find that most of the steganalysis techniques concentrate on uncompressed images such as TIF, BMP or JPEG images. Apart from
these, GIF images can be used as covers as they are very popular in internet applications and multimedia. Many steganography algorithms for GIF images have been proposed [7-10] but the steganalysis of GIF images is still in its initial stages. One of the reasons for selecting GIF as one of the best covers is that it is different from gray scale image or color image. It has lesser colors up to 256; so, some of the statistics present in other images may not present in these GIF images.

We find a few papers, proposing GIF steganography. Westfeld et al. proposed chi square attack which can detect effectively, the presence of secret embedded message from EzStego images but if the message is randomly spread all over the cover, its efficiency falls down. Fridrich et al. [12] proposed a pair analysis (PA) which is based on higher order statistics. PA is more powerful and efficient than chi square attack as it can also estimate the length of the hidden message. Coming to universal steganalytic methods, higher order statistics were taken out and these are classified by using SVM.

In this paper, universal steganalysis algorithm for GIF images is proposed in which pixel value differentiation of adjacent pixels of image is calculated after reading it. Histograms of the characteristic functions were obtained and these are considered as features. Now a new technique is applied, called color corellogram, for measuring the relation between each other function and is given to a classifier, which decide it whether it is a cover image or a plain image. And finally the performance of the algorithm is evaluated by some other techniques such as Optimal Parity Assignment (OPA), Sum of Components (SoC), Multi Bit Adaptive Scheme (MBAS) algorithms.

II. GENERALIZED DIFFERENCE IMAGES CALCULATION:

The best way to measure the dependencies between adjacent pixels is by calculating the difference between them. Here we consider absolute difference instead of common difference. It is obvious that if the difference is more, the probability of being a cover stego is more i.e. distortion introduced by embedding data will be known.

As we know that GIF has three channels red (r), green (g), blue (b) we consider each color as a unit in this proposal. Let the image S be of size P x Q and pixel at mth row and nth column may be represented as p\textsubscript{mn}. The generalized difference image for pixel in three directions is calculated. If they are represented as H\textsubscript{D}, V\textsubscript{D}, and D\textsubscript{D}, then,

\[
H_{D(m,n)} = S(p_{m,n}) - S(P_{m,n+1})
= |r_{m,n} - r_{m+1,n}| + |g_{m,n} - g_{m+1,n}| + |b_{m,n} - b_{m+1,n}|
\]

\[
V_{D(m,n)} = S(p_{m,n}) - S(P_{m+1,n})
= |r_{m,n} - r_{m+1,n}| + |g_{m,n} - g_{m+1,n}| + |b_{m,n} - b_{m+1,n}|
\]

\[
D_{D(m,n)} = S(p_{m,n}) - S(P_{m+1,n+1})
= |r_{m,n} - r_{m+1,n+1}| + |g_{m,n} - g_{m+1,n+1}| + |b_{m,n} - b_{m+1,n+1}|
\]

\[
H_{hist}(l) = \sum_{m=1}^{P} \sum_{n=1}^{Q} (H_{D(m,n)l}), \quad 0 \leq l \leq 765
\]

\[
V_{hist}(l) = \sum_{m=1}^{P} \sum_{n=1}^{Q} (V_{D(m,n)l}), \quad 0 \leq l \leq 765
\]

\[
D_{hist}(l) = \sum_{m=1}^{P} \sum_{n=1}^{Q} (D_{D(m,n)l}), \quad 0 \leq l \leq 765
\]

Here fig. 2 and fig. 3. are some of the examples of Fourier coefficients absolute amplitudes for H\textsubscript{hist}. The cover image is selected randomly and embedded random bits into the selected cover image and made it a stego image. The rate of embedding is 50% for stego of fig. 1. and 60% for fig. 2..
Fig. 2. The absolute amplitude of Fourier coefficients of generalized difference image with 50% embedding rate.

Color correlation is a feature which is being extensively used in retrieval of image and indexing. It is nothing but a graph or feature extracted by performing spatial auto-correlation of palette i.e. range of colors used in the following image. The center of mass of the following function is obtained by applying this technique and is given to a classifier. We have used Support Vector Machine (SVM) as classifier, which decides whether the image is steganographed or not, with a radial basis of kernel function[26]. Every experiment is repeated twenty times and the average of these results is considered for optimization. The best parameters are of the classifier is obtained using five fold cross validation technique. Accuracy is calculated as

\[ A = \frac{(R_{TP} + R_{FP})}{2} \]  

Where \( R_{TP} \) is the true positive rate that an image is stated as stego by the classifiers and \( R_{FP} \) is the false positive rate that the image is not a stego when it is. The greater is the accuracy, the better is the performance.

### III. PERFORMANCE EVALUATION:

We consider three steganography algorithms and two tools for GIF images for the evaluation of the proposed algorithm. They are optimal parity assignment (OPA), the second is based on parity of Sum of Components and the last one is Multi Bit Assignment Hiding Scheme (MBAHS).

A graph is plotted for True Positive Rate (TPR) and False positive rate (FPR) the curve obtained is called Receiver Operating Characteristic Curve (ROCC). As the detection of hidden message is harder when the embedded rate is too low, we consider it to be more than 10%. The Table 1 below shows the classification accuracy of our proposed algorithm for the different hiding algorithms with different embedding rates.

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Embedding rate (%)</th>
<th>Accuracy (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA</td>
<td>50</td>
<td>97.48</td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>93.32</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>82.44</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>64.17</td>
</tr>
<tr>
<td>SoC</td>
<td>50</td>
<td>94.00</td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>89.69</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>75.22</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>67.26</td>
</tr>
<tr>
<td>MBAHS</td>
<td>50</td>
<td>73.26</td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>62.58</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>57.22</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>51.64</td>
</tr>
</tbody>
</table>

Table 1. Classification accuracy of proposed scheme

From the above table 1, we can notice that for SoC and OPA, when the embedding rate is greater than 30%, the accuracies crossed 90%. The proposed scheme is very effective against OPA as the accuracy reaches 97.48% when the embedding rate is 50%. The accuracy values fall down with the decrease in the embedding rate. In MBAS, it fell down more prominently. As the rate is 10%, its accuracy is around 50%, which is an equal probability to be a stego or a cover image and it seems to be undetectable against this scheme and the performance against OPA and SoC are still promising even the embedding rate is 10%. For better understanding, ROC curves are plotted for TPR and FPR for all the performance evaluators, namely, OPA, SoC, MBAS with embedding rates of 50%, 30%, 20% and 10%.

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International Conference on Advances in Electrical and Electronics Engineering (AEEE), ISBN: 978-93-81693-69-8, 22nd July 2012, Vijayawada
Steganalysis of GIF Images by Generalized Difference Image and Spatial Correlation of Pixels

It is observed that the TPR reaches almost 100% when the embedding rate is greater than 25% for OPA and SoC even though the FPR is 5% and also these plots indicate that MBAAS is not as better as the other two, however, the proposed scheme will efficiently detect the presence of embedded data if the rate is larger than 50%. And our proposed scheme failed to detect the presence of hidden message in adaptive hiding scheme (AHS) though maximum amount of message is embedded because AHS only embeds the image into the texture and smooth pixels are kept at one place collectively. As the detection is difficult in texture areas than smooth areas.

IV. CONCLUSION

Several GIF steganographic algorithms have been studied in this paper. A Universal steganalysis for detecting GIF steganographic algorithms has been proposed in which, the steganalytic features with high efficiency, were extracted while having a low directivity. The features extracted from GDI and color corellogram are highly effective in differentiating plain images from a steganographed image as they are designed to calculate spatial correlation among the adjacent pixels. By using a classifier, which is of two stages, we distinguished steganogram and a cover which have the embedding rate, not less than 20%. Results of the proposed scheme also show that it outperforms most of the other steganography techniques. It also achieves similar performance with Fridrich’s scheme. There are some limitations with the proposed scheme. Our proposed scheme is incapable of detecting the presence of embedded message if the embedding rate is less than 10%. The second limitation is that it fails to detect the hidden message against adaptive steganography as hide message in texture areas. Third limitation is that cartoons and computer generated GIF images are not considered in this scheme. And, detecting the GIF images with low embedding rate is still a challenge.

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REAL-TIME ATOMATION OF INDIAN AGRICULTURAL SYSTEM

M. Nagendra babu
School of Electronics,
Vignan University,
Guntur, India.
Mannepalli.babu@gmail.com

Indira priyadarsini.S.
Assistant Professor
School of Electronics
Vignan University,
Guntur, India.
Indirapriyadarsinis@yahoo.co.in

Abstract— the paper “Real time atomization of Indian agricultural system” using ARM7 and GSM” is focused on atomizing the irrigation system and at the same time caring the crop in all aspects for social welfare of Indian agricultural system and also to provide adequate irrigation in particular area. The setup consists of ARM7TDMI core with dedicated embedded equipment, the processor which is a 32-bit microprocessor; GSM serves as an important part as it is responsible for controlling the irrigation on field and sends them to the receiver through coded signals. GSM operates through SMSes and is the link between ARM processor and centralized unit. ARM7TDMI is an advanced version of microprocessors and forms the heart of the system. Our project aims to implement the basic application of atomizing the irrigation field by programming the components and building the necessary hardware. This project is used to find the exact field condition. The information is given on user request in form of SMS. GSM modem can be controlled by standard set of AT (Attention) commands. These commands can be used to control majority of the functions of GSM modem.

Keywords— ARM Controller, GSM, Sensors, Real-Time System, Data Acquisition and AT Commands.

I. INTRODUCTION

Atomized irrigation is an interesting application. Primarily for Real time atomization of Indian agricultural system for providing the better impacts on the social environment.

32-bit ARM processor is the contemporary general purpose microprocessor in the embedded market used in industrial level applications. GSM, as we know, is the most widely used mobile technology. Using a simple Subscriber Identity Module (SIM), it has taken the world of mobile communication to new heights. It is based on a simple architecture. Even with the introduction of new technologies like CDMA, GSM has stood its strength due to its efficiency and simplicity.

In our project, we are basically concentrating on the applications such as:

- To continuously monitor the soil moisture.
- To continuously monitor the water level of well.
- To check the temperature and humidity. so as to forecast the weather condition.
- To monitor the Plant or leaves health.
- To monitor & control the whole system through GSM module.
- Provide the detail information about the field condition like mineral content in the soil.
- Maintain faithful irrigation of the farm field via constant monitoring of 3–phase supply and other field parameters.

The system consists of a centralized unit, much like a mobile base station, consisting of the subscriber number. This forms the link between the user and the device. The whole system functions in the form network being connected to the centralized unit as a Node. The centralized unit is connected to many such nodes from/to which it receives or sends the data.

The user communicates with the centralized unit through SMS. The centralized unit communicates with the system through SMS which will be received by the GSM with the help of the SIM card. The GSM sends this data to ARM7. ARM7 also continuously receives the data from sensors in some form of codes. After processing, this data is displayed on the LCD. The communication between various devices takes place through RS232.

Thus in short whenever the system receives the activation command from the subscriber it checks all the field conditions and gives a detailed feedback to the user and waits for another activation command to start the motor. The motor is controlled by a simple manipulation in the internal structure of the starter. The starter coil is indirectly activated by means of a transistorized relay circuit. once the motor is started, a constant monitoring on soil moisture and water level is done & once the soil moisture is reached to sufficient level the motor is automatically turned off & a massage is send to subscriber that the motor is turned off.

II. WORKING PRINCIPLE

- To continuously monitor the soil moisture.

In case of monitoring the soil moisture, we know that each crop requires different moisture level. We are using a soil moisture sensor which is based on the principle of parallel capacitor. As we know that voltage across the plates is inversely proportional to the dielectric medium. This principle is used to determine the soil moisture by measuring the dielectric constant of soil. This is then informed the centralized unit. The centralized unit will send the message to
the device of that particular subscriber. The device waits for a certain amount of default time for which it is programmed. When the user does not respond to the centralized unit in default period the device continues monitoring the field parameters and keep on sending automatically to the centralized unit. Using the database stored in EEPROM of ARM, the corresponding moisture can be known by comparing the stored values and received.

- To continuously monitor the water level of well.

This application implemented using the Aluminium Or copper plates, the logic is simple but powerful. When the water surface will touch the plates then it will indicate the corresponding level of water source in the storage.

- To check the temperature and humidity, so as to forecast the weather condition.

For reading the Temperature and Humidity, here we are using two sensors, those devices gives little output voltages based on the environmental conditions.

- To monitor the Plant or leaves health.

Many fungal and bacterial diseases affect plants only when moisture is present on a leaf surface. The Leaf Wetness Sensor determines the presence and duration of canopy wetness, allowing you to forecast disease and protect the plant canopy. Because the Leaf Wetness Sensor measures the dielectric constant, droplets do not need to bridge electrical traces for the sensor to detect moisture. The presence of water or ice anywhere on the surface of the sensor will be detected.

Benefits:
- High resolution detects trace amounts of water or ice on the leaf surface.
- No painting or calibration necessary; factory calibration set at standard wetness threshold.
- Low power requirements enable long-term monitoring (2+yrs. with Em50 logger).
- Provide the detail information about the field condition like mineral content in the soil.

As a measure of soil acidity or alkalinity, soil pH constitutes one of the most important chemical soil parameters. Generally, soil pH (potential Hydrogen) values outside the range of 5.5 to 6.5 are considered as non-optimum because they can have negative impacts on nutrient availability, soil structure, soil organisms, and can make plants more sensitive to diseases. Due to uptake by plants and natural leaching of alkaline soil compounds, acidification is common among soils in temperate Climates. Fewer soils, like soils on limestone or on glacial till, have high pH values.

The regulation of soil pH by applying alkaline or acid fertilizers can limit effects of extreme acidic or alkaline soil conditions, which in turn improves crop production and resource efficiency. In a global view, soil pH regulation becomes a vital strategy within a radically changing world, where globally average crop yields must be increased by 60% to 120% until 2050 to meet the needs of the human population and dietary habits.

- To continuously monitor 3-phase supply.

It is based on the principle that whenever it will encounter 3-phases it will trigger a secondary relay circuit which in turn triggers the port pins indicating presence of all the three phases.

III. HARDWARE DESCRIPTION.
IV. ARM7TDMI ARCHITECTURE.

We have used ARM7TDMI processor in our model due to its advanced features like real-time clock and ISP-IAP. ARM7 consists of a number of peripherals interfaced to it. We use only the keypad matrix, LCD display, UARTS, GPIO and I2C protocol. ARM7 processor is a link between GPS and GSM modules for communication. The description of ARM7 is discussed in further sections.

Features:

- 16/32-bit ARM7TDMI-S microcontroller is a 64 or 144 pin package.
- 16 kB on-chip Static RAM.
- 128/256 kB on-chip Flash Program Memory. 128-bit wide interface/accelerator enables high speed 60 MHz operation.
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip boot-loader software. Flash programming takes 1 ms per 512 byte line. Single sector or full chip erase takes 400 ms.
- Two 32-bit timers (with 4 capture and 4 compare channels), PWM unit (6 outputs), Real Time Clock and Watchdog.
- Multiple serial interfaces including two UARTs (16C550), Fast I2C (400 kbits/s) and two SPIs
- 60 MHz maximum CPU clock available from programmable on-chip Phase-Locked Loop.
- On-chip crystal oscillator with an operating range of 1 MHz to 30 MHz.
- Two low power modems, Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Suitable for real-time applications with real-time clock.

V. GSM

A GSM modem is a wireless modem that works with a GSM wireless network. Computers use AT commands to control modems. Both GSM modems and dial-up modems support a common set of standard AT commands. So we can use a GSM modem just like a dial-up modem.

The main difference between them is that a dial-up modem sends and receives data through a fixed telephone line while a wireless modem sends and receives data through radio waves. GSM is one of the most vital components in our set up since all the communication between the users and centralized unit takes place through this modem. GSM communicates with ARM through I2C bus.

A GSM modem can be an external device or a PC Card. Typically, an external GSM modem is connected to a computer through a serial cable or a USB cable. Like a GSM mobile phone, a GSM modem requires a SIM card from a wireless carrier in order to operate. The description of GSM is given below.

V. ADVANTAGES

- The main advantages derived from this project are:

ARM7 is a 32-bit advance featured microprocessor that is a low power consuming processor, which is the foremost requirement of the industry. It has some unique features, which we have discussed in previous chapters. GSM is most common mobile technology with easy availability and simple operation. Its less signal deterioration inside buildings has ability to use repeaters. Talk time is generally higher in GSM phones due to the pulse nature of transmission. The availability of Subscriber Identity Modules allows users to switch networks and handsets at will. GSM covers virtually all parts of the world so international roaming is not a problem.

The project can be applicable at any level for different purposes by bringing about minor changes in programming, that is, there is no need to change the basic set up every time. For critical applications that need real-time monitoring, the field condition is transmitted to a base station through radio link. For non-real-time applications the data is logged on an on-board memory and down loaded as and when required.

VI. CONCLUSION

The project is thus carried out using ARM7TDMI core with the help of GSM technologies. This project finds application in domestic agricultural field. In civilian domain, this can be used to ensure faithful irrigation of farm field, since we have the option of finding out moisture level of soil in a particular area.

VII. FUTURE SCOPE OF THE PROJECT

- The future scope of this project is enhanced applications with the addition of the required feature One such application is to detect the soil parameter and suggesting the proper fertilizer and its feed time. Such Sensors can be incorporated in the design.
- In the same manner one can exactly predict the weather if the system is made to communicate with the nearer weather station through satellite communication.

VIII. RESULTS

Implemented hardware circuit for real-time automation of Indian agricultural system.
This below circuit consists of the ARM7 processor, GSM modem. all sensors are connected to the processor’s ADC pins because those components normally give analog output. And we are showing all the outputs in hyper-Terminal, which is a emulation program of connecting systems through TCP/IP networks, Dial-up modems and com ports.

Here, results for soil dry condition, level module and phase module.

This is another condition, which is having the good condition of the soil.

So, here no need to release water into the soil, here the sensor outputs like temperature and humidity along with those outputs.

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