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Study on Performance Analysis of CMOS RF front-end circuits for 2.4GHz Wireless Applications

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Study on Performance Analysis of CMOS RF front-end circuits for 2.4GHz Wireless Applications

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***Abstract*—In this paper, low voltage design concepts and new CMOS front-end circuits for 2.4GHz wireless applications are presented. The performances of these circuits are analysed and compared with other existing structures using TSMC 0.18-µm CMOS technology scale. The design trade-offs between impedance matching, power gain and noise figure of low-noise amplifiers are highlighted. The advantage of the introduced mixer topology is expressed in terms of conversion gain, noise figure and linearity. At a supply voltage of 1.8V, the design and performance analysis have been performed using Agilent's Advanced Design System (ADS2009) software.**

Keywords-CMOS,Front-end, LNA, Mixer, Radio Frequency.

I. INTRODUCTION

Today an increasing market demand for RF transceivers operating in the 2.4GHz consumer based wireless applications such as mobile phones and wireless local area networks. CMOS is one of the best integration technologies suitable for designing RF circuits and systems under deep sub-micron technology scale. The development of high performance Radio Frequency (RF) transceivers or multi-standard/reconfigurable receivers requires innovative RF circuit design to make the best of a good technology. Another aspect for realization of analog circuits in CMOS technology is the possibility of reduction of supply voltage with each technology generation. The selection of receiver architecture is based on high performance and less number of off-chip components. The following are the existing receiver topologies such as Zero-IF, Heterodyne, Low-IF and wide-band IF in RF transceivers. Recent research works proved that zero-IF always the popular and widely used for RF applications, among these four architectures. At the same time, heterodyne architecture can provide sufficiently low noise figure but more external filter circuitry required which also increases receiver size and power dissipation. So that, Direct Conversion (DCR) or zero-IF or Homodyne receiver is always the best because it uses less number of off-chip components and less power consumption. The down-conversion architecture produces an image at zero frequency, thus no image filter is required. Many short range 2.4GHz receivers have been designed with a higher supply voltage and with different technology scale [1]. Several low-power single-ended LNA designs have been reported with different frequency bands, such as 900MHz, 2GHz. These LNA

design needs additional balun circuitry to convert single-ended output into differential output [2]-[6]. Also, the second stages of receiver's are the mixers which require only signal to be fed from a differential source. Among the various CMOS mixer research, passive and active mixers can have low conversion

gain and high noise figure (NF)[8]-[12]. Such a high NF will limit the signal to noise ratio of the front-end. At the same time, existing circuit topologies cannot satisfy the required wireless specifications under low voltage operation. Hence it is of interest to introduce new wireless Direct Conversion receiver front-end components that can handle successfully low supply voltages. The choice of receiver architecture, circuit topology design and systematic optimization of the front-end blocks is always necessary. Basically, front-ends are responsible for tracking weak signals (RF) at high frequency and translating into IF signals for transmitting with high power levels. It is an interface between the antenna and digital modem of the wireless receiver. Therefore, it needs high performance analog circuits like RF amplifier (LNA), Mixer and Oscillator. The simplified block diagram of a Direct Conversion Receiver front-end is shown in Fig.1 It represents the process of 2.4GHz incoming RF signal frequency (f_{RF}) by the LNA and down-converted into 150MHz intermediate frequency (f_{IF}) by the mixer.

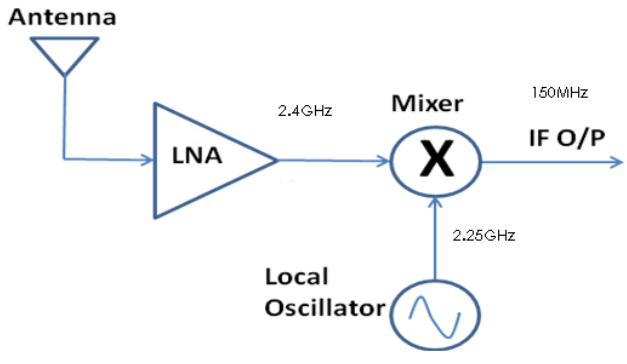

Fig.1. Block diagram of RF receiver front-end

II. LNA DESIGN

A low noise amplifier (LNA) being the first stage of the receiver front end and it is used to increase the power signal coming from the antenna while introducing little noise by the same LNA. Its main function is to provide enough gain to overcome the noise of next stages. The receiver's sensitivity is mainly depends upon the LNA noise figure and gain. Being the first gain stage of the receiver, it should also satisfy the following objectives such as accurate input/output matching, minimizing the noise figure and providing a high gain with good linearity. In general, the LNA structure composed of impedance matching block for input, output section and amplification block. In this work, LNA amplification block is modified for better noise figure and gain. The amplification block is constructed by dual transistors in CS stage, shown in fig.2. Also an inter-stage inductor is added in between the stages for improving the impedance matching.

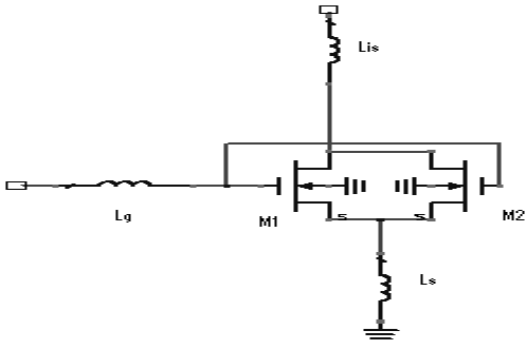

Fig.2.Single CS stage using two transistors

Using this principle, two new LNA structures are realized in single-ended and differential topologies. Fig.3 represents the schematic of proposed LNA architecture. It comprises an input stage inductor L_g , inter-stage inductor L_{IS} ,dual CS transistors M1,M2 , single CG transistor M3 and output impedance matching inductor L_d .

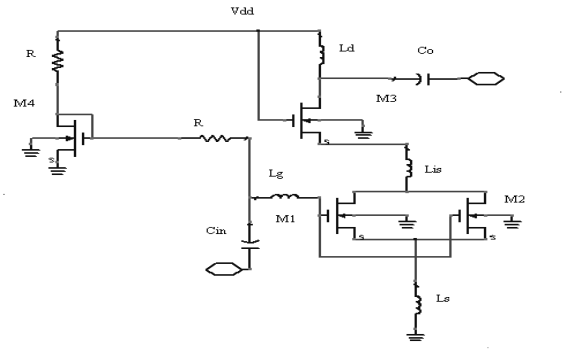

Fig.3. Schematic of Single-ended Dual-CS (SDC) LNA

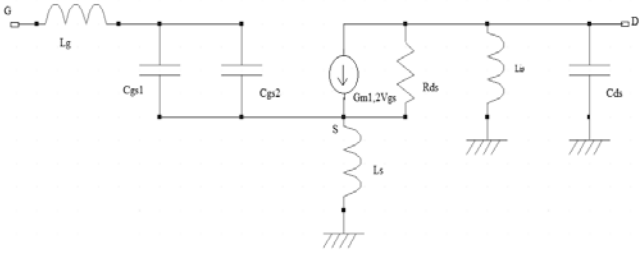

Fig.4.Equivalent model of input stage

The simplified theoretical expressions for input impedance and output impedance of the dual CS stage is developed from equivalent circuit, shown in fig.4.The gate-source capacitances and drain-source currents are paralleled in this model. C_{gs1} , C_{gs2} and $G_{m1,2}$ V_{gs} represents the gate-to-source capacitances and drain-source currents. The input impedance seen at the gate of M1 is calculated by using eqn.1.

$$R_{in} = \frac{L_s g_{m1} g_{m2}}{C_{gs1} + C_{gs2}} \qquad (1)$$

With the help of operating frequency ω_o and the gate-to-source capacitance, the optimized width of the transistors can be calculated. The output impedance of the common source stage with inter-stage matching inductor is calculated by using eqn. (2)

$$Z_{out} = SL_{is} + \frac{1}{S(C_{ds1} + C_{ds2})} + \frac{g_{m1} g_{m2} L_s}{(C_{ds1} + C_{ds2})} \qquad (2)$$

C_{ds1}, C_{ds2} are the drain-to-source capacitances of the transistors M1,M2.

The optimized transistor widths and inductor values are calculated by using the following design equations for performance analysis. The design steps are elaborated through these design factors.

- Gate inductance (L_g)
- Gate source capacitance (C_{gs})
- Width of the transistor (W)

The centre frequency $\omega = 2\pi f_0$ (3)

$= 2\pi * 2.4 * E^9 = 15.07964474 E^9$ rad/sec is calculated by using eqn.(3)

The value of L_g (gate inductance) is realized by means of eqn.(4). The Q of an inductor value is selected as 8, based on

0.18-µm CMOS scale characteristics. The source impedance is assumed to be 50ohms.

$$L_g = \frac{Q_L R_s}{\omega_o} \quad (4)$$

$$= \frac{(50)(50)}{15.07964473\,E^{9}} = 14.0786399 * E^{-9} H$$

The gate source capacitance (C_{gs}) is expressed in terms of RF frequency, shown in eqn.(5). L_s is equal to 1nH.

$$C_{gs} = \frac{1}{4\pi^2 f_o^2 (L_g + L_s)} \quad (5)$$

$$= \frac{1}{(39.47841760)(2.4E^{9})^2 (14.0786399E^{-9} + 1E^{-9})}$$

$$= 0.1005014634 E^{-12}$$

C_{gs} =0.1 pF

From the technology scale characteristics, the values of L_{min}=0.18E^{-6} m, T_{ox}=4.1E^{-9}m are observed. Permittivity of oxide is calculated by using this eqn.6,

$$\varepsilon_{ox} = \varepsilon_o \varepsilon_s \quad (6)$$

where ε_0 is the dielectric constant for free space, which is equal to 8.854E^{-14} F/cm and dielectric constant of silicon is equal to 3.9. Therefore, oxide capacitance is calculated by using eqn.(7)

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \quad (7)$$

$$= \frac{3.9 \times 8.854\,E^{-14}}{4.1E^{-9}} = 8.641446341E^{-8} \text{ F/um}^2$$

The optimized width of the transistors are calculated by using eqn.(8). The sizes of the transistors are assumed to be equal in dual CS stage.

$$W = \frac{3C_{gs}}{2C_{ox}L_{min}} \quad (8)$$

Therefore, width W $= \frac{3*0.1005014634E-12}{2*8.641446341*E^{-8}*0.18E^{-6}}$

W = 96.999999E^{-6} m

The calculated values are substituted in their respective places in the schematic and are simulated to evaluate the performance of the designed circuit. With the transistor width at 97µm, the LNA achieved the optimum performance in terms of gain, noise figure and impedance matching for this design. Dual-CS Differential LNA is constructed by using two single-ended LNA's and its structure shown in Fig.5. The design calculations are the same as that of Dual-CS single ended LNA. In addition, the values of drain inductors are calculated by assuming C_{out} as 1pF in eqn.(9).

$$L_D = \frac{1}{4\pi^2 f_o^2 C_{out}} \quad (9)$$

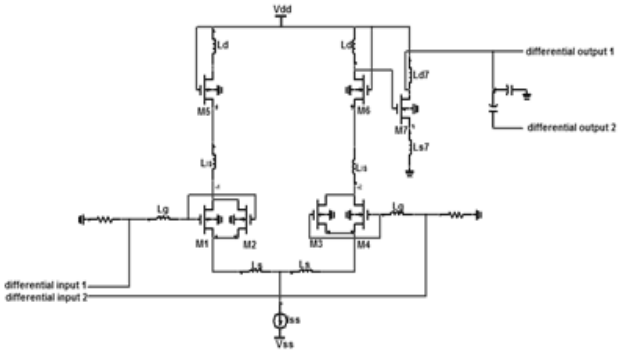

Fig.5. Schematic of Differential Dual-CS (DDC)LNA

The other existing LNA structures such as Cascode single-ended LNA, differential LNA are also designed using 0.18-µm technology scale. The schematics are shown in fig.6&fig.7

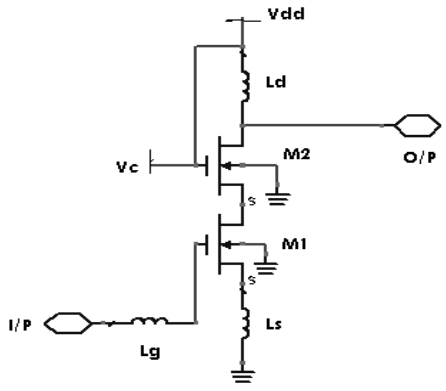

Fig.6. Single-ended Cascode LNA

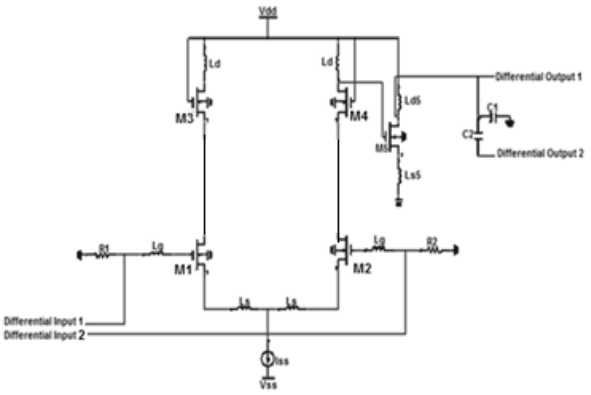

Fig.7. Differential LNA

III. MIXER DESIGN

A down-conversion mixer is always followed by the RF Low-noise amplifier. It is one of the most important parts and used to translate one frequency into another. It changes the RF signal into IF output signal. IF signal frequency is the difference between RF and Local oscillator signal frequencies. Mixer plays an important role in improving the overall system linearity. The proposed mixer designs based on double-balanced, active mixer topology and mainly developed for low voltage applications. There are two modifications done here, one in transconductance stage, another in biasing. The RF stages are completely revised in both designs. In order to utilize the low supply voltage both RF and LO stages have been biased separately and it is done with passive elements such as resistors. The first design uses series form of transistors and the second one uses inductors at RF input stage for providing better impedance matching and reducing noise figure.

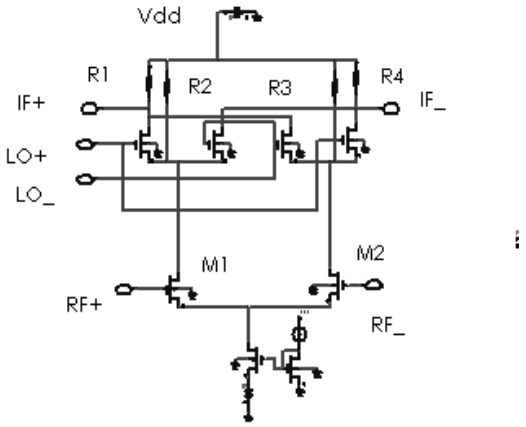

Fig.8. Folded Gilbert mixer

Fig.8 represents the Folded Gilbert mixer whose RF &LO stages have been biased separately. The other two structures are Inductive coupled and Transconductance mixers,which are shown in Fig.9&10. The first topology consists of four nMOS transistors (M5-M8) in transconductance stage, and the second design composed of only two transistors M5,M6 with inter-stage matching inductor L.

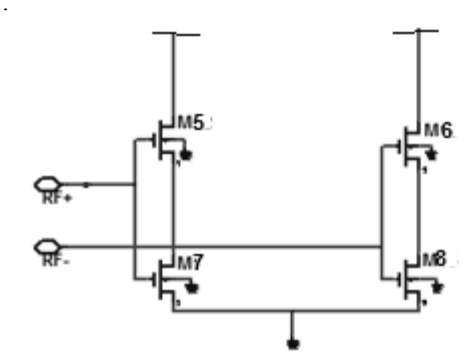

Fig.9. RF stage of Transconductance mixer

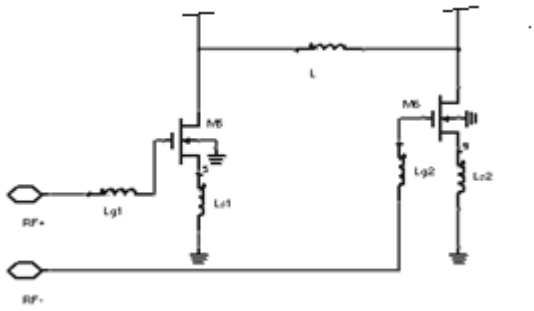

Fig.10. RF stage of Inductive Coupled mixer

The use of folded technique is only to increase the bias current through the transconductance stage without increasing the current through the switching transistors. It needs smaller LO drive voltage to drive the switching transistors and thereby improves the switching efficiency. In order to reduce flicker noise, transconductance stage is altered by adding inductors L_g and L_s at the gate and source terminals of the RF transistors. Additionally, an inductor L with 20nH is added in between the stages to achieve good performances of mixer in terms of conversion gain and noise figure. The size of the transistors are calculated by evaluating g_m and C_{ox} design formulas. L_g and L_s inductors used not only for reducing the noise figure but also, the input impedance matching at 50 ohm. Their values are 10nH and 0.5nH respectively. The width of the transistor is evaluated by using this eqn. 9.

$$W = \frac{g_m^2 L}{2K_n I_{DS}} \quad (9)$$

where L is the channel length of the transistor and I_{DS} is the drain to source current. Here $g_m = 0.02$, $L = 0.18$ um and I_{DS} is assumed to be 3mA

$K_n = \frac{\varepsilon_{ins}\varepsilon_o\mu}{D}$ is the process dependent term

where D is the oxide thickness and ε_{ins} is the permittivity of insulator. ϵ_o is the permittivity of free space and μ is the mobility of charge carriers.

The typical values of these factors are substituted and calculated the optimized width of the transistors.

$$W = \frac{0.02^2 \times 0.18}{2 \times 288.3 \times 10^{-6} \times 3 \times 10^{-3}} = 80.4359 \text{ um}$$

IV. RESULTS

Front-end design evaluations are performed at 2.4GHz RF frequency and 2.25GHz LO frequency. The front-end circuits' performance is analyzed by using Intel Core2DuoCPU E7400@2.80GHz processor with Agilent's Advanced Design System (ADS) 2009 version software. The design simulation process has been carried out in a standard TSMC 0.18-µm CMOS process technology. The simulation environment offers great flexibility in investigating the performance characteristics of front-end subsystems. The various parameters analysed here are S parameters (S21,S11), noise figure and conversion gain to describe LNA and mixer performance with a supply voltage of 1.8V. Simulation parameters with their values are described in the Table-1.

TABLE 1. Simulation Input Variables

Parameters	Values
Source/Load impedance	50 /500ohms
RF frequency	2.4GHz
LO frequency	2.25GHz
RF power	-30dBm
LO power	5dBm

The dual-CS Differential LNA graphs of S parameter analysis with respect to RF frequency which lies between the range of 1.0 to 3.0 giga hertz are given below in Fig.11. The value of the input impedance matching can be obtained as -8.37 dB. The value of forward gain S_{21} is reached as 28.75 dB, indicated by markers m1&m2.

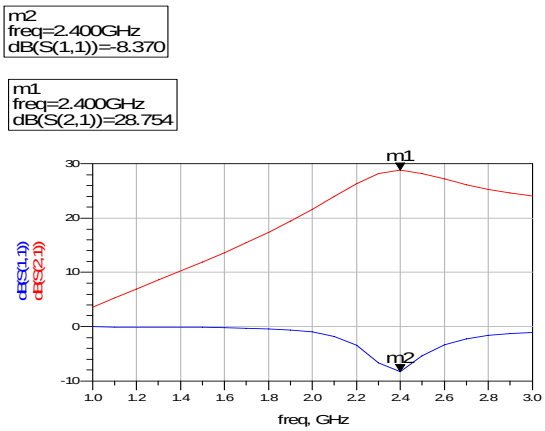

Fig.11. S-parameters of Dual-CS Differential LNA

The noise figure of LNA should remain below 4 dB at 2.4GHz in order to prevent inducing noise problems in other stages of the receiver; like mixer, voltage gain amplifier etc. The noise figure graph of the proposed LNA design satisfied this constraint and it is given below in fig.12.

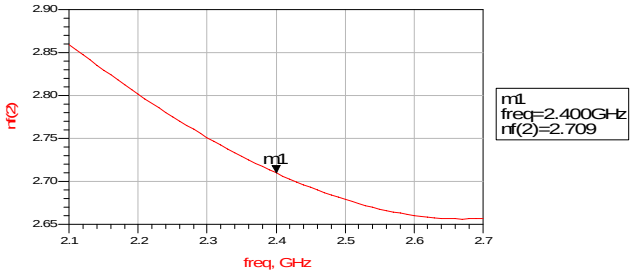

Fig.12. Noise Figure of Dual-CS Differential LNA

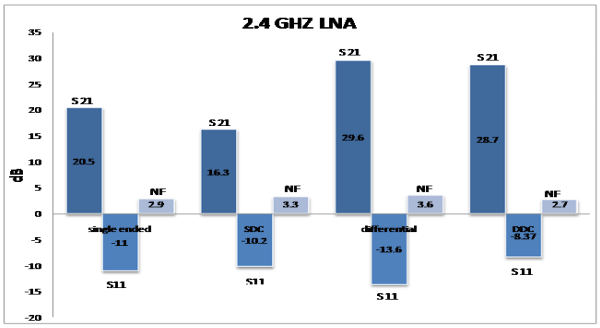

Fig.13. Performance Comparison of LNA's

The performances of other LNA's have been observed and compared,shown in Fig.13. The conversion gain of a mixer is defined as the ratio of the desired IF output to the RF input. If the ratio is less than one, it is referred as conversion loss. The conversion gain of a mixer is important because it supports to

determine the noise figure and linearity of the overall system. It is plotted as the function of LO_power in dBm. Fig.14. shows the conversion gain of the mixer. It has a value of 21.276 dB at LO_power of 5 dBm. The noise figure of the mixer is observed as 7.9dB and the graph is given in Fig.15.

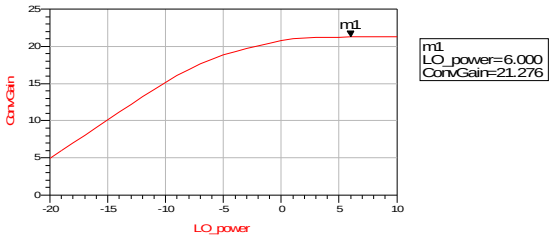

Fig.14. Conversion of Gain Inductive Coupled Mixer

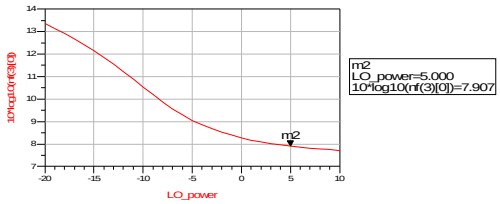

Fig.15. Noise Figure of Inductive Coupled Mixer

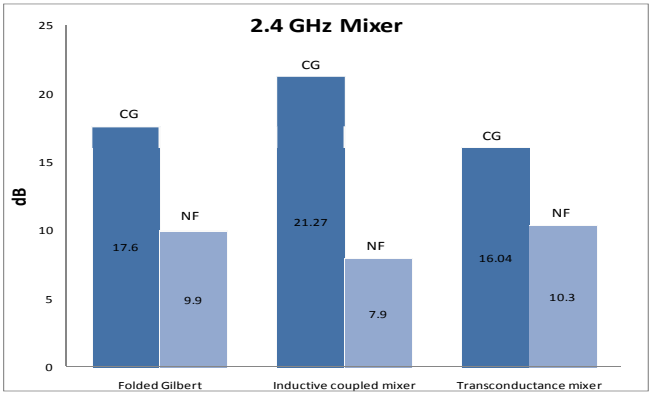

Fig.16. Performance Comparison of Mixers

The performance of Mixers have been analysed and highlighted in Fig.16. The proposed mixers compared with folded Gilbert mixer.

V.CONCLUSION

In this paper, front-end circuits suitable for 2.4GHz wireless applications were presented. The demonstrated front-end circuits include LNA and Down-Conversion Mixers. The theoretical background is discussed and the formulae of optimum LNA, Mixer design for the proposed configuration has been given. Several topologies of LNA, Mixers were first studied, analysed and also utilized for performance comparison study. DDC LNA and inductive coupled mixer shows good performance improvement in all performance factors by 20% than other circuits.

REFERENCES

[1] J.A.M.Jarvinen et al., "2.4GHz receiver for Sensor Applications", *IEEE Journal of Solid State Circuits*,vol.40,N0.7,pp.1426-1433,July 2005.

[2] Arthur Nieuwodt , et al. "Design techniques for reducing the impact of component variations on narrow-band low noise amplifiers", *Analog Integr Circ Sig Process, Springer Science Journal* , No.55pp.189-193,2008.

[3] Trung-lien Nguyen,et al., "CMOS Low-noise amplifier design optimization techniques", *IEEE Trancactions in Microwave theory and techniques*,vol.52,No.5,pp.1433-1442,2004.

[4] Ahmed A.Youssef,"Design guidelines for the noise optimization of a 0.18µm CMOS Low noise amplifier", *Analog Integr Circ Sig Process, Springer Science Journal*,No.46,pp.193-201,2006.

[5] Baimei Liu, et al., "An Ultra-Low Voltage and Ultra-Low Power 2.4GHz LNA Design", Radio Engineering, vol.18, No.4, pp.527- 531,2009.

[6] P.Andreani, H.Sjoland, "Noise optimization of an inductively degenerated CMOS low noise amplifier", IEEE Transactions on Circuits &Systems, vol.48, No. 9, pp.835-841,2001.

[7] Tae-Sung Kim, et al.., "Post-Linearization of Differential CMOS LNA Using Cross-Coupled FET's", *Journal of Semiconductor technology and Science*, vol.8,No.4,December 2008.

[8] Jenn-Tzer Yang.et al.,"A 2.4GHz Low power Highly linear mixer for Direct-conversion receivers", *International journalof circuits, systems &signal processing*,vol.no2,2007

[9] Vidojkovic.V, et al., "A low-voltage folded-switching mixer in 0.18µm CMOS", *IEEE Journal of solid-state circuits*, vol.40, no.6,1259-1264, 2005.

[10] Park.J,Lee.C,Kim.B ,"Design and analysis of low flicker-noise CMOS mixers for direct –conversion receivers", IEEE transaction on Microwave theory and techniques,vol.54 no.(12),4372-4380,2006.

[11] Jenn-Tzer Yang, et al., "A 2.4GHz Low Power Mixer for Direct Conversion Receivers", *International Journal of Circuits,Systems and Signal processing*,issue 2,vol.1,2007.

[12] Wan-Rone Liou,et al.,"Design and Implementation of 2.4GHz CMOS Front-end for Wireless Communication", *Journal of Marine Science and Technology*,vol.13,No.3,pp.170-175, 2005.

[13] Mihai A.T.Sanduleanu, Maja Vidojkovic, Arthur, "Receiver Front- End Circuits for Future Generations of Wireless Communications", *IEEE Transactions on Circuits and Systems* –II, vol.55, No.4, April 2008.

[14] M.Arasu,et al, "A 2.4GHz CMOS RF front-end for wireless sensor network applications", *IEEE Radio Frequency* Integrated Circuits Symposium, 2006.