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Power Optimization For A Datapath Of General Purpose Processor

VIJAYALAKSHMI. NARISETI
Department of ECE,GIT.GITAM University,vizag, vijaya.nariseti@gmail.com

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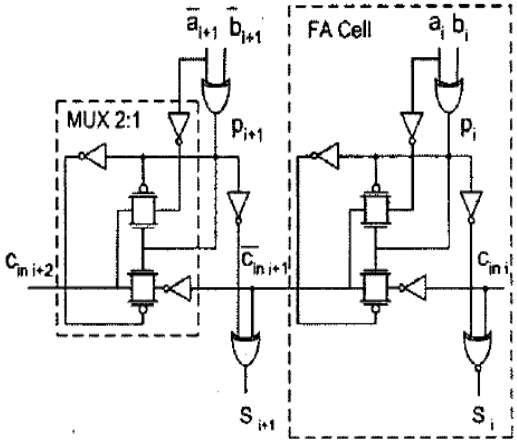
VIJAYALAKSHMI.NARISETI
Pursuing master of technology
(Department of ECE,GIT.GITAM University,vizag)
Email: vijaya.nariseti@gmail.com

Abstract: This paper explores different data path architecture topologies for low power solutions. And we look at the energy optimization of different topologies. This paper is aimed at characterizing various architecture implementations of different data path operators like adders and multipliers and a different style of multiplier with minimum power and delay product and different adder topologies.

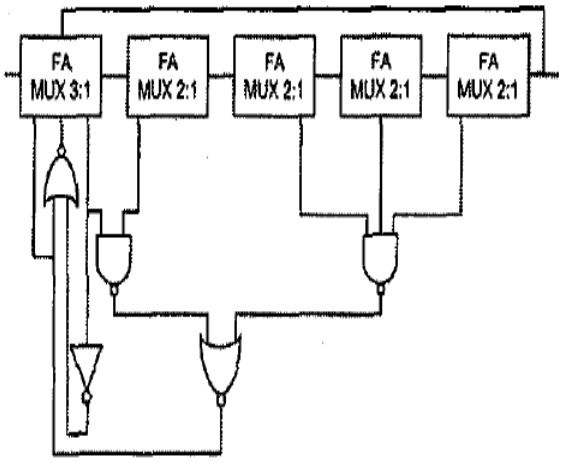
Adder design:

In VLSI design, different adder topologies were proposed. Here full adder is design with pass transistor logic.



1. Full adder cell

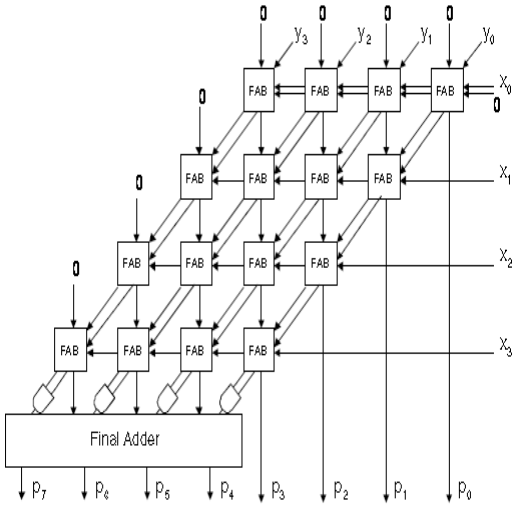
Small no. of gates provides great energy consumption. In the beginning of analysis for low power applications refer to the ripple carry adder. Full adder complementary cells can be implemented using multiplexer and pass transistor logic.To keep the power requirements low the next adder topology is carry skip adder. This is having same architecture as ripple carry adder but the difference is the multiplexer in the carry path. For the delay performance the next type of adder is variable block adder.



2.Variable block adder

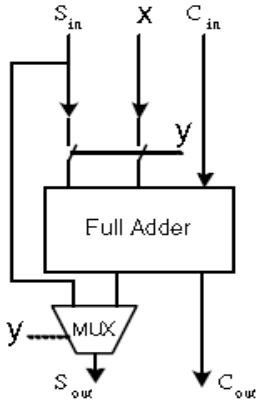
Multiplier design:

This paper contains the normal carry save multiplier and bypass carry save multiplier and finally mixed multiplier is the combination of Wallace tree and bypass multiplier.



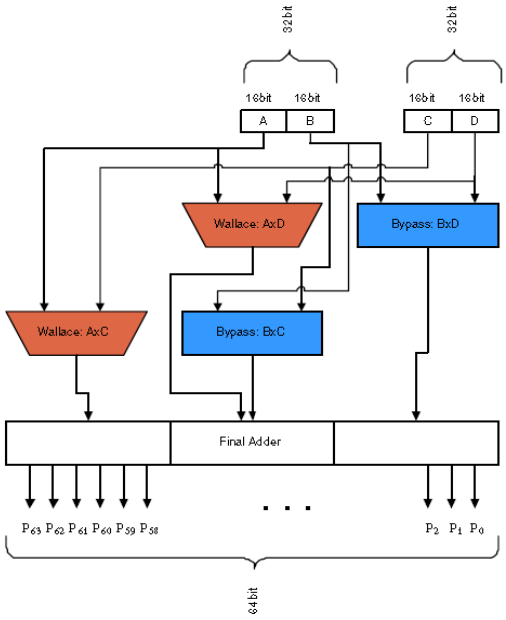
3.bypassmultiplier

In this paper presenting a technique to minimize the power dissipation in digital multipliers in both dynamic power and switching activity



4.fulladder

To minimize the switching activity there has been lot of techniques, one of that is clock gating. Here similar technique is used i.e. use of transmission gates, to block or pass the logic similar to clock gating.



5.mixed multiplier

In general, the normal carry save adder offers great dynamic power savings and tree multipliers offers reduced area and fast speed. The mixed type architecture operation is as follows, the 32 bit input is split into two 16 bit numbers and using two different types of multipliers bypass and Wallace LSB and MSB bits are arranged accordingly. The final output product can be obtained by doing shift and add method. The shift is done as follows.

P=z<<32+w<<16<<x<<16+y

Here the output is a 64 bit partial product But mixed architecture gives both power and delay savings compared any other architectures such as array, bypass and tree multipliers. All these adder and multiplier deigns are synthesized and verified using cadence tools and the technology that is using is ami 0.6µm technology and for power optimization the tool used is synopsys design compiler.

Conclusion:

Architectural exploration of for the design of low power data path and power optimization has been done. The multiplier used gives better performance and these adder designs gives better delays and low power consumption compared all other architectures that are previously used. This mixed multiplier gives a better delay and power product compared to all other architectures. This offers significant power and timing changes.

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