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A Strategic Review on Growth of InP on Silicon Substrate for Applications in High Frequency RF Devices

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Abstract—A review is presented on the advances in InAlAs/InGaAs High Electron Mobility transistors (HEMT) on silicon substrates for high frequency and low noise applications. Although InAlAs/InGaAs HEMTs on InP and GaAs substrates have been much appreciated due to their superior performance, their widespread applications have been hindered due to higher cost of the substrates. Silicon has been used as an alternative substrate considering the benefits of low cost, technological maturity and integration of III-V and silicon technology inspite of the constraints like lattice mismatch and large difference in thermal expansion coefficient.

Keywords- HEMT, InP,Si ,SOHCOW

I. INTRODUCTION

Silicon substrates dominate over other available III-V substrates due to various reasons; the most noteworthy being their low cost. Silicon substrates without any doubts have better mechanical and thermal properties and are available as per consumers' specifications. Therefore silicon substrates are attractive in both their properties and utilization. InP substrates are fragile and very expensive, and InP technology is also not as matured as that of silicon. This limits the use of InP as a well balanced substrate material. Furthermore, these substrates need to be handled with utmost care as wafer breakage increases yield loss. Though, InP based HEMTs grown on GaAs substrates reduce the cost, they do not provide a pathway for integration with silicon technology. Besides, GaAs wafers are costlier than silicon substrates.

Recent International Technology Roadmap for Semiconductors (ITRS) update has given emphasis to "Beyond CMOS" and "More-than-Moore" technologies (Fig.1) to expand its roadmap and implement non-CMOS devices on Si-CMOS platform [1].

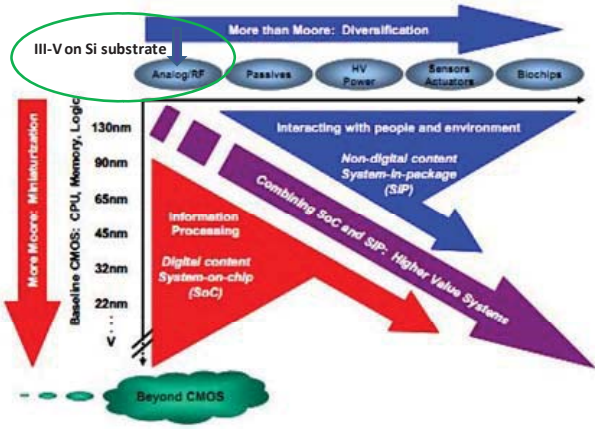

Figure 1. Hybrid Integration of III-V (non-CMOS) technology with Si-CMOS platform [1]

In this scenario, the growth of InP as a virtual substrate on silicon can open a new window for the integration of III-V technology with matured silicon technology so that we can reap the combined qualities of both the technologies forming System on Heterogeneous Chip On Wafer (SOHCOW). There has been extensive study of growth of InP on silicon and its approach to fabricate devices like LEDs, lasers, solar cells, and other optoelectronic devices for optical communication. The first reports date from 1986 [3] where InP thin film solar cell was fabricated on silicon substrate. However, the interest in using silicon as a substrate for InAlAs/InGaAs HEMTs is relatively new. Although,InAlAs/InGaAs HEMTs grown metamorphically on GaAs substrates contributes to high quality active layer extensively used in low cost, high power and low noise monolithic millimeter wave RF applications [4],[5], silicon still remains the anticipated platform for InAlAs/InGaAs HEMTs over conventional substrates. Although the cost of silicon substrate is highly dependent on various specifications, a general cost comparison of silicon with respect to GaAs and InP substrates is presented in Table I. [2]

In spite of several advantages of silicon substrates, there are some technological hindrances that need to be overcome for using epitaxially grown virtual substrate on silicon.

TABLE I. COST COMPARISON OF SUBSTRATES

Diameter(Inch)	Thickness (µm)	Substrate	Cost ($)
2	350	Si	60.16
		GaAs	208.60
		InP	551.30
3	600	Si	35.15
		GaAs	268.20
		InP	730.10

II. TECHNOLOGICAL HINDRANCES

The major problems faced by researchers when InP is grown on silicon substrate are:

1. High difference in lattice parameter between InP and silicon
2. Difference in thermal expansion coefficient
3. Presence of native oxide on the silicon substrate
4. Formation of antiphase domains(APD) due to difference in lattice symmetry

The 8% lattice mismatch between silicon and InP produces high dislocation density at the interface. Also, the propagation of the threading dislocations away from the interface into the device epilayer is a major concern. The degradation of electrical transport properties in the epilayer is well correlated with the density of these dislocations.

In addition to lattice mismatch, the difference in thermal expansion coefficients between silicon and InP (about 50%) has a major impact on the epitaxial quality due to thermal stress which results in degradation of the epitaxial film.

Further, for good epitaxy it is necessary to have an oxide free surface of the substrate.

Moreover the polar and non-polar nature of Si and InP results in antiphase domains separated by antiphase boundaries (APBs). This growth of polar semiconductors on non-polar substrates forms electrically active defects which are responsible for scattering and reduction of carrier mobility.

Various epitaxial and non epitaxial techniques have been realized to overcome these problems for the growth of InP based epilayers on silicon substrates with reduced dislocations.

III. TECHNIQUES FOR DEFECT ENGINEERING

a) Direct Epitaxy of InP on Silicon Substrate

A potential solution for direct epitaxy for high quality InP on Si substrate was reported by Y.Ababou et al.In this method the substrate roughness was minimized by using buffered HF solution [6].

Another technique that yields improved epilayer quality is Thermal Cycle Growth (TCG) (alternate growth and annealing steps) for the direct heteroepitaxy of InP on heterogeneous Si (111) substrates. In this technique, the use of silicon (111) instead of silicon (001) has helped in reducing dislocation density [7].

Furthermore a two step growth method using low pressure Metal Organic Chemical Vapor Deposition (LP-MOCVD) has also been reported to grow InP directly on silicon substrate. By optimizing various parameters like growth temperature and III/V ratio of the first layer the crystalline quality of InP grown on silicon was improved [8].

b) *Epitaxial growth of InP on Si using intermediate buffer layers*

Different techniques and methods have been worked out using intermediate buffer to reduce the lattice mismatch and filter the existing dislocations from propagating into the device channel. One of them involves the growth of InP layers on GaAs buffer by Metal Organic Chemical Vapor Deposition (MOCVD) on Si substrates [9]. Figure 2 shows a typical epilayer layout of InAlAs/InGaAs HEMT grown on silicon substrate using intermediate buffer layers.

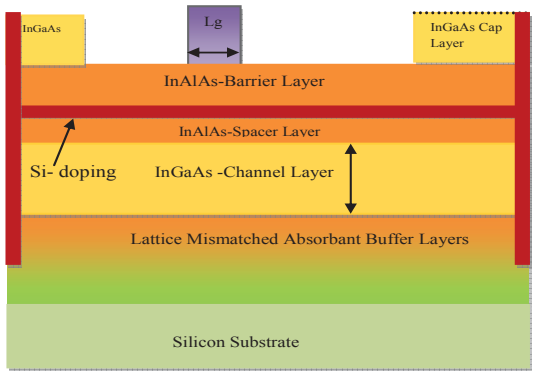

Figure 2. Schematic of InAlAs/InGaAs HEMT on Si substrate

Another approach involves the use of InP/GaAs [10] or InAsP/InP superlattice [11] layers to reduce dislocation density of InP on Si [12].Furthermore, strained-layer superlattice of InGaP has also been used to accommodate lattice mismatch as a buffer layer [13].

As compared to InP film on silicon with GaP buffer or InP on silicon without buffer, GaAs buffer layer is found to be more effective in reducing the residual stress and dislocation density in InP/Si [14]. Moreover, the formation of antiphase boundaries was successfully suppressed by using selective area overgrowth technique to grow InP on silicon substrate via Ge buffer [15].The use of intermediate buffer layer has successfully implemented silicon as a substrate for InAlAs/InGaAs HEMTs.

c) Epitaxial Lateral Overgrowth Technique

Epitaxial lateral overgrowth (ELOG) is one of the important technologies for realizing heteroepitaxy of III-V on silicon. This technique was first reported in 1980s [16] and was later extended for heteroepitaxial growth of InP on silicon [17, 18]. The primary objectives of ELOG are defect reduction and maximizing the amount of lateral growth vs. vertical growth to reduce the threading dislocations.

d) Non-epitaxial wafer bonding technique

The term wafer bonding refers to transfer of bulk or thin-film InP or other III-V compounds on Si substrates. The process of transferring thin film of InP on silicon wafer using proton implantation process and Si/SiO_2 wafer bonding technique has a potential application in associating III-V with Si technology [19].

Other schemes that have been developed to improve epilayer quality involve thermal annealing [20], growth on patterned Si substrates [21],[22] and use of ZnSe, Gd_2O_3 as intermediate layers between InP and Si substrate [23],[24].

IV. RECENT PROGRESS IN InAlAs/InGaAs HEMTs ON SILICON SUBSTRATE

InAlAs/InGaAs HEMTs are being intensively developed for high frequency and low noise applications. The possibility of epitaxy on silicon substrates promises lower manufacturing costs and hence wider application of such devices.

The first heteroepitaxial growth of high mobility metamorphic InAlAs/InGaAs Quantum well transistor on (100) silicon substrate was reported by S.Datta et al. using Molecular Beam Epitaxy (MBE).This depletion mode 0.08 μm gate length (Lg) device demonstrated a peak transconductance (g_m) of 930 mS/mm and cut off frequency (f_t) of 260 GHz. The misfit dislocations were predominantly contained in the 3.2 μm thick buffer layer. The performance characteristics of these heterogeneous III–V transistors on silicon substrate were found to be comparable with those previously achieved pseudomorphic InGaAs HEMTs on InP substrate [25].

Though the device performances were comparable, the thick buffer layers puts up additional cost in device fabrication and increases the device dimensions. The correlation between quality of active epitaxial layers and buffer thickness has been studied by M.K. Hudait et al. for InGaAs enhancement mode quantum well field effect transistor (QWFET).The buffer layer in this case consisted of GaAs and graded InAlAs layers grown on silicon substrate with the same orientation.

In this, the buffer thickness has been optimized to 1.3 μm from 3.2 μm with no detrimental effect on the channel mobility. This is because the thin buffer layer up to 1.3 μm successfully prevents the dislocations to penetrate the device epilayer and accommodates the lattice mismatch between the epilayers and silicon substrate [26] although it is usually reported that the threading dislocation density increases with decreasing thickness of buffer layer. The improvement in device performance has been attributed to improved transistor fabrication process. Although these devices have been proposed for low power applications, they provide a suitable roadmap for integration of high frequency RF devices with Si-CMOS platform.

K.M Lau et al. demonstrated 1.0 μm gate length InAlAs/InGaAs metamorphic HEMT (mHEMT) on 1.64 μm thick composite metamorphic buffer consisting of InAlAs/InP/GaAs low temperature (LT) and high temperature (HT) layers on (100) silicon substrate using MOCVD. This mHEMT exhibited a maximum transconductance of 587 mS/mm, cut off and maximum frequencies (f_{max}) of 32.3 and 44 GHz respectively [27].

Improvement in the RF performance of the above device was observed with gate length scaling from 1 μm to 0.3 μm without any change in the buffer layer thickness. The current gain cut-off frequency was 72.4 GHz, and the maximum oscillation frequency 77.3 GHz while the value of maximum transconductance increased up to 739 mS/mm. [28].

Table II presents a comparative view of RF performance of various InAlAs/InGaAs devices grown on GaAs, InP and Si substrates. Various device parameters like gate length, Indium mole fraction in InGaAs channel and growth process are also specified in the table for a more realistic comparison. Since, complementary-metal-oxide-semiconductor (CMOS) technology uses silicon substrates with (100) orientation, the table also indicates the compatibility for integration of InAlAs/InGaAs HEMTs with mainstream CMOS technology on a common Si (100) platform.

TABLE II. COMPARISION OF HEMTS ON VARIOUS SUBSTRATES

	Channel $In_xGa_{1-x}As$	Lg μm	f_t GHz	f_{max} GHz	g_m mS/mm	Growth	Ref.
Si (100)	$In_{0.53}Ga_{0.47}As$	1.0	32.3	44.0	587.0	MOCVD	[27]
	$In_{0.53}Ga_{0.47}As$	0.3	72.4	77.3	739.0	MOCVD	[26]
	$In_{0.7}Ga_{0.3}As$	0.08	260.0	-	930.0	MBE	[25]
GaAs	$In_{0.53}Ga_{0.47}As$	1.0	39.1	71.0	626.0	MOCVD	[4]
	$In_{0.53}Ga_{0.47}As$	0.15	279.0	231.0	1074.0	MOCVD	[5]
	$In_{0.6}Ga_{0.4}As$	0.08	235.0	290.0	1150.0	MBE	[33]
InP	$In_{0.7}Ga_{0.3}As$	1.0	30.0	35.0	280.0	MBE	[31]
	$In_{0.7}Ga_{0.3}As$	0.12	141.0	120.0	520.0	MBE	[34]
	$In_{0.7}Ga_{0.3}As$	0.08	250.0	-	1000.0	MBE	[32]

to improve as further work continues.

V. CONCLUSION

The high speed, high frequency and significantly low noise figure characteristics of InP based HEMTs have made it the technology of choice for various applications like low noise amplifiers, automotive radars, radio astronomy, and optoelectronic receivers. This technology has been made profitable by using InAlAs/InGaAs HEMTs on silicon substrate, which have established a comparative RF performance levels as of InP and GaAs based HEMTs.Also with the advancement in MBE and MOCVD technology, the virtual substrates can be made thinner without introducing dislocations. In addition to this, gate length scaling has resulted in better device performance in terms of transconductance and cut-off frequency. Therefore the replacement of much expensive InP substrates with silicon substrates promises even a wider usage of this device in future due to its economic and technological feasibility.

VI. FUTURE PROSPECTS

A novel path to integrate InP and GaAs based HEMTs on silicon substrate using step graded relaxed SiGe buffer layers with high Ge concentrations for eventual growth of the metamorphic GaAs up to InP epitaxial layer has been proposed by High performance Device Group (HPDG) of IIT Kharagpur. This approach benefits from the reduced mismatch between silicon and SiGe virtual substrate for epitaxial growth of GaAs and InP and would help to generate less dislocation in heterostructure than that of InP directly grown on silicon substrate. Further extension of metamorphic InP based devices on silicon through SiGe, binary-ternary phosphide towards InP will also be researched upon. Such efforts will spur further developments of InP on silicon substrate for high frequency RF as well as digital III-V technology.

We, High performance Device Group (HPDG) of IIT Kharagpur are working on the integration of compound semiconductor heterostructure devices on silicon substrate using MBE cluster tool based epitaxial nano-semiconductor infrastructure. This growth of III-V semiconductors on silicon substrate will serve as an integration pathway which otherwise could not be realized as SOHCOW.

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REFERENCES

[1] “ITRS update,”2010

[2] Personal Communication with Chris Baker ,University Wafer, 2011.

[3] Masafumi Yamaguchi, Akio Yamamoto, Naoto Uchida, Chikao Uemura, A new approach for thin film InP solar cells, *Solar Cells*, Volume 19, Issue 1, November 1986, Pages 85-96

[4] Haiou Li; Chak Wah Tang; Kei May Lau; , "Metamorphic InAlAs/InGaAs HEMTs on GaAs Substrates by MOCVD," *Electron Device Letters, IEEE* , vol.29, no.6, pp.561-564, June 2008

[5] Li, H.; Feng, Z.; Tang, C. W.; Lau, K. M.; , "Fabrication of 150-nm T-Gate Metamorphic InAlAs/InGaAs HEMTs on GaAs Substrates by MOCVD," *Electron Device Letters, IEEE* , vol.PP, no.99, pp.1-3

[6] Ababou, Y.; Masut, R. A.; Yelon, A.; Poulin, S.; , "Low temperature heteroepitaxy of InP on Si(111) substrates treated with buffered HF solution," *Applied Physics Letters* , vol.66, no.24, pp.3352-3354, Jun 1995

[7] Ababou, Y.; Desjardins, P.; Chennouf, A.; Leonelli, R.; Hetherington, D.; Yelon, A.; LEsperance, G.; Masut, R. A.; , "Structural and optical characterization of InP grown on Si(111) by metalorganic vapor phase epitaxy using thermal cycle growth," *Journal of Applied Physics* , vol.80, no.9, pp.4997-5005, Nov 1996

[8] C. A. Tran, R. A. Masut, P. Cova, J. L. Brebner, R. Leonelli, Growth and characterization of InP on silicon by MOCVD, *Journal of Crystal Growth*, Volume 121, Issue 3, July 1992, Pages 365-372

[9] Olego, D. J.; Tamura, M.; Okuno, Y.; Kawano, T.; Hashimoto, A.; , "Heteroepitaxial InP layers grown by metalorganic chemical vapor deposition on novel GaAs on Si buffers obtained by molecular beam epitaxy," *Journal of Applied Physics* , vol.71, no.9, pp.4329-4332, May 1992

[10] H. Horikawa, M. Akiyama, S. Onozawa, Y. Kawai, M. Sakuta, Interfacial layers of InP/Si heteroepitaxy, *Applied Surface Science*, Volumes 41-42, 2 November 1989, Pages 598-603, ISSN 0169-4332, DOI: 10.1016/0169-4332(89)90129-3.

[11] K.Araki,S.Has[egawa, H.Asahi, "Selective growth of InP on areas (1μm×1μm) of Silicon (100) substrate by molecular beam epitaxy," *Indium Phosphide and Related Materials, 2008. IPRM 2008. 20th International Conference on* , vol., no., pp.1-4, 25-29 May 2008

[12] Samonji, K.; Yonezu, H.; Takagi, Y.; Iwaki, K.; Ohshima, N.; Shin, J. K.; Pak, K.; , "Reduction of threading dislocation density in InP-on-Si heteroepitaxy with strained short-period superlattices," *Applied Physics Letters* , vol.69, no.1, pp.100-102, Jul 1996

[13] Crumbaker, T.E.; Hafich, M.J.; Robinson, G.Y.; Davis, A.; Lorenzo, J.P.; , "Heteroepitaxy of InP on Si: variation of electron concentration and mobility with depth," *Indium Phosphide and Related Materials, 1990. Second International Conference.* , vol., no., pp.131-134, 23-25 Apr 1990

[14] Mitsuru Sugo, Masafumi Yamaguchi, M.M. Al-Jassim, Heteroepitaxial growth of InP on Si substrates, *Journal of Crystal Growth*, Volume 99, Issues 1-4, January 1990, Pages 365-370

[15] Wang, G.; Leys, M. R.; Loo, R.; Richard, O.; Bender, H.; Waldron, N.; Brammertz, G.; Dekoster, J.; Wang, W.; Seefeldt, M.; Caymax, M.; Heyns, M. M.; , "Selective area growth of high quality InP on Si (001) substrates," *Applied Physics Letters* , vol.97, no.12, pp.121913-121913-3, Sep 2010

[16] Tsaur, B-Y.; McClelland, R. W.; Fan, John C. C.; Gale, R. P.; Salerno, J. P.; Vojak, B. A.; Bozler, C. O.; , "Low-dislocation-density GaAs epilayers grown on Ge-coated Si substrates by means of lateral epitaxial overgrowth," *Applied Physics Letters* , vol.41, no.4, pp.347-349, Aug 1982

[17] Sun, Y.T.; Napierala, J.; Lourdudoss, S.; , "Selective area growth of InP on InP precoated silicon substrate by hydride vapor phase epitaxy," *Indium Phosphide and Related Materials Conference, 2002. IPRM. 14th* , vol., no., pp. 339- 342, 2002

[18] Zhechao Wang; Junesand, C.; Metaferia, W.; Chen Hu; Lourdudoss, S.; Wosinski, L.; , "InP lateral overgrowth technology for silicon photonics," *Communications and Photonics Conference and Exhibition (ACP), 2010 Asia* , vol., no., pp.377-378, 8-12 Dec. 2010

[19] Jalaguier, E.; Aspar, B.; Pocas, S.; Michaud, J.F.; Papon, A.M.; Bruel, M.; , "Transfer Of Thin Inp Films Onto Silicon Substrate By Proton Implantation Process," *Indium Phosphide And Related Materials, 1999. IPRM. 1999 Eleventh International Conference On* , Vol., No., Pp.26-27 Suppl., 1999

[20] Y. Kohama, Y. Kadota, and Y. Ohmachi, "Heteroepitaxy of InP on Si substrates by MOCVD," *J. Electrochem. Soc*., Volume 136, Issue 12, pp. 3853-3856 (1989)

[21] Schnabel, R.F.; Grundmann, L.; Krost, A.; Christen, J.; Heinrichsdorff, F.; Bimberg, D.; Cerva, H.; , "Defect reductions and strain relaxation mechanisms in InP grown on patterned Si(001)," *Indium Phosphide and Related Materials, 1994. Conference Proceedings., Sixth International Conference on* , vol., no., pp.640-643, 27-31 Mar 1994

[22] Hasegawa, S.; Yamano, A.; Ahn, N.S.; Cha, N.G.; Kanki, T.; Tanaka, H.; Asahi, H.; , "Selective area growth of InP on nano-patterned SiO2/Si(100) substrates by molecular beam epitaxy," *Indium Phosphide & Related Materials (IPRM), 2010 International Conference on* , vol., no., pp.1-4, May 31 2010-June 4 2010

[23] Lee, M. K.; Wuu, D. S.; Tung, H. H.; Chang, J. H.; Lin, Y. F.; , "Growth and characterization of InP epilayers on ZnS;coated Si substrates by low-pressure metalorganic vapor phase epitaxy," *Applied Physics Letters* , vol.53, no.2, pp.107-109, Jul 1988

[24] Saint-Girons, G.; Regreny, P.; Largeau, L.; Patriarche, G.; Hollinger, G.; , "Monolithic integration of InP based heterostructures on silicon using crystalline Gd_2O_3 buffers," *Applied Physics Letters* , vol.91, no.24, pp.241912-241912-3, Dec 2007

[25] Datta, S.; Dewey, G.; Fastenau, J.M.; Hudait, M.K.; Loubychev, D.; Liu, W.K.; Radosavljevic, M.; Rachmady, W.; Chau, R.; , "Ultrahigh-Speed 0.5 V Supply Voltage $In_{0.7}$ $Ga_{0.3}As$ Quantum-Well Transistors on Silicon Substrate," *Electron Device Letters, IEEE* , vol.28, no.8, pp.685-687, Aug. 2007

[26] Hudait, M.K.; Dewey, G.; Datta, S.; Fastenau, J.M.; Kavalieros, J.; Liu, W.K.; Lubyshev, D.; Pillarisetty, R.; Rachmady, W.; Radosavljevic, M.; Rakshit, T.; Chau, R.; , "Heterogeneous integration of enhancement mode $In_{0.7}Ga_{0.3}As$ quantum well transistor on Silicon substrate using thin (<2 μm) composite buffer architecture for high-speed and low-voltage (0.5 v) logic applications," *Electron Devices Meeting, 2007. IEDM 2007. IEEE International* , vol., no., pp.625-628, 10-12 Dec. 2007

[27] Lau, K.M.; Chak Wah Tang; Haiou Li; Zhenyu Zhong; , "InAlAs/InGaAs mHEMTs on Silicon substrates grown By MOCVD," *Electron Devices Meeting, 2008. IEDM 2008. IEEE International* , vol., no., pp.1-4, 15-17 Dec. 2008

[28] Hai-Ou Li; Ming Li; Chak Wah Tang; Zhen Yu Zhong; Kei May Lau; , "0.3-μm gate-length metamorphic InAlAs/InGaAs HEMTs on Silicon substrates by MOCVD," *Solid-State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on* , vol., no., pp.1374-1376, 1-4 Nov. 2010

[29] Bollaert, S.; Wallaert, X.; Lepilliet, S.; Cappy, A.; Jalaguier, E.; Pocas, S.; Aspar, B.; , "0.12 μm transferred-substrate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}$ As HEMTs on Silicon wafer," *Electron Device Letters, IEEE* , vol.23, no.2, pp.73-75, Feb 2002

[30] Wichmann, N.; Duszynski, I.; Wallart, X.; Bollaert, S.; Cappy, A.; , "InAlAs-InGaAs double-gate HEMTs on transferred substrate," *Electron Device Letters, IEEE* , vol.25, no.6, pp. 354- 356, June 2004

[31] A. Bouloukou, B. Boudjelida, A. Sobih, S. Boulay, J. Sly, M. Missous, Very low leakage InGaAs/InAlAs pHEMTs for broadband (300 MHz to 2 GHz) low-noise applications, *Materials Science in Semiconductor Processing*, Volume 11, Issues 5-6, E-MRS 2008 Spring

Conference Symposium J: Beyond Silicon Technology: Materials and Devices for Post-Si CMOS, October 2008, Pages 390-393

[32] Lai, R.; Barsky, M.; Huang, T.; Sholley, M.; Wang, H.; Kok, Y.L.; Streit, D.C.; Block, T.; Liu, P.H.; Gaier, T.; Samoska, L.; , "An InP HEMT MMIC LNA with 7.2-dB gain at 190 GHz," *Microwave and Guided Wave Letters, IEEE* , vol.8, no.11, pp.393-395, Nov 1998

[33] Hyung Sup Yoon; Jae Yeob Shim; Dong Min Kang; Ju Yeon Hong; Kyung Ho Lee; , "Characteristics of 80 nm T-Gate Metamorphic HEMT with 60 % Indium Channel," *Indium Phosphide & Related Materials, 2007. IPRM '07. IEEE 19th International Conference on* , vol., no., pp.110-113, 14-18 May 2007

[34] Huang Jie;Guo Tianyi; Zhang Haiying; Xu Jingbo; Fu Xiaojun; Yang Hao and Niu Jiebin; , "120-nm gate-length $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ InP-based HEMT," J. Semicond *31,2010*