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# Virtual Fabrication and Analog Performance of Sub-40nm Bulk MOSFET Using TCAD TOOL

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ABSTRACT

Virtual Fabrication of sub-40nm Bulk MOSFET is carried out under channel engineering and source drain engineering process. These structures enable more aggressive device scaling in nano-scale region because of their ability to control short channel effects. How ever during scaling the junction depth should also be scaled down, which increases parasitic resistance so silicidation technique has been applied to reduce their effects on device. Analog performance has been measured in terms of gm, gds ,Av ,$f_T$ and $f_{max}$ .The simulation result predict that $g_m$ is 3.75ms for engineered MOSFET as compared to non-engineered MOSFET with $g_m$ of 2.9ms for similar gate length, similarly $A_v$ for engineered device is 17.5db and for non-engineered device is 6.96db,$f_T$ is 146GHz and for non-engineered $f_T$ is 65GHz,$f_{max}$ is 299GHz for engineered device and for non-engineered device $f_{max}$is 170GHz and a comparison of an engineered device is done with a non engineered device to investigate the improved performance of an engineered device as compared to a non engineered device. Silvaco TCAD Tool is used for Virtual fabrication and simulation. ATHENA process simulator is used for virtual fabrication and ATLAS device simulator is used for device characterization.

## I. INTRODUCTION

The Scaling of MOSFET device to sub40nm is very critical because of short channel effect. The SCE is mainly due to power supply since scaling of device is more rapid as compared to The scaling of supply voltage result is the SCE, because of high electric field degrades the mobility and causes velocity saturation. The gate looses control and short channel device is controlled by both gate and drain biase, the drain voltage gives more influence to the channel potential in nanoscale MOSFET[1].

According to ITRS roadmap[2],a precisely controlled process flow for the incorporation of new materials in Si CMOS technology is crucial for nanoscale devices. Also,an increased functionality at low cost leads an excessive high packaging density for VLSI chips, leads to an aggressive scaling of MOSFETs[3].

In this paper by using TCAD simulator we have used advances fabrication process such as: lightly doped drain(LDD) to reduce peak electric field and to provide shallow junctions adjacent to the channel, halo implantation to reduce punch through and hence called punch through stopper, retrograded p-well implant for latch-up immunity, and metal silicide $TiSi_2$ is used to reduce the sheet resistance. A comparison of an engineered device is done with a non engineered one to investigate the improved performance of an engineered device with respect to short channel effects and also an improved analog performance.

## II. PROCESS SIMULATION

The process simulation uses ATHENA as a simulator that provides general capabilities for numerical, physically based, two dimensional simulation of semiconductor processing. In process simulation, the result of an implantation step is mostly described by a so-called pearson function where as the diffusion equation is solved to derive the influence of an annealing step.

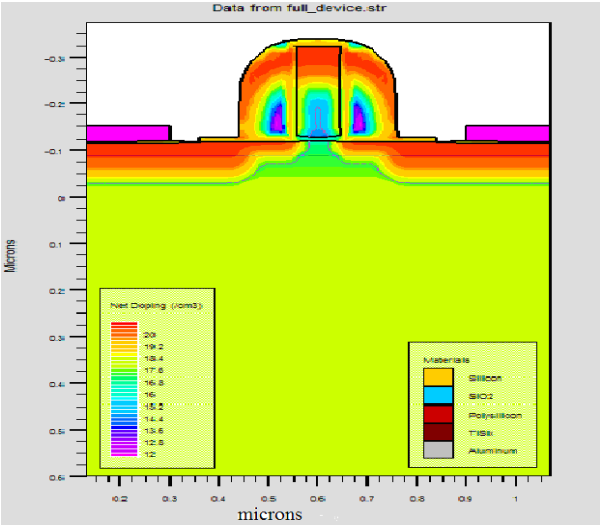



Fig. 1: Device structure obtained ATHENA simulator

The process steps are taken from Table1 and from reference paper[3,4].The initial grid has to be defined before any further steps of the design. A fine grid exist to those area of simulation structure where ion implantation will occur, where p-n junction will be formed. A retrograded p-well implantation is done with $BF_2$ at 90kev at 950°C.$Sio_2$ is deposited at 650-750°C using thermal oxidation by decomposing TEOS for sacrificial cleaning called screening oxide and is latter removed[7]. As the device is scaled the thickness of gate oxide must be scaled in order to overcome short channel effect. So a gate oxide of 25A° is then grown which is shown in the result after simulation.

As the device dimension is reduced, if voltage level are not correspondingly scaled down, electric field inside the device will rise, result in hot electron effect in the channel region to overcome this problem a lightly doped drain (LDD) structure is used to reduce the peak electric field across the channel. For NMOS device halo implant, which are deeper than the reach through but not as deep as the contact S/D are used on LDD structure to reduce SCE.A high dose of arsenic for NMOS is implanted with 50kev to build low resistance of source and drain region. Introduction of dopant atom into semiconductor is the only steps in changing the electrical property. The implantation damages the target and displaces many atom for each implanted ion. Annealing is required to repair lattice damage and put the dopant atom on substitutional site where they will be electrically active.

TABLE 1: Process Flow of 40nm NMOS used in SILVACO ATHENA process simulator

| Process | NMOS |
|---|---|
| Initial Substrate | p-type($2*10^{18}$per $cm^3$) |
| Epitaxial Layer | p-type($4*10^{16}$ per $cm^3$) |
| p-well implant | $BF_2$($1*10^{13}$), Energy=100kev |
| TEOS isolation and etch of oxide | 10nm (diffusion at 650°C) |
| Gate oxide growth | 2.5nm (At 650°C,dry $o_2$) |
| Poly deposition and etching for S/D | 200nm (p-type $1*10^{15}$) |
| Shallow S/D implant | Phosphorus($8*10^{13}$,10kev) |
| Halo implant | p-type($1*10^{13}$), Energy=15kev/30° angle |
| Spacer deposition | 100nm |
| Deep S/D implant | As($7*10^{14}$), Energy=50kev |
| Ti Silicide | 25nm Ti on S/D and gate |
| Final RTA anneal | 650-750°C for 30s and 1min |
| Metal deposition | Al-30nm |

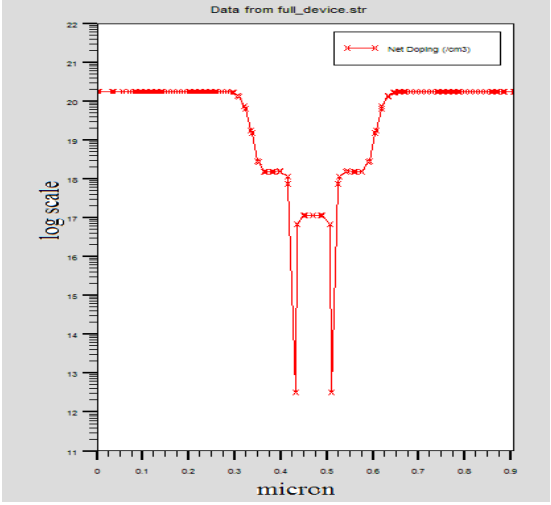



Fig2: Net doping profile through cut line taken across S/D and across the channel.

The resistivity of even heavily doped silicon is too large, in those case it is common to form metal silicide on top of the exposed silicon to reduce the resistivity. $TiSi_2$ is most desirable film for many application due to its low resistivity. During silicide formation anneal, however leads to over growth of the silicide on top of the edge of the oxide. This growth can be minimized by first annealing at low temperature to form TiSi and high temperature RTA around 750°C to form silicide[6]. Final device structure of a 40nm of n-channel MOSFET is shown in figure1.

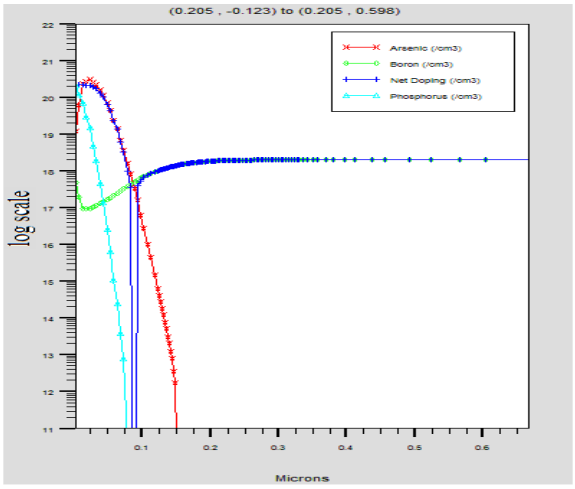



Fig3: Doping concentration vs depth of implant for Si MOSFET for different dopant

## III.DEVICE SIMULATION

The result of process simulator developed from ATHENA were used as the input for a device simulator Silvaco Tool ATLAS and device characteristics can be examined. This provides an easy way of studying the effects of process parameter on device performance and both device structure and fabrication process can thus be optimized. A comparison of an engineered device is done with a non-engineered device to investigate the improved performance of an engineered device compared to a non-engineered one.

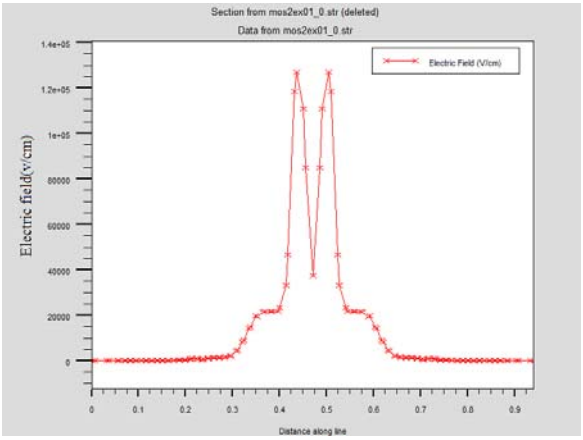



Fig4: Electric field across S/D and the channel: showing reduced electric field to minimize SCE.

The simulated DC output characteristics is shown in Fig5 for W/L of 10/0.04um for gate voltage varies from 0.3V to 1.5V.Sub-threshold characteristics is shown in Fig6 (a) and a sub-threshold of 77mV/dec is extracted, which indicates that the leakage current is greatly minimized for an engineered device. When a small channel length MOSFETs are not scaled properly and the source/drain junctions are too deep or the channel doping is too low, there can be unintended electrostatic interactions between the source and the drain known as Drain Induced Barrier Lowering (DIBL). This leads to punch-through leakage or breakdown between the source and the drain, and loss of gate control. . The result is a different curve of ID-VG after different value of drain voltage with respect to the source is applied. The simulation will use the structure file created from the previous Athena simulation. The simulation result is shown in Figure 6(b). A comparison of an engineered device is done with a non-engineered device is shown in fig7 shows an improved performance. Fig7 (a) shows sub-threshold characteristics of both engineered as well as non-engineered device and shows an improvement when using channel engineering process, while Fig7(b) shows the output characteristics of both the device and shows enhancement in drain current of same bias condition.

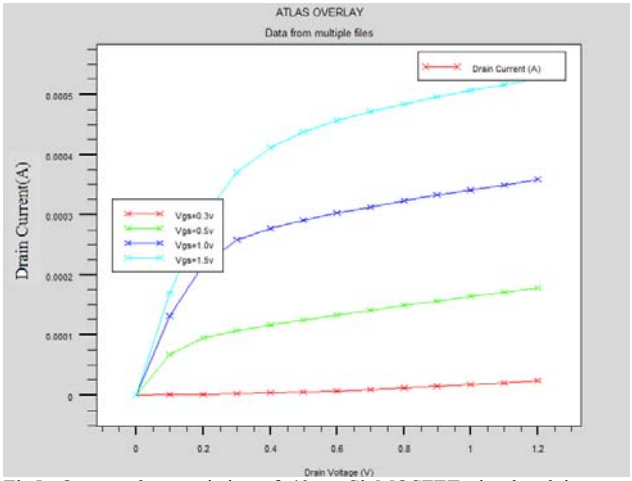
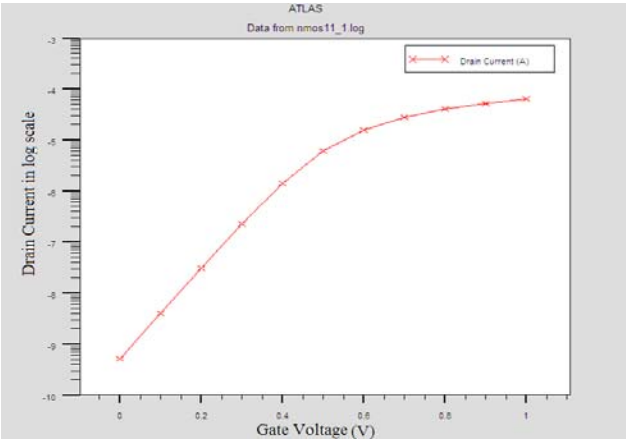
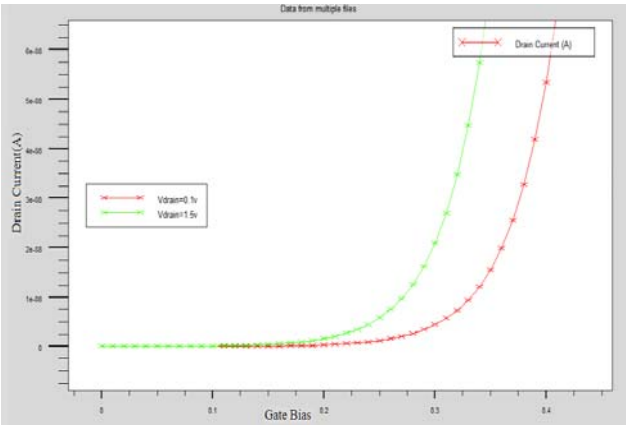



Fig5: Output characteristics of 40nm Si MOSFET simulated in ATLAS device simulator.

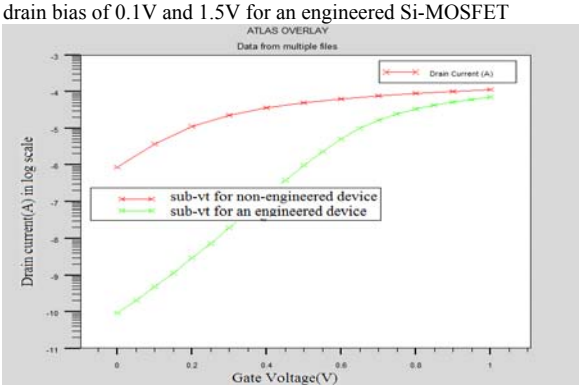



(a)

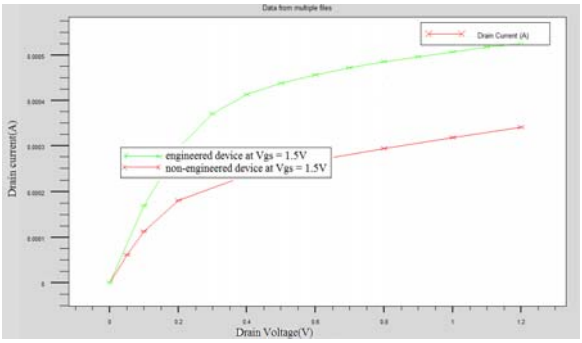



(b)

Fig6: (a) Sub-threshold characteristics for engineered Si MOSFET. (b) DIBL characteristics between drain current vs gate bias: For drain bias of 0.1V and 1.5V for an engineered Si-MOSFET




(a)




(b)

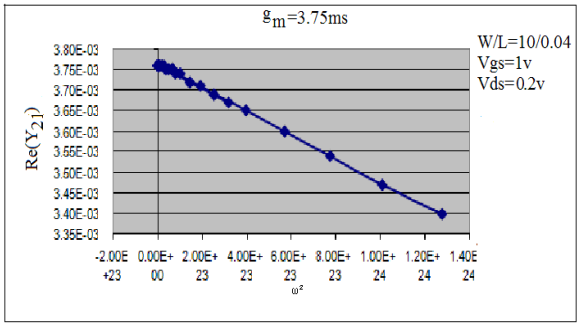
Fig7.(a) Sub-threshold characteristics for an engineered and non-engineered Si MOSFET.(b) Output characteristics of both the device at Vgs of 1.5V and channel length of 40nm.

## IV.PERFORMANCE INVESTIGATION

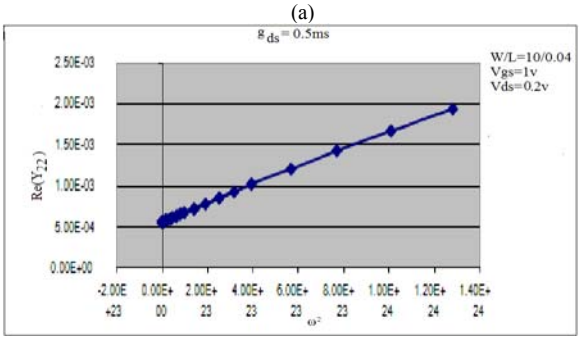
The performance investigation is done in terms of trans-conductance ($g_m$), output conductance ($g_{ds}$), voltage gain ($A_v$), transistor cutoff frequency($f_T$) and maximum frequency of oscillation ($f_{max}$)[3,7], and also a comparison is made for an engineered device with a non-engineered device of same channel length. The extraction of Y and h parameter is done from the simulation result for $g_m$, $g_{ds}$, and frequency response of Si n-MOSFET.

$$Re(Y_{21}) = g_m \text{ where } \omega^2 = 0 \quad (1)$$
$$Re(Y_{22}) = g_{ds} \text{ where } \omega^2 = 0 \quad (2)$$

and the extracted value of trans conductance ($g_m$) is 3.75ms is shown in Fig8 (a) and output conductance ($g_{ds}$) is 0.5ms is shown in Fig8 (b) and is also compared with a non engineered device is shown in Fig9(a), and Fig9(b), which clearly shows a great improved performance of an engineered Si MOSFET of same channel length. An important measure of RF transistor is the cutoff frequency $f_T$. This is the frequency at which the small signal current gain h21 of the transistor rolls off to unity (i.e., 0 dB).For an engineered Si MOSFET $f_T$ is 146GHz and for non-engineered $f_T$ is 65GHz as is shown in Fig10. The maximum frequency of oscillation ($f_{max}$) is extracted from maximum unilateral power gain Vs frequency plot is the frequency at which unilateral power gain become unity (i.e,0dB) which is shown in Fig11. For engineered. device $f_{max}$ is 299GHz and for non-enginee-red device $f_{max}$ is 170GHz

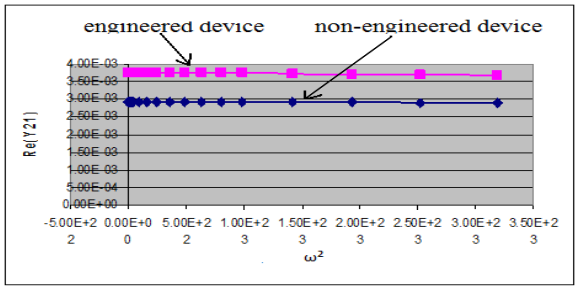



(a)

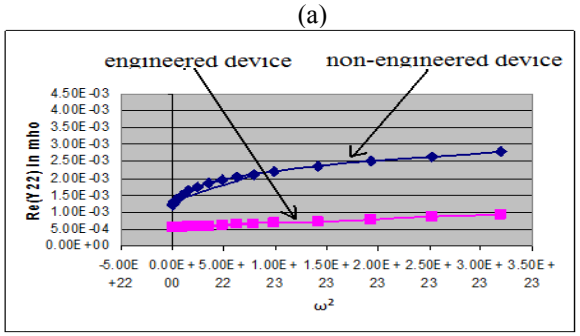



(b)

Fig 8: (a) $Re(Y_{21})$ Vs $\omega^2$ curve :For $g_m$ calculation of Si MOSFET and its value is 3.75ms. (b) $Re(Y_{22})$ Vs $\omega^2$ : Shows $g_{ds}$ extraction and its value is 0.5ms.




(a)




(b)

Fig9: (a) $Re(Y_{21})$ Vs $\omega^2$ for engineered and non-engineered Si n-MOSFET :$g_m$ for engineered device is 3.75ms and for non-engineered device $g_m$ is 2.9ms. (b) $Re(Y_{22})$ Vs $\omega^2$ :For engineered MOSFET $g_{ds}$ is 0.5ms and for non-engineered it is 1.2ms.

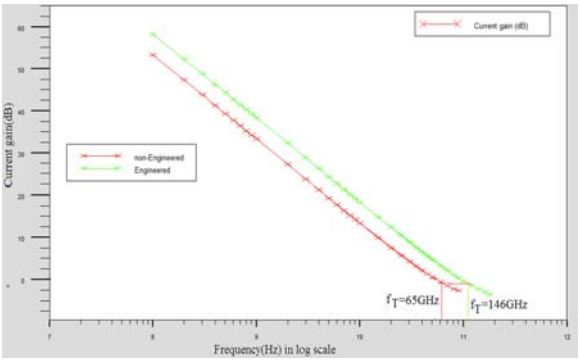



Fig10. Current gain(dB) Vs frequency : Cut of frequency of engineered Si n-MOSFET is 146GHz and for non-engineered Si n-MOSFET is 65GHz.

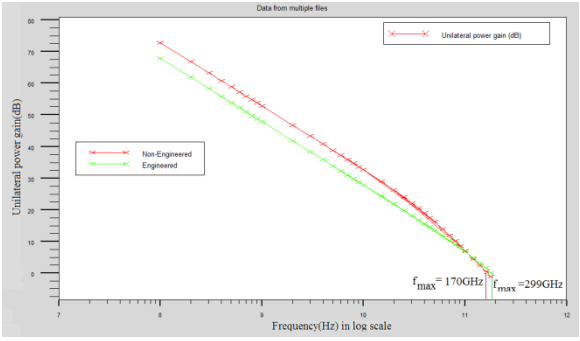



Fig11.Unilateral power gain Vs Frequency : $f_{max}$ for engineered Si n-MOSFET is 299GHz and for non-engineered MOSFET it is 170GHz.

## V.CONCLUSSION

The goal of this paper is to design a NMOS with channel length of 40nm has been achieved. Several advanced technique such as retrograde well, halo implant and light doped drain (LDD) has been applied to investigate the effectiveness of these techniques to suppress the short channel effects. Advanced CMOS processes such as retrograde well and halo implant reduces the threshold voltage variation (short channel effects). Halo and retrograde-well suppresses DIBL effect while LDD reduces the peak value of the electric field in the near drain region, which is less susceptible to "short channel effects" or drain-induced-barrier-lowering (DIBL). These techniques have shown good results in preventing the varying of the threshold voltage. The accuracy of the design can be determined from the output characteristics of the device simulation. As long as the characteristic does not exhibits punch-through effect the design is considered acceptable. This is because the short channel effects have an impact on threshold voltage, sub threshold currents, and I-V behavior beyond threshold. A comparison of an engineered device is performed with non-

engineered device and shown an improved performance of an engineered device

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