International Journal of Power System Operation and Energy Management

Volume 1 | Issue 1 Article 3

January 2012

A Space Vector PWM Scheme for Three level Inverters Based on Two-Level Space Vector PWM

D. Sandhya Rani
GMRIT,Rajam, sandhya_dollu@yahoo.com

A. Appaprao
GMRIT,Rajam, apparao.a@gmrit.org

A Space Vector PWM Scheme for Three level Inverters Based on Two-Level Space Vector PWM

D. Sandhya Rani [1], A.Appaprao[2]
GMRIT,Rajam
Email: sandhya_dollu@yahoo.com[1], apparao.a@gmrit.org[2]

ABSTRACT

Multilevel inverters are increasingly being used in high-power medium voltage applications due to their superior performance compared to two-level inverters. Among various modulation techniques for a multilevel inverter, the space vector pulse width modulation (SVPWM) is widely used. The complexity is due to the difficulty in determining the location of the reference vector, the calculation of on-times, and the determination and selection of switching states. This paper proposes a general SVPWM algorithm for multilevel inverters based on standard two-level SVPWM. Since the proposed multilevel SVPWM method uses two-level modulation to calculate the on-times, the computation of on-times for an *n*-level inverter becomes easier. The proposed method uses a simple mapping to achieve the SVPWM for a multilevel inverter. A general *n*-level implementation is explained, and experimental results are given for two-level and three-level inverters.

***Index Terms*—Multilevel inverter, neutral point clamped (NPC), space vector pulse width modulation (SVPWM), switching state, two-level inverter**

I. INTRODUCTION

To control multilevel converters, the pulse width modulation (PWM) strategies are the most effective, especially the space vector pulse width modulation (SVPWM) one, which has equally divided zero voltage vectors describing a lower total harmonic distortion (THD) [5]. Although the complexity that presents the SVPWM strategy (many output vectors) compared with the carrier-based PWM one, it remains the preferred seen that it reduces the power losses by minimizing the power electronic Devices switching frequency (limiting the minimum pulse width). For the high performance AC drive systems at increased power levels, high quality inverter output is necessary for the low harmonic losses and torque pulsation. In the conventional two-level inverter configurations, the reduction of the harmonic contents of the inverter output current is achieved mainly by raising the switching frequency. However in the field of high voltage, high power application, the switching frequency of the power devices has to be restricted below lkhz, due to the increased switching losses, even in case of the HVJGBT and GCT. So the harmonic reduction by raised switching frequency of the two-level inverter becomes more difficult in high power applications. In addition, in two-level configurations, the DC link voltage of the two-level inverter is limited by the voltage ratings of the switching devices, so the problematic series connection of the switching devices is required to raise the DC link voltage. By series connection, the maximum allowable switching frequency has to be more lowered, thus the harmonic reduction becomes more difficult. From the aspect of the harmonic reduction and the higher voltage level, three-level approach seems to be most promising alternative. The harmonic contents of the three-level inverter are less than that of two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the DC-link voltage. So the three-level inverter topology is generally used in realizing the high performance, high voltage AC drive systems.

II. Inverter Topology

Fig. 1 shows the popular topology of diode-clamped (neutral-point clamped) three-level inverter. The circuit employs 12 power switching devices (e.g. **Sl-S4**a)n d 6clamped diodes (e.g. ***Dj-D6).*** And the dc-bus voltage is split into three-level by two series-connected bulk capacitors, ***C,*** and C,. The middle point of the two capacitors can be defined as the neutral point ***0.*** **As** the result **of** the diode clamped, the switch voltage is limited to half the level of the dc-bus voltage Ud2. Thus, the voltage stress of switching device is greatly reduced. The output voltage ***tiAo*** has three different states: ***+Ud2,0***a,n d -Ud2. Here takes phase **A** as an example. For voltage level ***+Ud2,*** Sl and **S,** need to be turned on; for 0 level, ***S,*** and ***S,*** need to be turned on; and for ***-Ud2,S,*** and S4 need to be turned on. We can define these states as 2, 1, and 0, respectively. Then, the switching variable **So** is shown in Table **1,** Be similar to three-phase two-level inverter, the switching states of each bridge leg of three-phase three level inverter is described by using switching variables ***So,*** **S,** and **S,.** Whereas the difference is that, in three-level inverter, each bridge leg has three different switching stat e **s.**

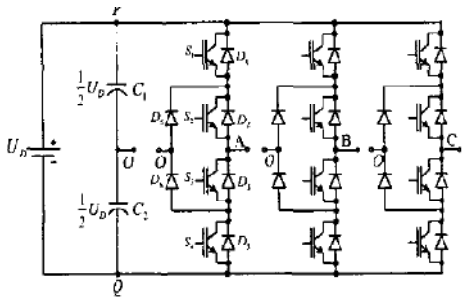


Fig-
Schematic of the Diode-clamped three-level inverter

TABLE I
THE SWITCHING VARIABLE OF PHASE A

U_{an}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_a
$+U_D/2$	1	1	0	0	2
0	0	1	1	0	1
$-U_D/2$	0	0	1	1	0

Using switching variable *S,,* and dc-bus voltage *Uo,* thevoutput phase voltage ***U,,"*** is obtained **as** follows:
The switching
states
And the output line voltage of phase A and B can be expressed **as** follows:
1
2
Ll,n =U, " -urn = - ***UD*** . (*g* - s,)
The matrix form of output line voltage equations is given **as** follow:Let now apply the Concordia transformation to the vector *Vin* giving it in the diphase (α - β) frame:

$$\begin{bmatrix} u_{AB} \\ u_{BC} \\ u_{CA} \end{bmatrix} = \frac{1}{2} U_D \cdot \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix}$$

III. Space vector PWM Modulation

As shown in Fig..**,** there are altogether **27** switching States in diode-clamped three-level inverter. They correspond to 19 voltage vectors *(VO* to VIE) whose Positions are fixed. These space voltage vectors can be classified into 4 groups: large voltage vector (VI,, VI, etc.), medium voltage vector *(V,, V,,* etc.), small voltage vector (VI, *Vz,* etc.), and zero voltage vector *(Vo).* The plane can be divided into 6 major triangular sectors (I to VI enclosed by solid lines) by large voltage vectors and zero voltage vector. Each major section represents *60'* of the fundamental cycle. Within each major sector, there are 4 minor triangular sectors (enclosed by the dotted lines). There are totally **24** minor sectors in the plane. And the vertices of these sectors represent the voltage vectors. Notice Table 11, each small voltage vector and zero voltage vector have **2** and **3** redundant switching states, respectively. This will be analyzed in detail in Section IV. In three-phase three-level inverter, when the rotating voltage vectors falls into one certain sector, adjacent voltage vectors are selected to synthesize the desired rotating voltage vector based on the vector synthesis principle, resulting in three-phase PWM waveforms. By the examination of the phase angle and the magnitude of a rotating reference voltage vector ?, the sector wherein ***v'*** resides can be easily located..

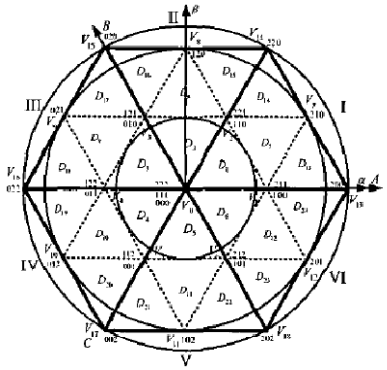


Fig. 2. Space vector diagram of three-level inverter

TABLE II
THE SWITCHING STATES AND THE CORRESPONDING VOLTAGE VECTORS

The switching states	S_a	S_b	S_c	The corresponding Voltage vectors
S_1	0	0	0	V_0
S_2	1	1	1	V_0
S_3	2	2	2	V_0
S_4	1	0	0	V_1
S_5	1	1	0	V_2
S_6	0	1	0	V_3
S_7	0	1	1	V_4
S_8	0	0	1	V_5
S_9	1	0	1	V_6
S_{10}	2	1	1	V_7
S_{11}	2	2	1	V_8
S_{12}	1	2	1	V_9
S_{13}	1	2	2	V_{10}
S_{14}	1	1	2	V_{11}
S_{15}	2	1	2	V_{12}
S_{16}	2	1	0	V_{13}
S_{17}	1	2	0	V_{14}
S_{18}	0	2	1	V_{15}
S_{19}	0	1	2	V_{16}
S_{20}	1	0	2	V_{17}
S_{21}	2	0	1	V_{18}
S_{22}	2	0	0	V_{19}
S_{23}	2	2	0	V_{20}
S_{24}	0	2	0	V_{21}
S_{25}	0	2	2	V_{22}
S_{26}	0	0	2	V_{23}
S_{27}	2	0	2	V_{24}

If the triangle sector is defined by vector *Vx, V,,* and *V:,*then ? can be synthesized by *V,, V,,* and V? Assuming the duration of vector V, **yK,** and k: are *T,, T,,* and *T;* respectively, and ***T,+Tv+Tx=Ts,*** where *T,* is switching

period. T h,e′n*i X,* and *2* can be defined **as** the following equations:

$$X = \frac{T_a}{T_s}$$

$$Y = \frac{T_b}{T_s}$$

$$Z = \frac{T_c}{T_s}$$

Based on the principle of vector synthesis, the following equations can be written:

$$X + Y + Z = 1$$

$$V_a X + V_b Y + V_c Z = V^*$$

The modulation ratio of three-phase three-level inverter is represented as follows:

$$m = \frac{|V^*|}{\frac{2}{3}U_D} = \frac{3|V^*|}{2U_D}$$

Where *(V'l* is the magnitude of the reference voltage vector **f,** which rotates with an angle speed of ***w=27cf*** in ***d-q*** coordinate plane. And 2/3UD is magnitude the of the large voltage vector, e.g. *VI,*. As shown in Fig. 3, the boundaries of modulation ratio are Markl, Mark2, and Mark3. The equation forms **of** them are obtained as follows:

$$Mark1 = \frac{\sqrt{3}/2}{\sqrt{3}\cos\theta + \sin\theta}$$

$$Mark2 = \begin{cases} \dfrac{\sqrt{3}/2}{\sqrt{3}\cos\theta - \sin\theta}, & \theta \le \dfrac{\pi}{6} \\ \dfrac{\sqrt{3}/4}{\sin\theta}, & \dfrac{\pi}{6} < \theta \le \dfrac{\pi}{3} \end{cases}$$

$$Mark3 = \frac{\sqrt{3}}{\sqrt{3}\cos\theta + \sin\theta}$$

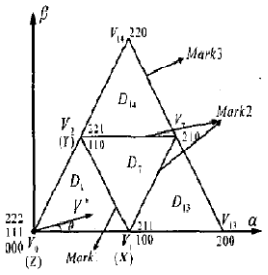


Fig. 3. The space vector diagram of sector I

Here takes an example. **As** illustrate! in Fig. 3, we can suppose that the rotating voltage *Y* falls into sector 1(0<8<60°). Notice that there are 4 minor sectors, *D,, D,,* Dl,, and Dl, in this sector, then *X, Y,* and *Z* can be calculated with the following four cases, respectively. ***A.*** When the modulation ratio m<Markl, the rotating voltage vector **f** is in sector Dl. As shown in Fig. 3, **f** is synthesized by *Yo,* VI, and *VI.* According to **(8),** the following equation is acquired

$$\frac{1}{2}X + \frac{1}{2}\left[\cos\left(\frac{\pi}{3}\right)Y + j\sin\left(\frac{\pi}{3}\right)\right]Y = m\left[\cos(\theta) + j\sin(\theta)\right]$$

$$\begin{cases} X = 2m \cdot \left[\cos(\theta) - \dfrac{\sin(\theta)}{\sqrt{3}}\right] \\ Y = m \cdot \dfrac{4\sin(\theta)}{\sqrt{3}} \\ Z = 1 - 2m\left[\cos(\theta) + \dfrac{\sin(\theta)}{\sqrt{3}}\right] \end{cases}$$

C. When **Mark%m<Mark3** and 0<8<30°, *Y** is inpector **Dll.** *V,,* VI,, and ***V7*** are selected to synthesize *Y* . The durations of them are obtained as follows:

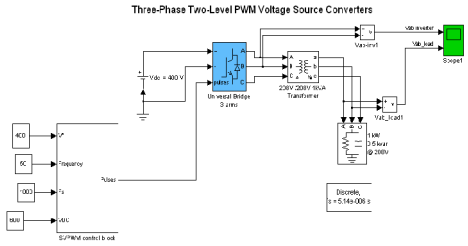
$$\begin{cases} X = -1 + 2m \cdot \left[\cos(\theta) - \dfrac{\sin(\theta)}{\sqrt{3}}\right] \\ Y = m \cdot \dfrac{4\sin(\theta)}{\sqrt{3}} \\ Z = 2 - 2m \cdot \left[\cos(\theta) + \dfrac{\sin(\theta)}{\sqrt{3}}\right] \end{cases}$$

D. When Mark2<m<Mark3 and 3O0<S<60", **h'*** is in sector DI4. Vectors ***V2, V7,*** and VI, will be employed togenerate the required voltage. *X, Y,* and *Z* can be expressed **as** follows:

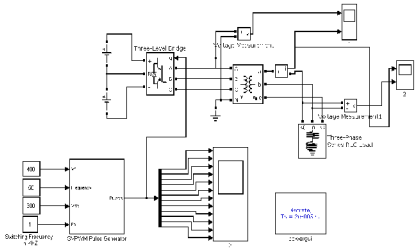
$$\begin{cases} X = 2m \cdot \left[\cos(\theta) - \dfrac{\sin(\theta)}{\sqrt{3}}\right] \\ Y = -1 + m \cdot \dfrac{4\sin(\theta)}{\sqrt{3}} \\ Z = 2 - 2m \cdot \left[\cos(\theta) + \dfrac{\sin(\theta)}{\sqrt{3}}\right] \end{cases}$$

When the reference vector falls into the others major sectors, similar argument can be applied. Replacing *8* of (14), **(15),** (16), and (17) by 8-60', 8-120', O-180°, **8-240',** and 8-300' respectively, the calculation of the entire coordinate plane can be established.

IV. Matlab /Simulink model

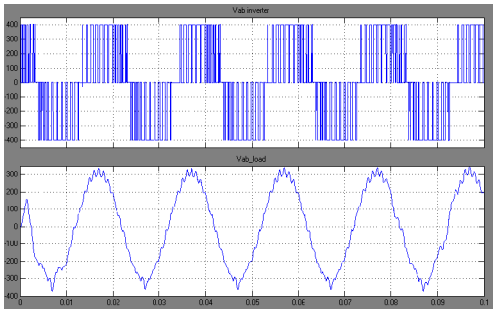


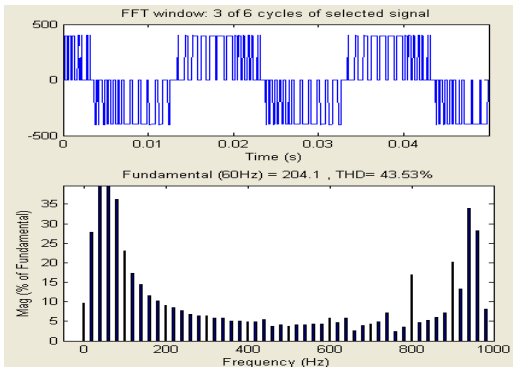
Space Vector Diagram of Three Level Inverter

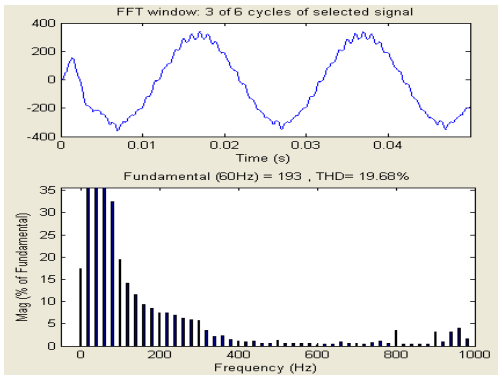


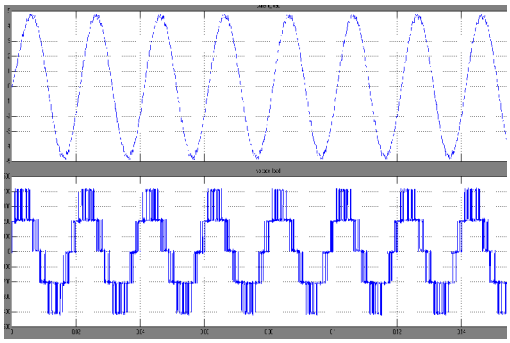
BLOCK DIAGRAM OF 3-LEVEL INVERTER

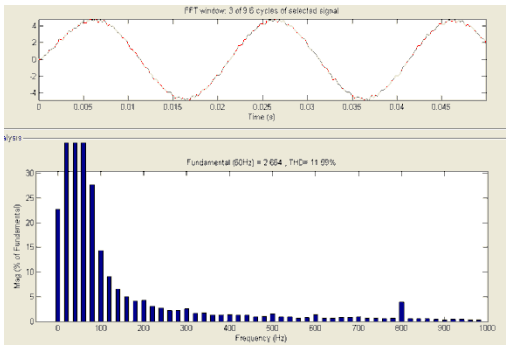
V. SIMULATION RESULTS

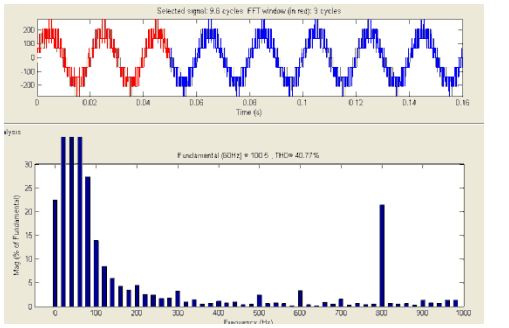












X. CONCLUSION

A simple Matlab/ Simulink model is presented to implement SVPWM for three phase VSI.A brief view of the VSI model is also reported based on space vector representation. A Matlab/ Simulink based model for implementation of SVPWM is presented. The step by step model gives an insight into the SVPWM. By varying the magnitude of the input reference different modulation index can be achieved.

XI. REFERENCES

1] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2] R. Teodorescu, F. Beaabjerg, J. K. Pedersen, E. Cengelci, S. U. Sulistijo, B. O. Woo, and P. Enjeti, "Multilevel converters—A survey," in *Proc. EPE Conf.*, 1999, pp. 2–11.

[3] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped pwm inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[4] T. Ishida, T. Miyamoto, T. Oota, K. Matsuse, K. Sasagawa, and L. Huang, "A control strategy for a five-level double converter with adjustable dc link voltage," in *Proc. Ind. Appl. Conf.*, Oct. 2002, vol. 1, pp. 530–536.

[5] A. Nabea, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on Industrial Application*, Vol.IA- 17, No. 5, pp. 518-523, September/October 1981.

[6] R. Teichmann, S.Bernet, "A Comparison of Three-Level Converters Versus Two-Level Converters for Low-Voltage Drives, Traction, and Utility Applications," *IEEE Transaction On Industry Applications*, Vol.41, No. 3, pp: 855-865, May/June 2005.

[7] C. Newton, and M. Sumner, "Multi-level converters, a real solution to medium/high-voltage drives? "*Power Engineering Journal*, Vol. 12, Iss.1, pp: 21-26 , Feb. 1998.

[8] J. H. Seo, C. H. Choi, and D. S. Hyun, "A new simplified space-vector PWM method for three level inverters," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 545–550, Jul. 2001.

[9] R. Jotten, "A fast space–vector control for a three-level voltage source inverter," in *Proc. EPE Conf.*, 1991, pp. 70–75.

[10] J. *S.* Lai. and F. Z. Peng, "Multilevel converters-a new breed of power converters," LEE *Trans. Ind. Applicm..* vol. 32. pp. 509-5 17, Mny.lJun. 1996.

[11] M. D. Manjrekar, P. K. Steirner, and T. A. Lipa, "Hybrid multilevel power conversion system: a competitive solution for high- power applications." LEE€ Trans. *Ind, Applicot.,* vol. *36,* pp. 834-841, May.lJun. 2000.

[12] J. Rodriguez, I. S. Lai, and F. Z. Peng. "Multilevel inverters: a survey of topologies, controls, and applicntions," *IEEE Trans. Ind Elecrron..* vol. 49, pp. 724-738, Aug. 2002. N. Celanovic, and D. Boroyevich, "A fast space-vector modulation algorithm far multilevel three-
phase canvertc~."IEEE *Truns. on Ind. Applicor..* vol. *37,* pp. 637-641, MarJApr.2000

[13] **I.** F. Z. Peng. **"A** genenlired multilevel iwmer topology with self voltage balancing," IEEE ***Trans. on Ind. Applrcal.,*** **vol. 37,** pp.611-618. MadApr. 2001.